Integratie van Actieve en Passieve Componenten in Polyimide Interconnectie Substraten

Active and Passive Component Integration in Polyimide Interconnection Substrates

Wim Christiaens

Promotor: Prof. dr. ir. J. Vanfleteren

Proefschrift ingediend tot het behalen van de graad van
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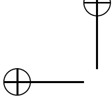
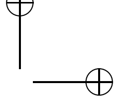

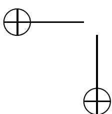

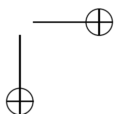

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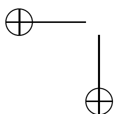
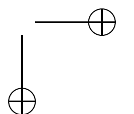

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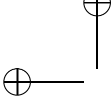
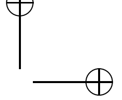

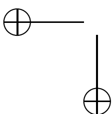

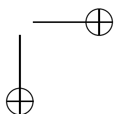

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Wim Christiaens

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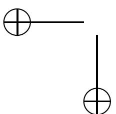
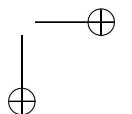

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Samenvatting

Een van de grote uitdagingen voor de elektronische productie- en verpakkingsindustrie blijft de integratie van steeds meer functies in hetzelfde, of zelfs minder, volume. De performantie en het aantal functies van elke nieuwe generatie producten blijf steeds toenemen, terwijl de afmetingen en het gewicht van deze nieuwe producten steeds maar afnemen. Om hieraan te kunnen blijven tegemoetkomen, integreert de halfgeleiderindustrie meer en meer transistoren op hetzelfde siliciumoppervlak. Daardoor kan men ofwel de chipafmetingen reduceren, ofwel de functionaliteit op hetzelfde oppervlak vergroten. Daarnaast, is er ook een stijgende interesse om de verpakkingsdichtheid te verhogen. Terwijl de silicium chips steeds meer functies bevatten, is er ook voor de elektronische verpakking de grote uitdaging om steeds meer te integreren en dus te verkleinen.

Een hoge graad aan miniaturisatie kan bereikt worden door de geassembleerde, actieve componenten van de oppervlakte van de printkaart te verwijderen en ze te integreren binnenin de lagen van de meerlaagse substraten. Voorliggend doctoraatswerk presenteert dergelijke 3D integratie van dunne chips in flexibele meerlaagse substraten, dit d.m.v. een uniek concept voor het verpakken van ultra-dunne chips: de Ultra-Thin Chip Package (UTCP).

Silicium chips, met een dikte van zelfs minder dan 30 μm, worden verpakt tussen 2 spin-on polyimide lagen, als UTCP verpakking. Dit resulteert uiteindelijk in een zeer dunne, zelfs plooibare, chip verpakking, met een totale verpakkingsdikte van nauwelijks 50–60 μm.

De UTCP kan dienst doen als flexibele interposer, die dan kan gebruikt worden om verder te integreren in het substraat, bijvoorbeeld als alternatief voor de directe integratie van naakte siliciumchips. De UTCP verpakking heeft als voordeel dat de chip gemakkelijk kan getest worden voor integratie, en dat de verpakking ook een uitwaaiering van de chip contacten voorziet, zodat men dan geen hoge densiteitsubstraten dient te gebruiken met dezelfde pitch als de chip contacten.

De 3D integratie van de UTCP verpakte chips leidt tot verhoogde miniaturisatie, aangezien boven en onder de geïntegreerde chip ook nog SMD componenten kunnen geplaatst worden. Bovendien zijn de UTCP verpakte, dunne silicium chips zelfs plooibaar, wat de totale flexibiliteit van het uiteindelijke systeem ten

goede komt.

Alle processtappen van de Ultra-Thin Chip Package technologie worden uitgebreid besproken in Hoofdstuk 2. Een 20 μm dikke, spin-on polyimide laag, aangebracht op een stijve glas drager, vormt het basissubstraat. De verpakking zal achteraf gemakkelijk losgemaakt kunnen worden: alvorens de polyimide aan te brengen, worden de randen van het glas substraat gecoat met een adhesiepromotor. Bijgevolg zal de onderste polyimide laag zeer goed hechten aan de randen van de substraten, maar bijna niet in het midden. Maar desondanks is de adhesie wel voldoende tijdens de volledige procescyclus. Op deze onderste polyimide laag, worden de chips, met de contacten naar boven, vastgelijmd met een druppeltje BCB. Vervolgens wordt de bovenste polyimide laag aangebracht en worden vias naar de contacten geopend. Verschillende laser technieken werden hiertoe ontwikkeld, alsook droog (RIE) etsen van de vias werd gedemonstreerd. Uiteindelijk wordt het top metaal aangebracht: een TiW Cu laag wordt gesputterd en daarin wordt het interconnectiepatroon dan fotolithografisch gedefinieerd. Indien gewenst, kunnen dikkere metaallagen gevormd worden door middel van electroplating.

Hoofdstuk 3 licht de uitgebreide haalbaarheidstudie toe voor de UTCP technologie. IMEC interconnectie testchips werden UTCP verpakt. Een specifiek test design maakt vierpuntsmetingen van de via weerstanden mogelijk, alsook kettingen van weerstanden kunnen gemeten worden. Typische via weerstanden op de UTPC verpakkingen zijn lager dan 30 mΩ. Verschillende betrouwbaarheidstesten zijn uitgevoerd op deze test vehikels, ze werden onderworpen aan thermische cycli tussen -40°C en +125°C, temperatuur/vochtigheid test op 85°C/85 r.h. en aan hoge temperatuur (125°C/150°C). Geen enkele faling werd vastgesteld na 1000 u op 85°C/85 r.h. of na 1000 thermische cycli tussen -40°C en +125°C. De eerste testen op hoge temperatuur waren echter minder positief, maar deze slechte resultaten konden niet bevestigd worden tijdens een tweede studie met gelijkaardige UTCP's. Dwarsdoorsnede en EDAX analyse op de gefaalde UTCP's kon geen duidelijke oorzaak aanduiden. Enige verschil was de aanwezigheid van Cu interconnecties op de gefaalde chips.

De UTCP technologie is ook gedemonstreerd met functionele circuiten. Onverpakte, verdunde TI microcontrollers and Nordic radio chips werden geïntegreerd als UTCP, en hun functionaliteit werd gedemonstreerd na verpakken. De verpakte microcontrollers konden succesvol geprogrammeerd worden, bovendien wezen uitgebreide testen van de ADC aan dat de UTCP verpakking slechts heel weinig invloed heeft: de afwijkingen zijn minimaal en zullen bijna geen invloed hebben op de bruikbaarheid van de microcontroller. Hoogstwaarschijnlijk zijn deze afwijkingen eerder te wijten aan parasitaire effecten op de UTCP verpakking. Ook de functionaliteit van Nordic radio chip is gedemonstreerd na verpakking, en was minstens even goed als een conventioneel verpakte radio chip.

Daarnaast worden in ditzelfde hoofdstuk ook nog een paar FEM simulaties aangehaald. Deze bevestigen enerzijds de beperkte stress die geïntroduceerd wordt tijdens processen (dankzij een geschikte materiaalkeuze, nl. de combinatie van een laag CTE polyimide en het silicium), en anderzijds ook de mechanische plooibaarheid van de UTCP verpakkingen.

Hoofdstuk 4 demonstreert de 3D integratie van actieve componenten in de binnenlagen van commerciële, meerlaagse flexibele substraten. De UTCP verpakkingen doen dienst als tussenstap: ultra-dunne silicium chips worden eerst verpakt als UTCP, die op hun beurt geïntegreerd kunnen worden in standaard dubbelzijdige flex substraten. Eerst werd een geschikte procescyclus opgesteld door ACB, een Belgische flex producent: de UTCP's kunnen gealigneerd en gefixeerd worden op een flex binnenlaag en worden, na laminatie, dan door middel van vias geconnecteerd met de geleiders van de PCB of FCB. Dit integratieconcept werd vooreerst gedemonstreerd met UTCP test substraatjes. Uit deze testen bleek dat 3.5 μm Cu dikte op de UTCP verpakking een voldoende goede interconnectie kan voorzien na embedden, alsook dat een eventuele ENIG finish op de UTCP verpakkingen geen bijkomende problemen stelt voor de metallisatie van de doorverbindingen tussen verpakking en substraat. Weerstanden naar de geïntegreerde verpakkingen werden gekarakteriseerd en gemonitord tijdens betrouwbaarheidsstudies. Zowel het onderwerpen aan 1000 u op 150°C, als aan 1000 u vochtigheid/temperatuur (85°C/85 r.h.), als aan 1000 thermische cycli (-40°C/+125°C) blijkt geen falingen in de interconnecties te introduceren. Bovendien blijkt het integratieproces ook geen invloed uit te oefenen op de vierpuntsweerstanden van de interconnecties op geïntegreerde UTCP verpakkingen.

De 3D integratie is ook toegepast voor de integratie van een functionele microcontroller voor een draadloos ECG systeem. Een Texas Instruments microcontroller, MSP430F149, werd succesvol ingebed in een standaard dubbelzijdig flex substraat, met zelfs aan boven en onderzijde nog geassembleerde SMD componenten bovenop de microcontroller. Dit resulteerde in een perfect werkende, volledig functioneel, draadloos biopotentiaal systeem met geïntegreerde microcontroller.

Hoofdstuk 5 stelt twee alternatieve UTCP technologieën voor, beide gebaseerd op fotodefinieerbare polyimides. Een eerste concept presenteert vlakke UTCP verpakkingen. Deze technologie maakt gebruik van een extra, HD-7012, fotodefinieerbare polyimide laag, waarin caviteiten kunnen gedefinieerd worden. De chips worden dan geplaatst in deze caviteiten, resulterend in vlakkere UTCP verpakkingen. De proces optimalisatie voor de realisatie van een symmetrische polyimide opbouw wordt nader toegelicht. Dit werk werd uiteindelijk verdergezet voor de integratie van beeldschermaansturing in het kader van het Europese Flexidis project. Een tweede alternatieve UTCP technologie maakt gebruik van fotodefinieerbare vias. De PI-2611 toplaag wordt hierin vervangen door het fotodefinieerbare PI-2731. Daarin konden 60 μm vias gerealiseerd wor-

den naar de geïntegreerde chips.

Hoofdstuk 6 beschrijft de optimalisatie van een silicium verdunningsproces voor individuele chips. Conventionele silicium verdunningsprocessen zijn gebaseerd op het verdunnen van volledige wafers. Maar aangezien functionele wafers soms heel moeilijk verkrijgbaar zijn, en deze ook zeer kostbaar kunnen zijn, kan het in sommige gevallen zeer interessant zijn om individuele chips te kunnen verdunnen. Daartoe werd een Logitech PM5 machine in het labo geïnstalleerd, en werd daarop een lap- en polijstproces voor het afdunnen van individuele silicium chips geoptimaliseerd. Het lapping proces verwijdert het silicium vrij snel, terwijl het verwijderen van eventuele schade in het silicium gebeurt tijdens het polijstproces, wat uiteindelijk resulteert in een zeer gladde oppervlakte-afwerking. Microcontrollers, aanstuurchips voor beeldschermen, radio chips en zelfs MEMs konden op die manier succesvol verdund worden, van originele chip dikte van 700 μm tot diktes zelfs minder dan 20 μm, zonder schadelijke effecten voor de functionaliteit.

Uiteindelijk wordt in Hoofdstuk 7 een 'dunne film op flex' technologie voorgesteld. Hier worden de dunne film technologieën die gebruikt zijn voor de UTCP productie, toegepast voor de productie van zeer dunne, extreem plooibare, polyimide substraten. Hoge resolutie, meerlaagse, flex structuren kunnen opgebouwd worden op tijdelijke rigide dragers door repetitieve applicatie van spin-on polyimide lagen en gesputterde metaallagen. Deze technologie is gedemonstreerd tot 3 verschillende metallisatielagen voor het vervaardigen van hoge precisie RF structuren. De individuele processtappen en hun optimalisatie worden nader toegelicht in dit hoofdstuk.

Summary

One of the main challenges in the electronics manufacturing and packaging development is how to integrate more functions inside the same, or even smaller, size. The electrical performance and the number of functions of every new product generation are increasing while the size and the weight of the products are decreasing. To meet this, the semiconductor industry is integrating more and more transistors into the same silicon area. This allows either to reduce the size of the IC or to increase the functionality and performance of the same size IC components. At the same time there is also an interest to increase the packaging density. While silicon chips continue integrating more functionality as per Moores law, the packaging is challenged to also integrate and shrink.

A high degree of miniaturization can be achieved by removing the assembled active devices from the surface and integrate them inside the inner layers of multilayer FCB or PCB boards. This PhD dissertation presents the embedding of thin dies inside (flexible) multilayer boards, by means of a unique concept for packaging ultra-thin chips: the Ultra-Thin Chip Package (UTCP).

Silicon devices, with thickness below 30 μm, can be packaged in between 2 spin-on polyimide layers as UTCP package. The result a is a very thin, even flexible, chip package, with a total package thickness of only 50–60 μm.

The UTCP will serve as flex interposer and can be used for the embedding inside the substrate, replacing for example the direct integration of bare dies. The UTCP allows for easy testing of the chip before embedding, solving the KGD issue, and provides a contact fan out with more relaxed pitches, eliminating the need for very fine pitch PCB or FPC compatible with the chip contact pad pitch.

The 3D integration of UTCP packages leads to high density integration, since SMD components can be mounted on top and bottom of the integrated devices. In addition, the UTCP packaged thin silicon devices are mechanically flexible themselves, leading to an increased total flexibility of the resulting system.

All individual process steps of the Ultra-Thin Chip Package technology are discussed in detail in Chapter 2. The base substrate is a uniform, 20 μm thick, polyimide layer, applied (spin coated and cured) on a glass carrier. An easy release of the package from the rigid substrate is obtained in a special way: before spinning

the polyimide layer, the 4 edges of the square glass substrate are coated with an adhesion promoter. The consequence of this is that the first layer of polyimide adheres well to the edges of the substrates, and has marginal adhesion strength to the centre of the substrate. However, the adhesion to the edges is sufficient to allow for the whole process cycle. On top of the first polyimide layer the ultra-thin chip is placed, face-up, and fixed using dispensed BCB as die attach material. Next, the die is covered with another 20 μm thick polyimide and vias to the contacts of the integrated device are opened. Different laser ablation based via technologies are developed and discussed. Also feasiblity of dry etching of microvias using Reactive Ion Etching has been demonstrated. The final processing step is the top metal deposition. A TiW Cu interconnection layer is deposited by sputtering and photolithographically patterned, metallizing the contacts to the chip and providing a fan out to the contacts of the chips. If needed, the sputtered top metal layer can also be enforced by electroplating.

An extensive feasibility study for the developed UTCP technology is included in Chapter 3. Interconnection test vehicles are produced, based on IMEC interconnection test chips, allowing for four-point measurements of via resistances and for daisy chain measurements. Typical via resistance values for the chip contacting on the UTCP packages are below 30 mΩ. Different reliability investigations are reported: test vehicles were subjected to thermal cycling test between -40°C and +125°C, temperature/humidity testing at 85°C/85 r.h., and to thermal ageing at 125°C and 150°C. No failures occurred during 1000 h storage at 85°C/85% r.h. or during temperature cycling between -40°C and +125°C up to 1000 cycles. First high temperature storage testing indicated early failures, but these bad results were not confirmed in a second study, using similar UTCP test samples. Failure analysis (cross sections, EDX) only indicated the presence of Cu interconnects on the failed interconnection test chips.

The UTCP technology has also been demonstrated for the packaging of ultra-thin, functional devices. Bare, thinned, TI microcontroller and Nordic radio devices were UTCP packaged, and functionality was demonstrated after embedding. UTCP embedded microcontrollers could be successfully programmed (and retained their program). Extensive tests of the ADC of the embedded microcontrollers indicated that the UTCP performs only slightly worse than the bare, unpackaged devices. These small deviations are limited and will have only little effect on the usability of the packaged microcontroller. Most probably they are caused by parasitics on the UTCP package. Also the UTCP packaged Nordic radio device showed perfect functionality after embedding, at least as good as could be achieved for a conventional packaged Nordic radio device.

Also some FEM simulation results are included in Chapter 3, confirming the limited stresses introduced in the package during the processing. This can be explained by the material selection: combination of the low CTE polyimide with the silicon material. Simulations on mechanical bending of the UTCP packages

confirm the bendability of the UTCP packages.

Chapter 4 presents a technology for the 3D integration of active devices inside the inner layers of commercial flexible multilayer circuits. The UTCP packages serve as interposers: ultra-thin active devices are first integrated as UTCP, which is in turn embedded inside a standard double-layer flex PCB. A suitable process flow to integrate small UTCP packages inside large flex laminates has been successfully established at ACB, a Belgian flex manufacturer: UTCP packages are aligned and fixed (by heat tack) on a patterned inner layer of the multilayer substrate and connection between package and wiring of the PCB or FCB is achieved by through hole interconnects. This embedding concept has first been demonstrated with UTCP test packages, indicating that 3.5 μm metal thickness on the UTCP package is sufficient to ensure good interconnects and that an ENIG metal finish on the UTCP samples will not affect the through hole plating quality. Daisy chain interconnects between integrated dummy packages and the FCB were characterized, and monitored during reliability investigations. High temperature storage at 150°C (up to 1000 h), hot humidity storage at 85°C/85 r.H. (up to 1000 h) and thermal cycling between -40°C and +125°C (up to 1000 cycles) did not introduce any failure of the interconnects. The integration process does also not affect the values of the 4PT via resistance of the interconnects on the UTCP package.

This 3D technology was used for the integration of a functional microcontroller device for a wireless ECG application. A Texas Instruments microcontroller, MSP430F149, was removed from the surface of the substrate and successfully integrated inside a standard double-layer flex PCB, with even smaller SMD components mounted above and below the embedded chip, realizing a fully functional wireless biopotential system.

Two alternative UTCP technologies, based on photodefinable polyimides, are presented in Chapter 5. First, a concept for producing flat ultra-thin chip packages has been introduced. This technology introduces an extra HD-7012 photodefinable polyimide inner layer, in which cavities are defined. The chips can be placed in these cavities, realizing more flat packages. Process optimization, realizing the symmetric polyimide stack and demonstrating the principle, is presented. This technology has been further optimized and used for display driver integration in flexible substrates in the framework of the European Flexidis project. A second technology describes a UTCP package with photodefined vias. The PI-2611 top layer of the conventional UTCP is replaced by a photodefinable PI-2731 polyimide layer: 60 μm vias to integrated interconnection test chips have been realized, and characterized after metallization.

Chapter 6 describes the optimization of a silicon thinning process for individual dies. Most of the silicon thinning processes, available at the moment, are based on full wafer thinning. As full wafers with functional dies are not always accessible and as these wafers can be extremely costly, it can be very interesting to be able to thin down individual devices. A Logitech PM5 machine was installed in the

lab and a combined lap- and polishing process was successfully optimized for back thinning individual silicon dies. The lapping process ensures a fast back grinding step, while the polishing process removes the back surface damage and ensures a smooth back surface finish of the thinned die. This thinning process has been demonstrated for several functional dies: microcontrollers, display drivers, radio chips and MEMs devices are thinned from original silicon thickness, up to 700 μm, down to thicknesses even below 20 μm, without any loss in functionality.

Finally, a 'thin film on flex' technology is presented in Chapter 7. Thin film technologies, also used for UTCP package production, are applied for the production of ultra-thin, extremely flexible, polyimide substrates. High resolution multilayer flex structures can be built-up on temporary carrier substrates by repetitive application of polyimide layers by a spin-on process and metal layers by sputtering. The technology has been demonstrated with three metalization layers and has been used for realizing high resolution, high precision RF structures. All processing optimization work is included in this chapter.

Notations

Notation	Meaning
ASIC	Application Specific Integrated Circuit
BCB	Benzocyclobutene
CiP	Chip in Polymer
CiSP	Chip-in-Substrate Package
COB	Chip-On-Board
COF	Chip-On-Flex
CSP	Chip Scale Package
CTE	Coefficient of Thermal Expansion
DNL	Differential Nonlinearity
ECG	Electrocardiogram
EEG	Electroencephalogram
ENIG	Electroless Nickel / Immersion Gold
ENOB	Effective Number Of Bits
EMG	Electromyogram
FCB	Flexible Circuit Board
FCIP	Flip-Chip In Package
FCOB	Flip-Chip On Board
GSG	Ground-Signal-Ground
IC	Integrated Circuit
IPD	Integrated Passive Devices
INL	Integrated Nonlinearity
KGD	Known Good Die
LSB	Least Significant Bit
MEMS	Micro Electro Mechanical Systems
MCM	Multi Chip Module
PCB	Printed Circuit Board
PDPI	Photodefinable Polyimide
PEB	Post Exposure Bake
PI	Polyimide
PiP	Package-in-Package

PoP	Package-on-Package
PWB	Printed Wiring Board
QFP	Quad Flat Package
RIE	Reactive Ion Etching
rpm	rotations per minute
RT	Room Temperature
sccm	Standard Cubic Centimeters per Minute
SEM	Scanning Electron Microscope
SFDR	Spurious Free Dynamic Range
SiP	System-In-Package
SMD	Surface Mount Device
SMU	Source Measurement Unit
SNR	Signal to Noise Ratio
SoC	Systems-On-Chip
SOLT	Short-Open-Load-Thru
THD	Total Harmonic Distortion
TSV	Through-Si-Vias
TTV	Total Thickness Variation
UBM	Under Bump Metallurgy
UTCP	Ultra-Thin Chip Package
USA	Ultrasonic Agitation
UV	Ultra Violet
WLP	Wafer Level Packaging

Chapter 1

Introduction

1.1 Electronic packaging

One of the main challenges in the electronics manufacturing and packaging development is how to integrate more functions inside a device, maintaining the same, or even smaller, size. The electrical performance and the number of functions of every new product generation are increasing, while the size and the weight of the products are decreasing. To meet this, the semiconductor industry is integrating more and more transistors into the same silicon area. This allows either to reduce the size of the IC or to increase the functionality and performance of the same size IC components. At the same time there is also an interest to increase the packaging density. While silicon chips continue integrating more functionality as per Moores law, the packaging is challenged to also integrate and shrink.

Figure 1.1 gives an impression on how a possible footprint reduction can be realized by using novel single die packages, compared with a typical SMD package, such as the Quad Flat Package (QFP) [1].

A first alternative technology depicted on this figure is the Chip On Board (COB) technology: the chip is attached directly on the substrate and interconnected by wire bonds to the wiring of the board. A next alternative involves the Chip Scale Package (CSP): dies are packaged, with maximum total package size of 1.2 times the die size. Further reduction in footprint is finally achieved by using True Chip Scale Packages (package size equals die size) or by flip chip assembly of the die face down on the substrate.

This way, the space requirement of active chips could already be reduced to a minimum by implementing CSP's (chip size packages) or flip chips. Saving the volume and weight of the package, significant reduction in footprint was achieved.

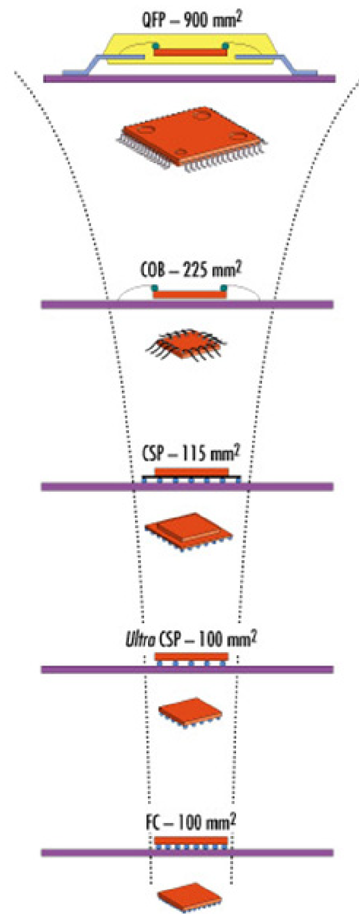

Figure 1.1: Possible foot print reduction for single chip package, offered by novel packaging technologies (Figure copied from [1], initial source unknown)

A next step conceived to further miniaturization is the integration of functions on miniaturized subsystems, i.e. System-in-Package (SiP), or even a full silicon integration (System-on-Chip, SoC).

But for some applications even this degree of miniaturization is still not sufficient. More space can be saved by making use of the third dimension. Possible 3D approaches include stacking of the dies on top of each other inside the packages, module stacking or foldable modules. Another alternative is the direct integration of active components inside the multilayer boards: the assembled packages are removed from the outer layers of the substrates and incorporated inside flex

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or PCB board inner layers.

This PhD dissertation will present a technology for embedding thin dies inside (flexible) multilayer boards, by means of a unique concept for packaging ultra-thin chips: the Ultra-Thin Chip Package (UTCP). This UTCP technology can provide ultra-thin flexible interposers suitable for the integration of active devices in conventional multilayer circuit boards, replacing for example the embedding of bare dies. The interposers allow for easy testing before embedding (solving the KGD issue), and also provide a fan-out to the chip contact pads, relaxing the interconnection contact pitch and excluding in this way the need for high density PCB or FCB.

This chapter will introduce first some of these latest electronic packaging trends, mentioned above, towards higher density packaging, prior to introduce the research performed in the framework of this PhD study.

Remark: this introduction is only very short, more extensive information on the latest electronic packaging developments and on the technology roadmaps is provided by [2, 3, 4, 5, 6].

1.1.1 Flip chip versus wire bonding

There are different ways for die attachment in electronic packages. Wire bonding is still used to assemble the vast majority of semiconductor packages. But for different type of applications flip chip gained in popularity as a packaging strategy [2].

For wire bonding the individual dies are fixed face-up on the substrate and interconnected by small wires to their carriers. These wires can lead from the IC contact pads to pins on the outside of the carriers, or eventually directly to the interconnections on the substrate.

An alternative technology for this wire bonding is flip chip. Flip chip microelectronic assembly is the direct electrical connection of face-down ('flipped') electronic components onto substrates, circuit boards, or carriers, by means of conductive bumps on the chip bond pads. Normally the area between the chip and the substrate is also filled with 'underfill'. This underfill protects the bumps from moisture or other environmental hazards, and provides additional mechanical strength to the assembly. However, its most important purpose is to compensate for any thermal expansion difference between the chip and the substrate. Underfill mechanically 'locks together' chip and substrate so that differences in thermal expansion do not break or damage the electrical connection of the bumps. Due to thermal expansion mismatch between the IC and the substrate, the flip chip solder joints experience fatigue damage during thermal cycling or power cycling. Underfill also improves the integrity and reliability of the assembly when subjected to mechanical shocks or bending.

Although flip chip assembly is not a new technology, it is gaining increasing popularity as a packaging strategy due to the benefits it can provide. For high-performance applications, the direct connecting of the die to a substrate or board greatly shortens the signal path while reducing the interconnect inductance and capacitance, all of which serves to greatly improve electrical performance. Flip chip also gives the greatest input/output connection flexibility. Wire bond connections are limited to the perimeter of the die, driving die sizes up as the number of connections increases. Flip chip connections can use the whole area of the die, accommodating many more connections on a smaller die. Also manufacturers of small electronics, like cell phones, pagers and other where the size savings are valuable: by using the entire surface of the die for establishing interconnect, the need for wire bond interconnect is eliminated and package size can be reduced.

Figure 1.2 compares a flip chip in package, with a wire bonded configuration.

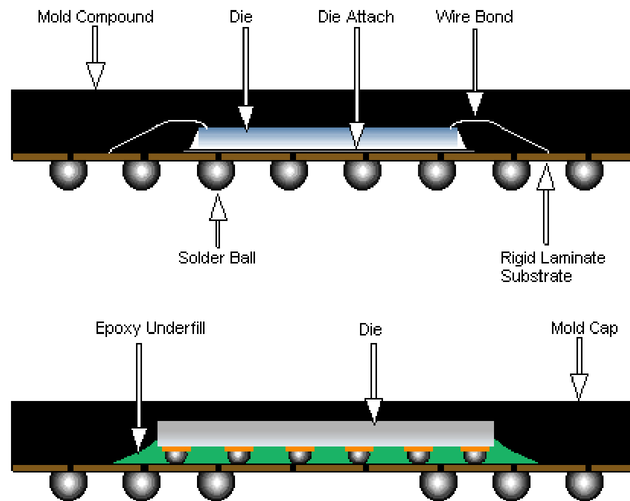


Figure 1.2: In the wire bond method (top), the die faces up and is attached to the package via wires. The flip chip (bottom) faces down and is typically attached via solder bumps similar to the larger ones that attach BGA packages to the printed circuit board (Image courtesy of Amkor Technology, Inc.)

1.1.2 Chip scale package

A Chip Scale Package (CSP), based on IPC/JEDEC J-STD-012 definition, is a single-die, direct surface mountable package with an area of no more than 1.2 x the original die area. The IPC/JEDEC definition likewise doesn't define how

a chip scale package is to be constructed, so any package that meets the surface mountability and dimensional requirements of the definition is a CSP, regardless of structure.

There are a number of different types of chip scale packages, each employed in a different combination of chip to package interconnect and interposer technology. CSPs come in many forms: flip-chip, wire-bonded, ball grid array, leaded, etc. and also include transfer molded and wafer-level packaging [7].

Wafer Level Packaging (WLP) is a technology in which all of the IC packaging process steps are performed at wafer level (so all package IO terminals will be located within the chip outline (fan-in design)).

Also embedded wafer level package technologies are now emerging. For this approach the chips are first reconstituted and embedded in epoxy compound to build an artificial wafer. A thin film redistribution layer is applied instead of a laminate substrate which is typical for classical BGAs.

Some examples of such WLP technologies are described in [8, 9, 10, 11].

Chip scale packaging can combine the strengths of various packaging technologies, such as the size and performance advantage of bare die assembly and the reliability of encapsulated devices. The significant size and weight reduction offered by the CSP makes it ideal for use in mobile devices like cell phones, laptops, palmtops, and digital cameras.

1.1.3 SoC - SiP

A next step towards further miniaturization is the integration of functions on miniaturized subsystems, i.e. System-in-Package (SiP), or even a full silicon integration (System-on-Chip, SoC).

'System on a Chip', or SoC, integrates multiple chip functionality onto one single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions all on one single chip-level system to come up with a complete electronic system that performs the more complex but more useful final product function. Thus, instead of building an electronic product by assembling various chips and components on a circuit board, SoC technology will allow all of these parts to be fabricated together on a single chip, which can function as the final product itself.

The advantages offered by SoC technology include: higher performance, smaller space requirements, higher system reliability and lower package costs. Of course, this SoC technology also poses some challenges: larger design space, higher design and prototyping costs, longer design and prototyping cycle time, more complex debugging, lower IC yields and higher wafer fab costs due to the relatively larger die sizes involved and the integration of intellectual property from multiple (and possibly independent) sources. Aside from these challenges, the task of

electrically testing SoC's is daunting as well. A SoC, in essence being composed of many different devices, requires a test system that can perform electrical testing on all its analog and digital circuit components.

System-on-a-Chip (SoC) must not be confused with System-in-a-Package (SiP). Systems-on-Chip employs technologically compatible functions integrated into a single die. If it is not feasible to construct a SoC for a particular application (mix of Si and gallium arsinide, high voltage and small signal), a system in package (SiP) can be the alternative comprising a number of chips in a single package.

System-In-a-Package allows a mix of functionally related but differently processed die into an integrated sub-system. The SiP is a device that consists of multiple individually fabricated chips that make up a complete electronic system housed in a single package. Thus, SiP pertains to an advanced type of packaging technology, while SoC deals with microchip fabrication technology.

With SiP, single or multiple ICs, along with discrete and embedded components, can be integrated in a high-performance, compact package that can be designed and manufactured very quickly, improving overall functionality and time-to-market.

As the electronics industry faces the challenge of integrating multiple technologies on a single piece of silicon, system-in-package (SiP) is seeing growing acceptance as a viable alternative to system-on-a-chip (SoC).

The SiP with side-by-side placement (horizontal) is actually a traditional multichip module (MCM) where wire bonding or flip-chip bonding technology has been used. The chief reason of this structure is to enable higher data transfer rate between dice on module by means of flip-chip bonding and build-up substrate. For commercial applications, even though this structure is considered to be an expensive structure, the side-by-side placement with small dice may not expand the package size and keep the package inexpensive. A die-stacked structure is mostly cheaper than the side-by-side placement in terms of packaging cost.

1.1.4 3D packaging

For some applications the above described degree of miniaturization is still not sufficient. Only the application of 3D-packaging methods can provide further decrease in footprint and volume. A 3D packaging approach utilizes the vertical dimension, usually with no additional area required on the PCB and the height is typically equivalent to single die packages due to the use of thinner dies.

There are different approaches for 3D modules. A first possibility is by stacking multiple dies inside the packages, other alternatives include stackable modules and foldable modules. But an even higher level of integration will be achieved through removing the packages from the surface and embedding of the ICs inside the FCB or PCB inner layers.

It is quite obvious that all these highly space-efficient configurations increase capacity and/or functionality in the same volume often facilitating new capabilities, e.g. 3rd generation PDA, with telephone, internet, GSM, photographic capability. These packages are very useful for all kind of applications with size and weight limitations such as cellular phones, thin laptops, PDA.

Stacked dies

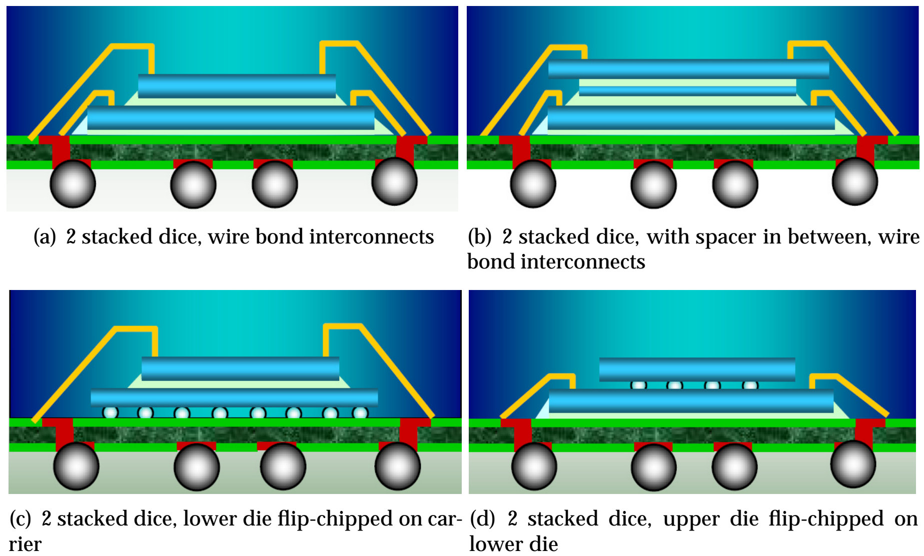
Die stacking has been used for consumer products such as cell phones for several years. Multiple chips are mounted on top of each other within a single semiconductor package, this significantly increases the amount of silicon chip area that can be housed within a single package of a given footprint, conserving precious real estate on the printed circuit board and simplifying the board assembly process. Aside from space savings, die stacking also results in better electrical performance of the device, since the shorter routing of interconnections between circuits results in faster signal propagation and reduction in noise and cross-talk. The stacked die may be interconnected using wirebonding alone, or by a combination of wirebonding and flipchip assembly [12, 13].

An alternative for interconnecting the dies in the single packages is TSV, 'through-Si-vias'. The dies or even complete wafers can be stacked on top of each other and are interconnected by microvias [14]. Since wire bonding is limited in density and performances, 3D stacking with microvias is necessary in the future for further miniaturization first and increased performances after. Through-silicon vias replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D package can also be flatter than an edge-wired 3D package.

Figure 1.3 and Figure 1.4 illustrate some possible stacked die configurations. More examples and information are found in [12, 13, 15, 16, 17, 18].

The ability to stack dies cost effectively in such non-reworkable 3D configurations will largely be determined by the quality of the dies that are used in it: use of defective dies in die stacking will result in yield losses and higher costs. Test before assembly can mitigate the multichip yield effects, but wafer-level testing is often not enough to ensure that only KGDs will be picked for die stacking, especially if the device involved is a complex circuit. Thus, poorly yielding wafers that are difficult to test at wafer level are not good candidates for die stacking.

In general die stacking becomes less attractive as the number of dies to be stacked increases and as the dies involved become more expensive or complex. In such cases, package stacking will be a valuable alternative for die stacking.

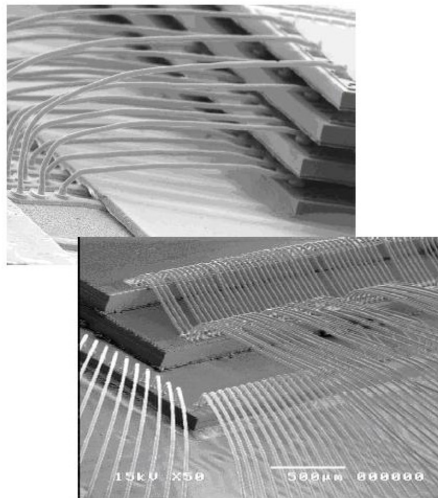


(a) 2 stacked dice, wire bond interconnects

(b) 2 stacked dice, with spacer in between, wire bond interconnects

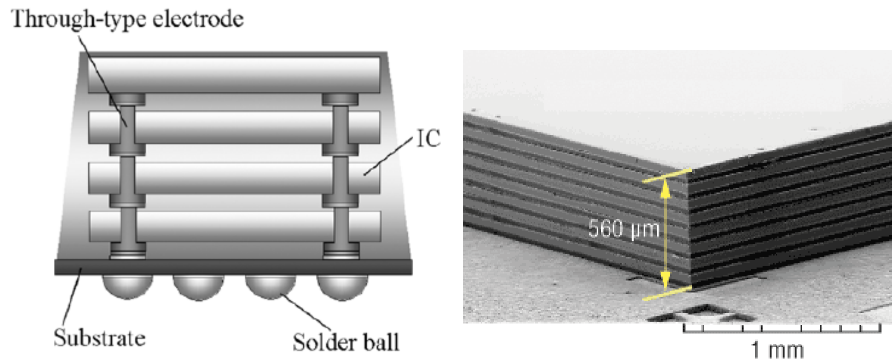
(c) 2 stacked dice, lower die flip-chipped on carrier

(d) 2 stacked dice, upper die flip-chipped on lower die



(e) Multiple stacked die configurations, interconnected by wirebonding

Figure 1.3: Some die stack configurations: (a)-(d) double die stacks (source: [13]), (e) multiple die stacks (source: [19])



(a) Schematic cross-section for stacking dies using TSV (picture courtesy of Seiko-Epson [19]

(b) Wafer level processed stack package, eight 2Gbit NAND flash chips, each 50m high, vertically stacked to a height of 0.56mm, developed by Samsung Electronics Co. Ltd. [20])

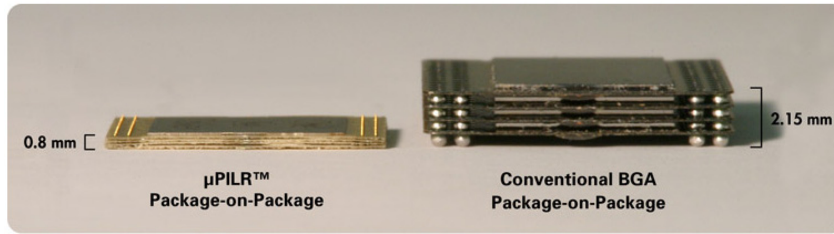
Figure 1.4: Interconnection of stacked dies by through-Si-vias (TSV)

Stacked packages

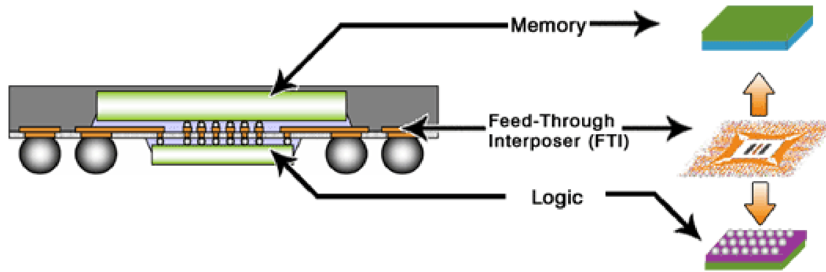
Beyond a certain point, that can vary substantially from one application and one IC provider to another, it may be necessary to consider building up the 3D stack in sub-units that can be assembled after package level burn-in and test, using a technology named Stackable Packages [21, 22].

The advantages offered by the package-on-package (PoP) architectures include memory flexibility and easy testing compared to e.g. ASIC + memory die stacking [23], and also the ability to mix and match devices from multiple vendors.

A lot of different PoP applications and architectures have been developed. Some recent examples include the μZ®- ball stacked package and the μPILR™ flash and DRAM PoP (Tessera, [24, 25]). Also NEC has some stacked technologies, see [26, 27], like the SMAFTI concept [28]. Figure 1.5 illustrates the μPILR™ and the SMAFTI concept.



(a) μPILR™ flash PoP compared with a conventional BGA package-on-package (source: Tessera, [24, 25])



(b) SMAFTI architecture (source: NEC, [26, 28])

Figure 1.5: Different PoP approaches

Figure 1.6 presents even a PiP (Package-in-Package) approach. The difference between PiP and PoP can be a little bit confusing. Instead of stacking the dies themselves, very thin packages, enclosing one or more dies, can be stacked as if it is one die. In the figure a PiP is depicted, such that the bottom die in the package stack is assembled and encapsulated while a thin tested package is stacked on top of the base package, wire bonded, and finally encapsulated like a conventional stacked die package [29].

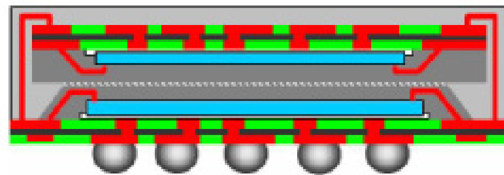


Figure 1.6: PiP package with single Land Grid Array (source: ChipPac, Inc. [30])

Foldable modules

Another alternative for stacking active devices is the technique of folding stacked dies, to eliminate the need for spacers between them, calling the process 'folded/stacked' technology. The dies are produced side by side and then folded over so that the bond pads are independent of each other. A relieving layer is placed between the chips to alleviate thermomechanical stresses.

This approach is a so-called 2-1/2 D technology: dies are 3D stacked in physical format but interconnected only through the circuits on folded flex.

One example of this architecture is shown in Figure 1.7: a three die μZ®-Folded Die Stack, from Tessera Inc. [24, 30]. Another example of such a folded module is based on the HiCoFlex substrates from HighTec MC AG and can be used for hearing aid applications [31, 32].

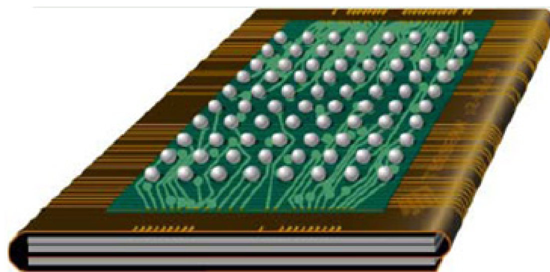


Figure 1.7: Tessera's Folded Die Stack technology utilizes a folding technique to combine multiple die in a single CSP (source: [13])

Integration of ICs in flex or PCB

The highest degree of miniaturization can be achieved by removing part of the assembled packages from the outer layers of the substrates and incorporate not only passive components, but also active circuitry (IC's), inside PCB or even FCB board inner layers. The complete product or system, including numerous passive and active components, can be integrated inside the motherboard (System-In-Board, SIB). Such modules allow assembly of surface mount devices on the bottom and top surface and are typically used as motherboards for the rest of the components.

Some technologies are already developed for integrating bare dies in the inner layers of multilayer substrates. Examples include the Chip in Polymer technology (CiP, [33, 34]), the Chip-in-Substrate Package (CiSP, [35]) and the Integrated Module Board technology (Imbera Electronics [36, 37, 38]).

These above mentioned technologies integrate the bare dies directly inside the

substrates. Possible hurdles for those technologies include the testing of the dies before embedding (Known Good Die problem), the necessary precise placement of the bare die, and the need for very fine pitch PCB or FPC (flexible printed circuit), compatible with the pad pitch of the embedded chip.

An alternative approach can be to provide an interposer, permitting the testing of the chip before embedding and providing a contact fan out with more relaxed pitches. This eliminates the need for precise placement and ultra high density printed circuit boards. Of course in order to be able to embed chip + interposer in the inner PCB or FPC layers, the unit itself has to be extremely thin, using ultra-thin interposer layers and chips.

This is precisely what has been developed within this PhD work: this dissertation will present the embedding of ultra-thin silicon dies inside (flexible) multilayer boards, by means of a unique concept for packaging ultra-thin chips: the Ultra-Thin Chip Package (UTCP).

Silicon devices, with thickness below 30 μm, can be packaged in between 2 spin-on polyimide layers as UTCP package. The result a is a very thin chip package, with a total package thickness of only 50–60 μm. This UTCP will serve as flex interposer and can be used for the embedding inside the substrate, replacing for example the direct integration of bare dies.

3D integration of UTCP packages will not only lead to high density integration, since SMD components can be mounted on top and bottom of the integrated devices, but also to an increased total flexibility of the resulting system, since the UTCP packaged thin silicon devices are mechanically flexible themselves.

1.2 Chip thinning

Packaged integrated circuit devices must not only be reduced in footprint but also in thickness. Die thickness is one of many crucial aspects for developing thinner and smaller packages: thin chips allow more functionality per unit volume in a stacked die package, reduce the weight, and even become flexible. In this way chip thinning can also improve the flexibility in applications like smart cards.

Provision of extremely thin components and semiconductors plays a decisive role in the steadily progressing development of highly integrated systems. The current chip thickness of about 100 μm for volume production is expected to decrease to about 50 μm in the near future and 20 μm within the next decade [39].

The most effective way for silicon backthinning, is the thinning of the whole wafer: suitable processes have been developed, and efficient thinning equipment is available, e.g. see [40]. But for a lot of research purposes it can be very useful to have also a thinning process available for thinning down individual chips. Very often one needs only a limited amount of thinned dies, and not a full wafer.

Purchasing whole functional wafers and thinning these wafers down would then be very costly. Therefore a dedicated individual die thinning process has been developed within this PhD work. A Logitech PM5 machine was installed in the lab and a combined lap- and polishing process has been successfully optimized for back thinning individual silicon dies. The lapping process ensures a fast back grinding step, while the polishing process removes the back surface damage and ensures a smooth back surface finish of the thinned die.

1.3 Thin film on flex

The thin film technologies, used for the production of the UTCP package, can also be applied for the production of ultra-thin, extremely flexible polyimide substrates. Multilayer structures can be built-up on temporary rigid carrier substrates by repetitive application of polyimide layers by a spin-on process, and metal layers by sputtering. This 'thin film on flex' technology can offer several advantages over traditional flex. Among these are: it allows for dense routing (thin film technologies), very fine features, very high performance and a perfect flat surface for component assembly (the thin flex stays on the glass carrier and will only be released after testing and assembly).

This technology was illustrated within this PhD study for the realization of ultra-thin, extremely flexible RF structures, but can be easily applied for other applications like: fine pitch interconnections, fine-pitch flip chips, resistor foils, RF parts, microstrip interconnects, etc.

Such high resolution flex substrates can be used to be assembled as a package or laminated inside multilayer flex substrates. This way, they offer the possibility to limit the need for high density parts of the total substrate only to a small area, realized with the thin film flex, e.g. for fine pitch flip chip or for having a high performance RF part, and they can exclude the need for a complete high density wiring board.

1.4 Research context

The research presented in this work was done in the Framework of the European SHIFT project. SHIFT is a European Commission (EC) funded Integrated Project in the frame of the IST (Information Society Technologies) Programme (contract number 507745) [41].

The objective of this project was the development of smart, high-integration, mechanically flexible electronic systems, for a wide variety of applications. 'Smart' means that the flexible multilayer laminate has embedded components, and that the different flex layers in the multilayer structure can have different functions,

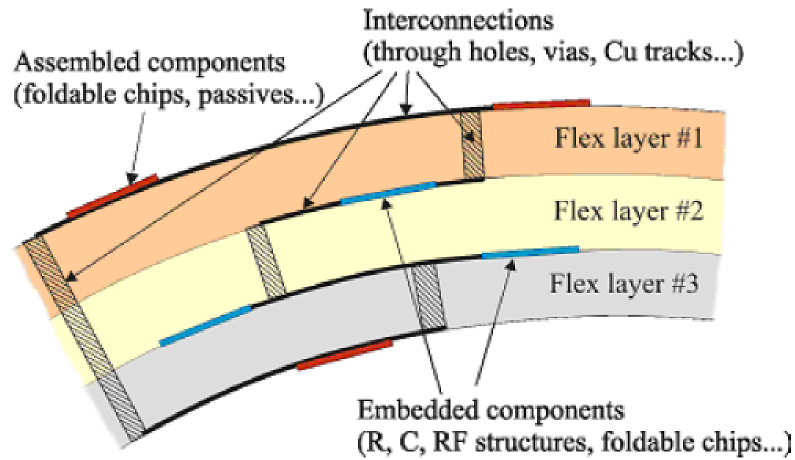


Figure 1.8: Principle of smart flex, including assembled components

meaning that it might be necessary to combine layers of different base material in the laminate. The principle of such smart flex, including assembled components, is shown in Figure 1.8.

Compactness of the resulting circuit is boosted by using the third dimension for electronic component integration (not only on front and back side, but potentially on every conductive layer). One possibility to obtain this 3D integration is offered by the polyimide based embedding technologies, developed during this PhD study.

1.5 Publications

The following patent application has been filed

- J. Vanfleteren and W. Christiaens. Method for embedding dies. *United States Patent application*, US2007/0134849 A1. Jun 2007.

The following journal papers have been submitted/published

- J. Govaerts, W. Christiaens, E. Bosman and J. Vanfleteren. Fabrication Processes for Embedding Thin Chips in Flat Flexible Substrates. *IEEE Transactions on Advanced Packaging*, Accepted for publication Aug 2008.

- P. Bauwens, A. Monte, W. Christiaens, J. Doutreloigne and J. Vanfleteren. Improved Passive-Matrix Multiplexability with Modular Display. *Displays*, Accepted for publication Dec 2008.

- W. Christiaens, E. Bosman, and J. Vanfleteren. UTCP: a Novel Polyimide Based Ultra-Thin Chip Packaging Technology. Paper submitted to *IEEE Transactions on Components and Packaging Technologies*.

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Chapter 2

UTCP technology

This chapter discusses the different process steps of the UTCP technology. The first section gives an overview of the optimized UTCP process flow, and the following sections describe the optimization of the different individual processing steps in more detail.

2.1 UTCP process flow overview

The Ultra-Thin Chip Package (UTCP) technology is a polyimide based embedding technology for integrating very thin silicon chips in flexible substrates. Dies with thicknesses down to 15 μm can be embedded in between two 20 μm thin spin-on polyimide layers, resulting in a package with a total thickness of only 50–60 μm. Thanks to the very low thickness of the chip, polyimide layers and metal, the whole package is even bendable. Figure 2.1 gives a brief overview of the optimized flow of the UTCP technology.

The base substrate is a 20 μm-thick polyimide layer spin-coated on a rigid glass carrier. For the fixation and the placement of the chips on the polyimide layer a benzocyclobutene (BCB) of about 5 μm is used as adhesive. By placing the chips properly with a dispensed benzocyclobutene, void-free bonds can be obtained. After the cure of the benzocyclobutene at 350°C, the chip is fixed on the polyimide layer. A covering polyimide layer is spin-coated on the fixed die with a layer thickness of about 20 μm. This way the chip is embedded in between two polyimide layers. For interconnecting the chip, contact openings to the bumps of the chips are laser drilled. Next, a top metal layer of 1 μm TiW/Cu is sputtered and photolithographically patterned, metallizing the vias to the chip and providing a fan out to the contacts of the chips. If needed the sputtered top metal layer can also be enforced by electroplating. Finally, after processing and functionality testing of the integrated devices, the whole package can easily be released from

its rigid carrier.

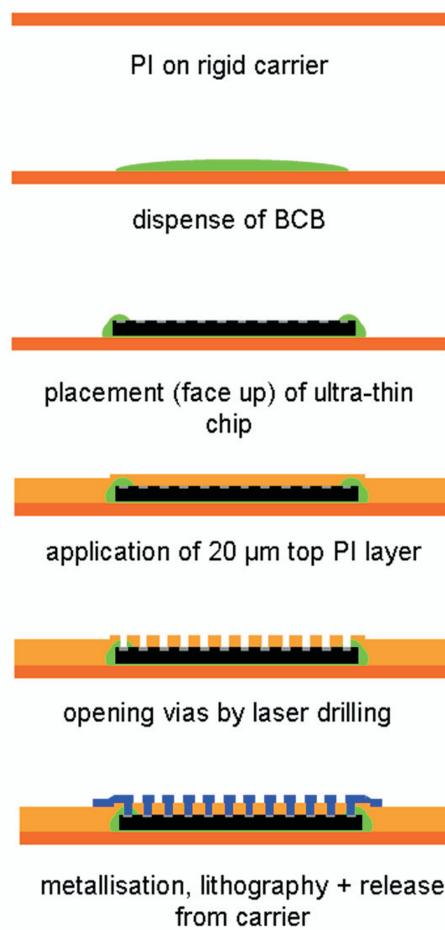


Figure 2.1: UTCP process flow overview

All these different processing steps are discussed in this chapter, including all detailed process parameters. First, also the selected polyimide material is introduced.

2.2 Selected polyimide

Polyimides are high temperature engineering polymers that exhibit an exceptional combination of thermal stability ($> 500\,^{o}$C), mechanical toughness and chemical resistance. In addition, they have excellent dielectric properties. Because of their high degree of ductility and inherently low CTE, these polymers can be readily implemented into a variety of microelectronic applications.

Several companies offer liquid polyimide products. For the UTCP technology a liquid polyimide from HD Microsystems was selected: the PI-2611. This type of polyimide not only offers excellent material properties (see below), but it is also used and recommended by our Swiss project partner, HighTec MC AG [1]. The use of their base materials can facilitate a possible transfer of our developed technology to the HighTec production facilities.

2.2.1 Material properties of PI-2611

PI-2610 and PI-2611 (PI-2600 Series) have both been well characterized by the semiconductor industry and are most frequently used as interlayer dielectrics due to a desirable combination of high performance cured film properties.

The polyimide structure of cured PI-2600 products offer low stress, low CTE, low moisture uptake, high modulus and good ductility for microelectronic applications. Their CTE of 3ppm / ^{o}C matches that of silicon. An overview of the material cured film properties is given in Table 2.1.

tensile strength	kg / mm^2	35
elongation	%	25
modulus	kg / mm^2	845
moisture uptake	%	0.5
dielectric constant (at 1 kHz, 50 % r.H.)		2.9
dissipation factor (at 1 kHz)		0.002
CTE	ppm	3
glass transition temp.	^{o}C	400
decomposition temp.	^{o}C	620

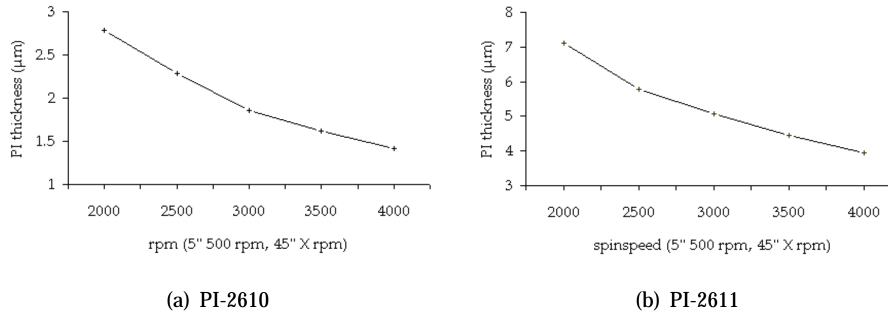
Table 2.1: Cured film properties for the PI-2600 Series polyimide, HD Microsystems [2]

These properties make the polyimide ideally suited as a dielectric layer for most semiconductor and MCM-D applications or wherever thick films or stacked layers of metallization are required. Patterning is typically done by dry etch or laser ablation techniques.

2.2.2 Process parameters

The PI-2610 and PI-2611 products are highly viscous solutions, and are deposited by spincoating. Before spincoating, the liquid is dispensed at the centre of the substrate. During dispensing, it is important to avoid trapped air in the solution. If bubbles are enclosed, one should allow them to dissipate out of the solution, otherwise coating 'comets' will result in the polyimide film. After dispense, the samples are first rotated at 500 rpm for 5 seconds, to ensure a nice spread of the material all over the substrate, and next rotated at final speed for 45 seconds, to reach the final layer thickness.

Cured layer thicknesses for the PI-2610 and PI-2611 are depicted in Figure 2.2. Achievable film thicknesses range between 1.5 and 3 μm for the PI-2610 and between 4 and 7 μm for the PI-2611.



(a) PI-2610

(b) PI-2611

Figure 2.2: Spin curves for the PI-2600 Series polyimides

These polyimides are cured in a vacuum oven up to 350°C, using the following cure profile:

- heating from room temperature to 200°C, with a ramp rate of 4°C per minute
- 30 minutes at 200°C
- heating from 200 to 350°C, with a ramp rate of 2,5^{o}C per minute
- 60 minutes at 350°C
- gradual cooling down to room temperature

During the cure of the polyimides, a small N_2 flow rate (5 sccm) is always added for a better removal of water and solvents evaporating from the spin-on polyimide.

To ensure improved adhesion on materials like metals, glass and semiconductor material, a silane adhesion promoter is recommended: the Pyralin VM652 [3]. This adhesion promoter has to be applied prior to the polyimide application. VM652 is spincoated at 3000 rpm for 30 sec and is dried during a 1 minute hot plate bake at 120 ^{o}C.

2.2.3 Moisture absorption

Polyimide materials are also known for absorbing a certain amount of moisture, called swelling. This occurs especially during wet processing (photoresist stripping, etching, etc.), but also when left out in the open and not stored in vacuum conditions.

This can affect certain process steps: e.g. evaporating water can cause blistering in sputtered metal layers. To avoid these effects this was taken into account during all UTCP processing. The substrates were always dried in an oven, after each wet processing step or after longtime storage in open air, and before the next processing step. A few hours at 200°C is usually sufficient to drive off most of the water.

2.3 UTCP base substrate preparation

The base material for the UTCP is a spin-on polyimide, the PI-2611 (HD Microsystems). This PI-2611 is selected as base material because of its excellent properties and its coefficient of thermal expansion of 3 ppm close to the CTE of inorganics used to make IC devices.

A rigid substrate is needed as carrier for the application of the spin-on polyimide. This section deals first with the selection of glass as a suitable carrier material and presents also a dedicated release technology in order to be able to release the cured polyimide film from its rigid carrier after processing the UTCP packages.

2.3.1 Glass as carrier material

As the selected polyimide has to be cured at very high temperatures, i.e. up to 350°C, it is important to limit the stress introduced in the polyimide layers during its curing cycle. Therefore it is important that the carrier material and the polyimide don't differ too much in CTE, since large CTE mismatches would introduce high stress in the polyimide layer during curing, which could result in curling after release from the carrier. The very low CTE of PI-2611 was a first reason to select glass is as suitable carrier material for processing with this PI-2611 spin-on polyimide. Glass is also a hard material and is known for its excellent

characteristics in dimensional stability.

All processing described in this PhD dissertation is developed using 5 cm x 5 cm Selected White Float glass substrates (from Praezisions Glas and Optik GmbH [4]). This glass guarantees a good flatness of the surface and has a CTE of 17 ppm.

Beside the advantage of the quite low CTE of the selected glass substrates, also the transparency makes this material very interesting: this enabled visual inspection from the backside of the package during all the optimization work of the UTCP processing.

In addition, also a very interesting release technology has been developed for obtaining selective adhesion between the polyimide PI-2611 and the glass carrier so that the package can easily be released from its carrier, after all necessary processing and testing steps. This release technology is described in the next section.

2.3.2 Polyimide release technology

A first possible release technology for spin-on polyimides, applied on rigid carriers, is the laser release method: polyimides are processed on glass carriers and can be separated by ablation with an excimer laser from the back [5]. This method implicates the use of an excimer laser and also requires expensive polished quartz substrates as substrate materials in order to have sufficient transmission of the laser beam for the excimer wavelength. Also Philips' EPLaR technology (Electronics on Plastic by Laser Release, [6]) requires a laser to remove the polyimide substrate from its carrier.

Another possible release technology could be the application of an extra separation layer in between the carrier and the first polyimide layer. After processing this release layer has to be dissolved for removing the polyimide from the carrier. This technology is used by HighTec MC AG [1].

For the UTCP technology, another interesting method for releasing polyimide layers from glass carriers has been developed. This method eliminates the need for using a(n excimer) laser or an expensive quartz glass carrier or any extra release layer. The release of the cured polyimide film from the glass carrier can be obtained in a special way: by selective application of an adhesion promoter on the carrier substrates. The polyimide has a very bad adhesion on glass substrates, but if the glass is coated with a dedicated adhesion promoter (Pyralin^{TM} VM652 from HD Microsystems) the polyimide has a very good adhesion on glass. VM652 is a dedicated adhesion promoter which is used to improve the adhesion of the polyimide to substrates as silicon dioxide or silicon nitride coatings [3] and is also working for the selected silica-based glass substrates. So selective adhesion of polyimide is easily obtained by coating only the edges of the glass substrates with the adhesion promoter. After curing, the polyimide will have only marginal

adhesion in the middle of the substrate and very good adhesion at the edges of the carrier. The polyimide can easily be removed from the carrier by simply cutting out the cured polyimide film from the glass. This way the UTCP packages will be processed starting from this base polyimide layer applied on the glass carriers and can easily be cut out from the carrier after processing. Using this release technology the UTCP is carried on this rigid substrate during the whole processing cycle, as shown above in figure 2.1. This makes it possible to make use of very fine pitch thin-film techniques during processing and also to test the package on the rigid carrier with standard (rigid) test equipment before release. The result is a very flexible chip package after release.

2.3.3 Cleaning procedure for glass substrates

Before preparing the base samples and processing the polyimide, the glass substrates are first thoroughly cleaned. A simple clean by rinsing the substrates for 2 minutes in acetone, followed by 2 minutes in acetone/isopropanol turned out to be insufficient to ensure that all greases and dirt are removed from the glass substrates. Therefore a cleaning procedure based on RBS 25 cleaning agent has to be done. The different steps for this cleaning procedure include:

- put substrates in 5% RBS solution for 12 hours
- ultrasonic agitation (USA) during 5 min in RBS
- rinse two times in DI water
- USA during 5 min in DI water
- rinse two times in isopropanol
- rinse in DI water
- dry with N_2 gun.

If the glass substrates are not cleaned thoroughly, hydrophobic problems can arise during the application of the adhesion promoter.

2.3.4 Processing parameters for UTCP base substrates

As described above, selective adhesion of the polyimide on the glass is obtained by selective coating of the carriers with adhesion promoter VM652. Application of the adhesion promoter on the substrates is done manually, by use of a very fine syringe. In this way only a small border of 1–2 mm at the edge of the glass substrate is coated with VM652. Alternative ways for depositing the adhesion promoter for large volume processing, include dipcoating the substrates in the

adhesion promoter or dispensing the adhesion promoter by means of an automatic dispenser. After application of the adhesion promoter, the substrates are dried on a hotplate for 1 minute at 120°C.

Once the adhesion promoter is applied selectively and dried on the hotplate, the polyimide can be applied on the glass substrates. Due to handling concerns after release of the flexible package from its rigid carrier, the desired total thickness of the base polyimide layer is approximately 20 μm. As the maximum cured film thickness of a spincoated polyimide PI-2611 layer is only about 10 μm (see Figure 2.2), the base layer has to be built up with several polyimide layers. Preferred single layer thicknesses used for the UTCP technology is always 5 μm, this means that the polyimides are always spincoated at 3000 rpm, so a 20 μm layer will be built up with four 5 μm polyimide layers. The reason for spinning the polyimide always at 3000 rpm is to limit the edge bead, i.e. a local thicker layer of PI at the edge of the substrate after spincoating. The lower the final speed during spincoating, the thicker the final thickness of the spincoated layer, but the more edge bead there will be at the edges of the substrates.

The application of the polyimide is as follows: the polyimide is first dispensed on the substrate, rotated at 500 rpm for 5 seconds (for a good spread of the material on the substrate) and next rotated at 3000 rpm for 45 seconds to reach the final 5 μm layer thickness. Before the application of the next polyimide layer, this first layer is fully cured in a vacuum oven, using the standard cure profile:

- heating from room temperature to 200°C, with a ramp rate of 4°C per minute
- 30 minutes at 200°C
- heating from 200 to 350°C, with a ramp rate of 2,5^{o}C per minute
- 60 minutes at 350°C
- gradual cooling down to room temperature

During the cure of the polyimides, a small N_2 flow rate (5 sccm) is added for a better removal of water and solvents evaporating from the spin-on polyimide.

The next 3 polyimide layers will be applied on this first polyimide layer by repetitive spincoating and drying: a next polyimide can be spincoated immediately on the previous polyimide layer after only a short drying step (15 minutes at 200°C). This hotplate dry step is sufficient to drive off part of the solvents and to harden the liquid polyimide before the spincoating of the next polyimide layer. After repetitive spincoating and drying, all layers will be finally fully cured at once during one curing cycle up to 350°C. This elimates the need for a time consuming curing step per individual polyimide layer.

However, this fast drying can not be applied on the first polyimide layer. A fast hotplate drying results in curling of the polyimide film on the glass carrier after final cure. This could be explained by the difference in CTE between the glass and the polyimide, since the final curing is done up to higher temperatures; and by the different chemical properties of the dried polyimide (compared with a fully cured polyimide layer).

In order to have good adhesion of the next polyimide layer on the first cured polyimide layer, an RIE (Reactive Ion Etching) treatment is needed. Without any pretreatment, a next polyimide layer has bad adhesion on a cured polyimide, resulting in delayering of both films during further processing or handling. This problem has been solved by applying a plasma treatment before the deposition of the next polyimide. Following RIE treatment has been introduced: 2 minutes with a 5 sccm-CHF_3/20 sccm-O_2 gas mixture, followed by 2 minutes 25 sccm oxygen plasma treatment (see Table 2.2). This plasma treatment turned out to be very effective: the polyimide film on the plasma-treated surface maintained strong adhesion for long periods of time in a high-temperature and high-humidity environment. No adhesion problems or delayering occurred during extensive reliability testings, as described in Chapter 3.

CHF_3 [sccm]	**O_2** [sccm]	**Power** [W]	**Pressure** [mTorr]	**Time** [min]
5.0	20.0	150	100	2
0	25.0	150	100	2

Table 2.2: Plasma treatment parameters for improved adhesion between two polyimide films

After RIE, the second polyimide layer can be spincoated with the same parameters as for the first polyimide layer: 5 s at 500 rpm for spreading and 45 s at 3000 rpm for achieving the final 5 μm layer thickness. In between the spincoating of this layer and the application of the next polyimide layer, the sample is dried on a hotplate, with following drying profile:

- start temperature hotplate: 100°C
- heating from 100 to 200°C, with a ramp rate of 3°C per minute
- 15 minutes at 200°C
- cooling down to 100°C

After this drying step, the third polyimide layer can be applied. Next, this third polyimide is dried before the application of the fourth polyimide layer. After spincoating this fourth polyimide layer, these 3 polyimide layers are fully cured during one curing cycle, using the typical polyimide curing profile up to 350°C in a vacuum oven.

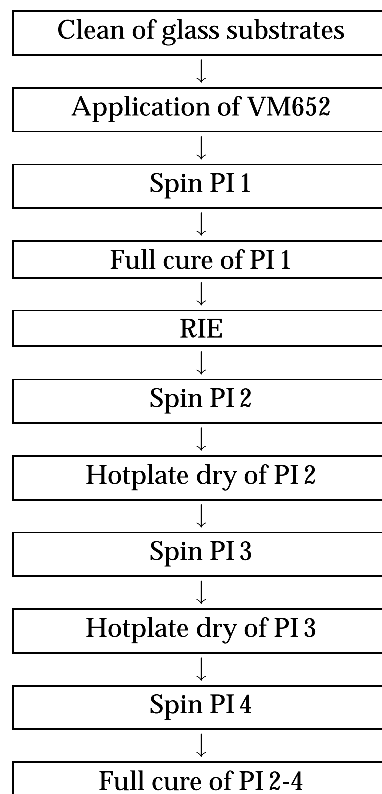


Table 2.3: Overview of different process steps for the base polyimide layer processing

A summarizing overview of all different process steps for the base polyimide layer preparation is given in Table 2.3. The final result is a polyimide layer with total cured film thickness of 20 μm, applied on a rigid glass carrier, which adheres only at the edges of the substrate, but which has enough adhesion to stay on this carrier during the whole UTCP process cycle as shown in figure 2.1.

2.4 Chip placement

2.4.1 Adhesive material

The UTCP technology integrates very thin silicon devices, with thicknesses down to 15 μm, in between two polyimide layers. The ultra-thin chips will be placed face-up on the base polyimide layer, using an adhesive material for the fixation of the dies on the substrate. After placement and fixation of the chips a next cove-

ring polyimide layer will be applied. This implicates that the adhesive material has to be resistant to the high curing temperature of this polyimide (up to 350°C). For this reason only a very limited number of materials can be used as adhesive in the UTCP technology.

Several polymers were already compared for full wafer bonding [7, 8]. In that study, BCB bonding offered the highest bond strengths. Different polymers are also compared in the framework of this PhD for single die bonding: polyimides PI-2610 and PI-2611 (from HD Microsystems) and the BCBs from the Cyclotene 3000 series (Dow [9]). Processing was optimized to realize nice, void free bonding of the ultra-thin devices on the cured polyimide substrates. The experiments and results using these different materials are discussed in the next paragraphs. The polyimides PI-2610 and PI-2611 turned out to be not appropriate as bonding material. The best bonding results were achieved using BCB as bonding material for the UTCP technology.

Polyimide bonding trials

Polyimides PI-2610 and PI-2611, both developed by HD Microsystems, were tested as adhesive material. The polyimide PI-2610 is a diluted version of the PI-2611, with cured layer thicknesses ranging between 1–3 μm, see Figure 2.2. The PI-2610 film thickness can be further reduced by mixing it with Pyralin T9039. This is a dedicated thinner for the Pyralin polyimides, suitable for reducing the viscosity and the solids contents.

Several bonding tests were done using the PI-2610 (both pure as well diluted with the T9039, 1 part PI2610 : 1 part T9039) and the PI-2611. The expected cured film thickness of the 1:1 diluted PI-2610 is about 1/3 of the cured film thickness of the undiluted PI-2610 (spincoated at the same speed). For this bonding trials the bonding polyimides were always spincoated for 5" at 500 rpm + 45" at 3000 rpm.

Bonding experiments were done using (unthinned) Si chips, size: 5 x 5 mm^2. The chips are always placed face-up on the adhesive layer. Placement is done manually, on the base UTCP substrates, i.e. a cured PI-2611 layer on rigid glass carriers.

A lot of different parameter combinations were tested. Experiments both with and without thermode bonding were performed. If the chips are fixed using a thermode, extra pressure and heating can be applied during bonding.

After placement of the dies, the adhesive film was always cured using the conventional curing profile for the polyimides, up to 350°C.

The polyimides PI-2610 and PI-2611 turned out to be not appropriate as bonding material, mainly due to the polyimide curing mechanism. During cure of the polyimide, a lot of water is released as a by-product of the polyimide [2]. This evaporating water and the evaporated solvents create bubbles at the bond interface, between the chip and the polyimide. Also the introduction of an extra pre-

cure step (with precure temperatures ranging from 50, 100 to 200°C) turned out to be insufficient to remove (most of) the evaporating products from the polyimide material and to ensure nice bonding.

A summary of all different parameters is given here:

- choice of bonding polyimide (PI-2611, PI-2610 or diluted PI-2610)
- thermode bonding pressure: none - 2 bar
- temperature during thermode bonding: ranging from room temperature (no heating) up to 400°C
- precure before bonding: none, up to 200°C.

Better results were achieved using BCB as bonding material: BCB has a different curing mechanism and turned out to be more suitable as adhesive for the UTCP technology.

BCB bonding trials

Different BCBs from the Cyclotene 3000 series (Dow) are compared for bonding single chips on the polyimide substrates. There are four formulations from this Cyclotene 3000 which are available: the 3022-35, 3022-46, 3022-57 and the 3022-63. The difference in viscosity and thickness range of these different types of BCBs are shown in Table 2.4.

solution properties	**3022-35**	**3022-46**	**3022-57**	**3022-63**
solvent	mesitylene	mesitylene	mesitylene	mesitylene
viscosity (cSt @ 25°C)	14	52	259	870
thickness range [μm]	1.0–2.4	2.4–5.8	5.7–15.6	9.5–26.0

Table 2.4: Some properties of the different formulations of the BCB Cyclotene 3000 Series (Dow, [10])

It is very important to have a void free bond interface after placement of the chips. Voids can be caused by evaporated water and solvents during the curing (see also the polyimide bonding trials, discussed above), but also by small air bubbles, trapped at the bonding surface during placement of the chip.

During the first bonding trials, the BCB Cyclotene 3022-46 was tested, spincoated on the samples with different spinspeeds, ranging from 1000 rpm up to 4000 rpm (with layer thickness ranging between approximately 5.5 and 2.5 μm [10]). In a second set of experiments, deposition of the BCB was also done by dispensing very small droplets on the substrate where the chip has to be mounted.

This use of a dispensed BCB was preferred above spincoated BCB, because it reduces the risk of having air bubbles trapped at the interface between the device and the substrate. During placement one can allow the drop of BCB to spread and flow, driven by capillary to the edges of the die, and this way preventing air below the fixed chip. An example of an air bubble which was trapped between the interface die/substrate during placement is shown in Figure 2.3. Even very small amounts of air in the adhesive layer can cause large bubbles after the curing up to 350°C.

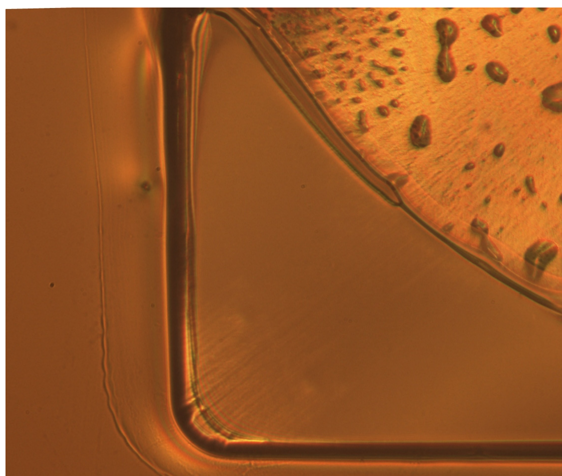


Figure 2.3: Air bubble trapped in the BCB layer between the silicon device and the polyimide substrate (picture taken from the backside of the glass substrate).

The initial idea was to cure the thin BCB layer by heating up the chip locally during placement, with the thermode. Different parameter combinations were tested for curing the BCB during the placement, similar to the polyimide bonding trials. These curing trials were not very satisfying: when applying the next polyimide layer on this 'dried' BCB layer a chemical reaction of the spincoated polyimide with the BCB was always visible. This is because the BCB is not fully cured: it has to be cured following a temperature profile with slow ramp rates to ensure hard cure of the BCB and to ensure nice material properties of the cured layer.

Since we were not able to program slow ramp rates with our thermode and a full cure of the BCB would also be too time consuming, the devices are now placed on BCB without heating by means of thermode. After placement, the BCB is fully cured in a vacuum oven. The normal curing temperature of BCB is 250°C, but as the top polyimide layer will be cured at 350°C also the BCB is cured at 350°C. Following curing profile is used:

- heating from room temperature to 200°C, with a ramp rate of 5°C per minute
- 20 minutes at 150°C
- heating from 150°C to 250°C, with a ramp rate of 1,6°C per minute
- 60 minutes at 250°C
- heating from 250°C to 350°C, with a ramp rate of 2,5°C per minute
- 60 minutes at 350°C
- gradual cooling down to room temperature.

This curing profile is the combination of the normal curing profile of BCB up to 250°C, and the curing profile of polyimide from 250°C up to 350°C. This way further outgassing of BCB during the next polyimide curing step up to 350°C is prevented. During the cure of the BCB, a small N_2 flow rate (5 sccm) is added for a better removal of water and solvents evaporating from the spin-on polyimide.

Also BCBs with different viscosities were tested for optimization of the placement: the Cyclotene 3022-35, 3022-46 and the 3022-63 were compared. Best placement results were achieved using the Cyclotene 3022-46 (with a viscosity of 52 cSt @ 25°C). The viscosity of the 3022-35 was too low to keep the die fixed at its position and to limit the displacement of the devices during the substrate handling after die placement. The higher viscosity of the 3022-63 slows down the capillary flow of the adhesive to the edges of the devices and would result in an unnecessary increase in final BCB layer thickness.

2.4.2 Chip placement

During chip placement, it is crucial to prevent air trapped in the BCB adhesive layer: even very small amounts of air at the interface between the polyimide and the die can result in very large bubbles after the curing of the BCB up to 350°C. These voids in the BCB layer can be prevented by allowing the BCB to flow, driven by capillary forces, to the edges of the die, ensuring a nice voidfree bond. Chip and substrate have to be brought in contact in a well controlled matter. So the BCB can have the time to spread to the edges of the chip.

Since there was no suitable bonding tool available at CMST for the handling and mounting of ultra thin devices, placement of the thin dies was done in an alternative way: by making use of the aligner. The thin dies are placed face down, on the substrate holder (where normally the substrates to be illuminated are placed) and the UTCP substrate (polyimide on glass), with a small dispensed droplet of BCB dispensed on it, is vacuum fixed on a dedicated mask: this plastic mask, regular illumination mask size, has a connection to the vacuum system and is fixed

in the aligner mask holder. Next, the mask holder (+ UTCP substrate) is brought in parallel with the chip. After alignment of the droplet of BCB on the backside of the die, the mask holder is lowered until the chip and the BCB are in contact. Once contact between the silicon and the BCB is established, the BCB flows automatically to the edges of the die, driven by capillary forces, ensuring a nice, void free bond.

Of course this method for mounting the thin dies has to be further optimized. At the time of writing this thesis, a new Dr. Tresky AG die bonder is installed in the lab. Using this bonder it will be possible to handle the extremely thin silicon devices (with dedicated vacuum head for handling and picking up ultra thin devices), to dispense the BCB precisely on the substrates and to ensure accurate pick and placement of the chip on this BCB. Also the deposition speed can be well controlled in order to allow the BCB flowing to the edges of the dies. Parallel placement with the bonder will also limit the possible thickness variation of the BCB thickness all over the device.

2.5 Top polyimide

Once the die is fixed on the base polyimide layer, using BCB as adhesive material, a covering PI-2611 spin-on polyimide layer is spincoated on top of the chip in the next step. This top polyimide has to adhere well on different surfaces:

- the cured base polyimide layer
- the cured BCB material
- the surface of the die.

Without any pretreatment, polyimide has a very poor adhesion on all 3 of these surfaces.

The adhesion of a next polyimide layer on a cured polyimide layer and on the cured BCB is improved by a combined RIE (Reactive Ion Etching) treatment, first 2 minutes with a 5 sccm $CHF_3/20$ sccm O_2 gas mixture, followed by a 2 minutes 25 sccm oxygen plasma; both applied with a power of 150 W and a pressure of 100 mTorr.

A good adhesion of the spin-on polyimide on the surface of the chip can be achieved by the application of a dedicated adhesion promoter, the VM652 from HD Microsystems. VM652 is dispensed on the sample and spin dried for 30 seconds at 3000 rpm. Next, the sample is baked on a hotplate for 60 seconds at 120^oC.

After the RIE treatment and the application of the adhesion promoter, the top polyimide is spincoated and cured in a similar way as the base polyimide layer:

starting with the spincoating and full cure of the first polyimide layer, followed by a repetitive spincoating and drying for the next 3 polyimide layers, see Table 2.3. Finally also these polyimide layers are full cured up to 350°C.

The layer thickness is chosen to be the same as for the base polyimide (also four layers of about 5 μm are spincoated), to ensure a nice edge coverage of the embedded die. Since polyimide is not a planarizing material (it follows the shape of the die), a sufficient thickness of polyimide is required to ensure a smoother step at the edge of the die. This is an important issue during the lithography step for patterning the metal layer.

Figure 2.4 shows a cross sectional view of a test chip embedded in between these two PI layers. The test chip has a thickness of 15–16 μm, the thickness BCB is only 2 μm. Note that the polyimide thickness on top of the chip is slightly less than 20 μm on top of the chip, although four layers of 5 μm were applied.

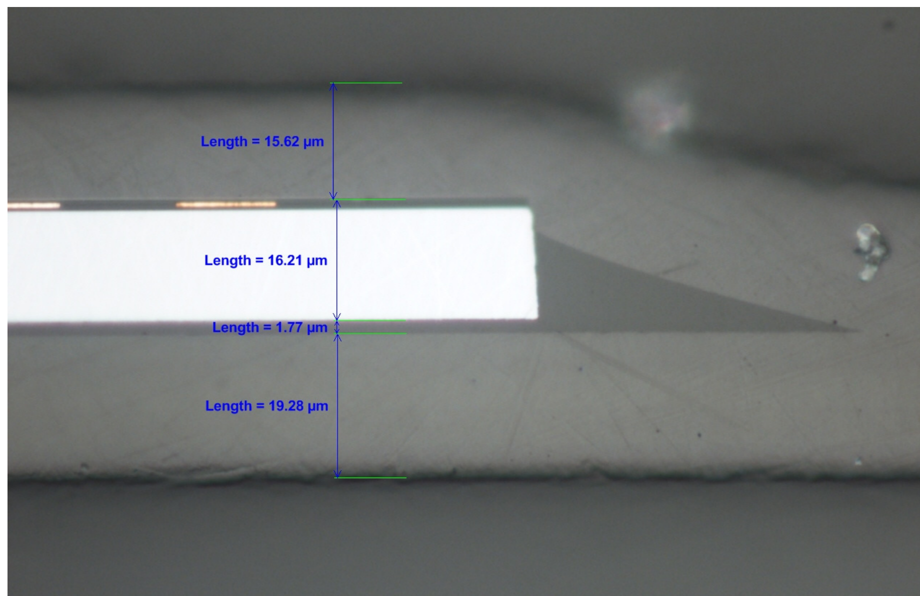


Figure 2.4: Cross section of embedded test chips, top metallization not visible

2.6 Via technology

2.6.1 Introduction

Once the chip is embedded in between the two polyimide layers, vias have to be drilled to the contact pads of the chip. This section deals with the different microvia drilling technologies developed for the UTCP technology. The contacts can be opened either by laser drilling or by dry etching. Laser drilling has emerged as a widely accepted method for creating microvias in high-density electronic interconnect and chip packaging devices. Different laser ablation based technologies were developed for the UTCP technology and are discussed in this section. The last part of this section presents also some feasibility results for dry etching of microvias using Reactive Ion Etching.

Via resistance measurements for each of these different via opening technologies will be discussed in Chapter 3, since metallization for the UTCP technology will be discussed first in a next session.

2.6.2 Laser ablation set-up

This section gives a short description of the laser ablation set-up available at CMST. A more extended explanation and more fundamentals about polymer material laser ablation are already given by Van Steenberge in [11]. The set-up as installed in our lab is shown in Figure 2.5. In this custom-built ablation set-up [12], three different laser sources are integrated in one system: a KrF excimer laser, a frequency tripled Nd-YAG laser and a CO_2 laser.

This set-up is used at CMST for structuring a whole set of materials for opto-electronic and micro-electronic applications. Typical optical applications are terminating optical fibers and structuring optical interconnections [13, 14, 15]. Typical micro-electronic applications are: photoresist structuring, using laser direct writing, and microvia drilling for both flex as rigid boards. Microvia drilling for FR4 based multilevel PCBs is studied within the framework of the European-Hiding Dies-project (HIgh Density INteGration of Dies Into Electronics Substrates) [16, 17]. The microvia drilling in polyimide based flex substrates is presented in this dissertation. Recent activities study also the laser patterning of thin layers for OLED applications. This work is done in the framework of the European-Fast2Light-project [18].

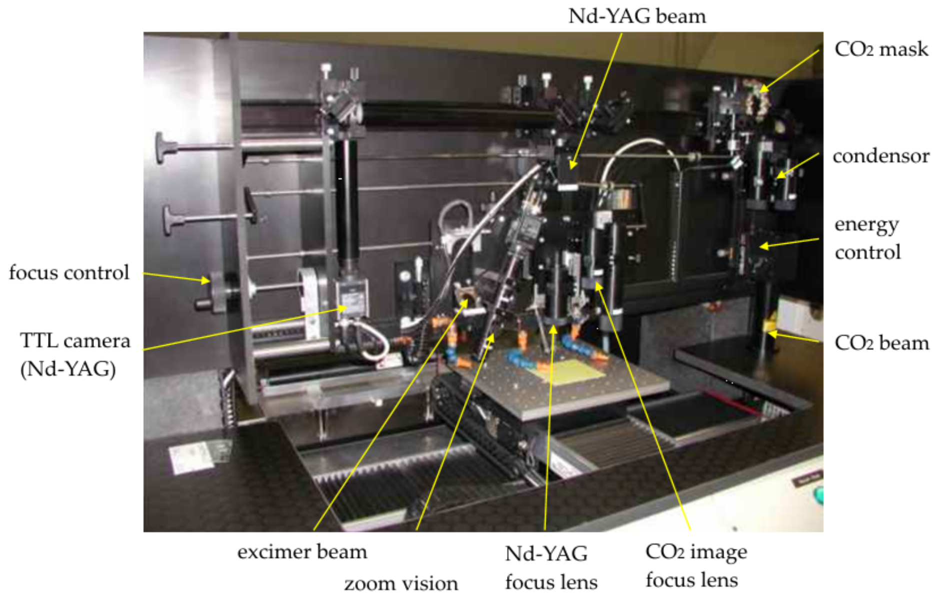


Figure 2.5: Laser set-up

Table 2.5 gives an overview of the properties of the three different lasers.

laser type	CO_2 GSIL Impact SSM 2150	freq. tripled Nd-YAG LWE 210-355-5000	KrF excimer ATL SP300i
wavelength	10.6 μm	355 nm	248nm
max. optical power	60 W	5 W	6 W
max. pulse energy	0.4 J	500 μJ	20mJ
max. pulse freq.	150 Hz	10–100 kHz	300 Hz
pulse length	70 nsec	35 nsec	3–7 nsec

Table 2.5: Properties of the different lasers

UV lasers, like the excimer and the frequency tripled Nd-YAG laser, are known for high-precision material removal and their ability to drill the smallest vias [19]. But the UV lasers have also the ability to effectively ablate metal layers, this means that measures must be taken to avoid too much laser damage to the metallization of the bumps of the chip.

Most of the metal layers reflect the incident IR light of the CO_2 laser beam and are not affected by the CO_2 laser, but CO_2 lasers have typically a much larger spot size, which makes it difficult to realize small microvias.

As the chips are embedded in polyimide, vias have to be drilled through this polyimide layer with thickness of about 15–20 μm. All processing is optimized on test chips with contact pitch of 100 μm and pad size of 70 μm, implicating a targeted maximum via diameter of about 50 μm. The contact pads on the die are finished with 5 μm NiAu, so laser ablation has to stop on this thin metal layer in order not to damage the contact pad.

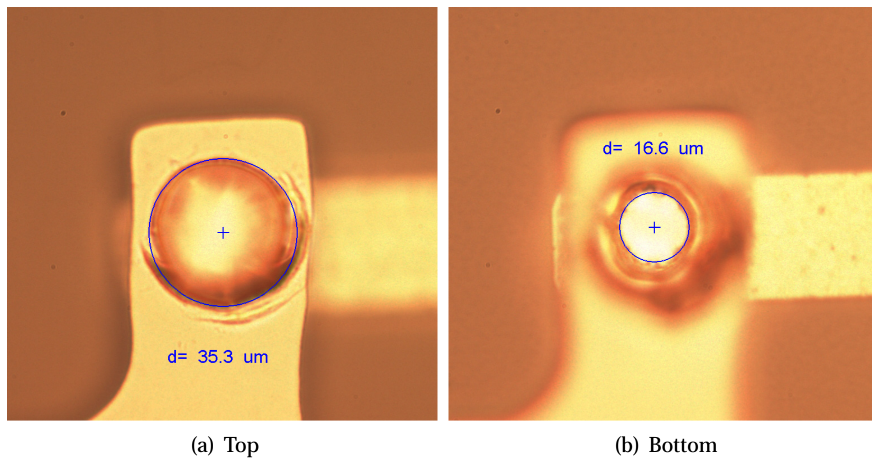
2.6.3 Frequency tripled Nd-YAG laser based via drilling

The first laser drilling tests were performed using the frequency tripled Nd-YAG-laser, working at 355 nm. With the YAG laser it is challenging to stop on a very thin metal layer, as the YAG-laser has a Gaussian beam intensity profile. This means that the beam has a high power in the center of the beam. This makes it very difficult to prevent metal damage at the center of the via, especially for thicker top polyimide layers: the thicker the layer, the more power needed to remove enough material through-out the via, but the more damage introduced in the underlying material at the center of the via. The 15-20 μm top polyimide layer turned out to be too thick: the process window between the power needed to ensure sufficient polyimide removal in the via and the maximum power which a 5 μm NiAu chip bump can withstand is too small.

A possible solution to reduce this metal damage in the centre of the via could be the use of the YAG out of focus. This is no option; because a precise out of focus regulation is not available in our set-up.

Another interesting solution is the use of the tripled YAG-laser with a shaped beam profile: beam-shaping optics can transform the natural Gaussian irradiance profile to a near-uniform 'tophat' profile. This imaged beam removes the polyimide material more uniformly across the via, without creating undesirable underlying metal damage at the centre of the imaged spot (which is difficult to control with a Gaussian beam). It is also shown that a substantially lower irradiance dose is required for drilling when using this reshaped beam profile. A lower irradiance dose reduces considerably the thermal load on the material and improves dramatically the overall hole quality (and reduces the debris). Due to the uniform profile of the beam also the tapering can be better controlled [20].

Via diameters with a top diameter down to 35 μm were realized using the tripled YAG laser with shaped beam. Figure 2.6 shows top and bottom diameter of a metallized via, Table 2.6 gives the optimized parameter settings for this laser drilling technology.



(a) Top (b) Bottom

Figure 2.6: Metallized via to a contact of an embedded test chip, drilled with shaped beam YAG laser

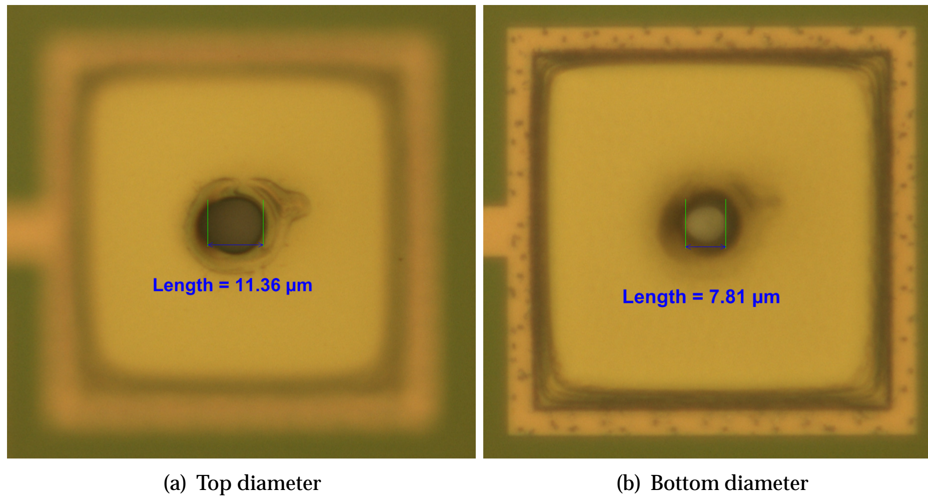
frequency	number of pulses	mask	demagnification	fluence
10 kHz	300	circular diam.: 200 μm	10	3.129 J/cm^2

Table 2.6: Parameters for shaped beam YAG via drilling technology

The settings of the beam shaping optics in our set-up turned out to be unstable, and recalibrating these settings every time made it very time consuming to reproduce the results in next experiments.

An alternative for preventing or reducing the contact pad damage was found in thinning down the top polyimide film before laser ablation. If the PI is thinned down to a thickness of about 5 μm, YAG laser with the Gaussian beam intensity profile can be used: this way the polyimide is thin enough to ensure sufficient polyimide removal without undesirable contact pad damage. As was shown in the cross section of Figure 2.4 the layer thickness on top of the chip is around 15 μm. This layer is first thinned down to approximately 5 μm of thickness by removing 10 μm of this top polyimide by RIE. Parameters for this RIE etch are: 23 minutes in a 5 sccm CHF_3/20 sccm O_2 gas mixture, applied with a power of 150 W and a pressure of 100 mTorr.

Figure 2.7 gives a detailed view of top and bottom of a YAG laser drilled via through this thin polyimide layer: the via has a top diameter of 11.4 μm and bottom diameter of 7.8 μm. Damage introduced to the NiAu finish is reduced since only 5 μm had to be removed.



(a) Top diameter (b) Bottom diameter

Figure 2.7: Top and bottom via diameter of a YAG laser drilled via through a 5 μm thin polyimide layer

As via dimensions are so small 3 x 3 via matrices are drilled to the 70 x 70 μm^2 (100 μm pitch) contact pads of the embedded interconnection test chip, see Figure 2.8.

Figure 2.9 shows a more detailed view of the top and bottom for a 3 x 3 matrix of YAG laser drilled vias. Parameters for this laser drilling are given in Table 2.7. These parameters for drilling microvias through thin PI layers were optimized in the framework of the PhD work of Jonathan Govaerts, see also [21]. Per contact pad nine (small) via holes are drilled instead of one to increase contact area between chip bump and metallization layer.

freq.	number of pulses	mask	demagn.	fluence
10 kHz	100	circular diam.: 200 μm	10	6.1 J/cm^2

Table 2.7: Parameters for YAG via technology (with Gaussian beam) for drilling through a 5 μm thin polyimide layer

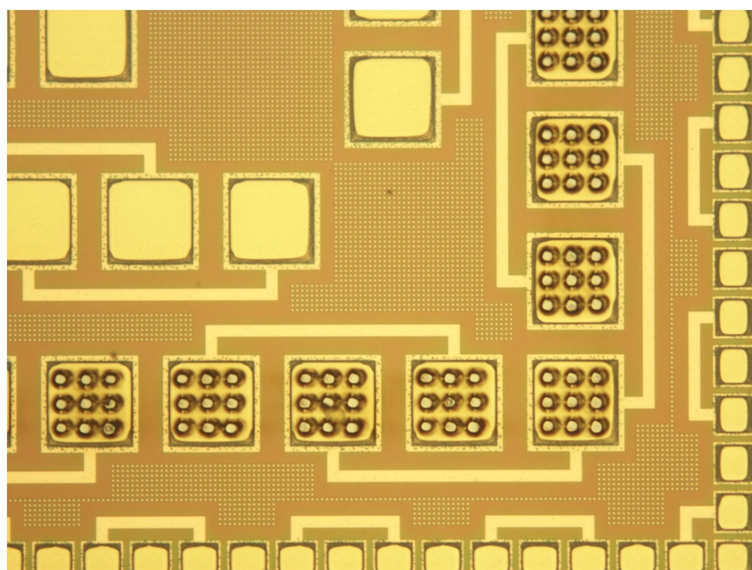
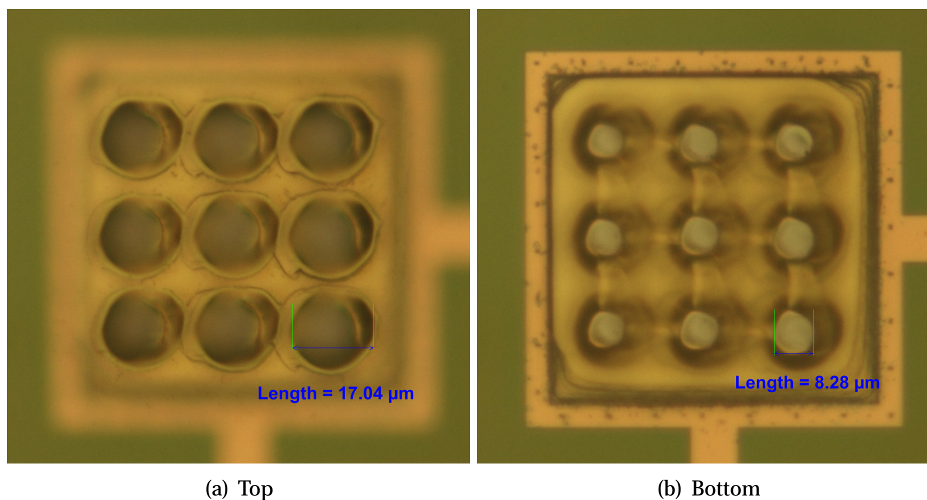


Figure 2.8: 3 x 3 matrices of YAG laser drilled vias to the contact pads at the corner of the embedded interconnection test chip



(a) Top (b) Bottom

Figure 2.9: Detailed view on matrix of small vias drilled with the YAG laser after thinning down the top polyimide layer

2.6.4 CO_2 laser based via drilling

An alternative and preferred via technology for the UTCP is based on CO_2 laser ablation. The advantage of CO_2 laser ablation for the UTCP application is that the CO_2 laser beam is not easily absorbed by metal. Most of the metal layers reflect the incident IR light of the CO_2 laser beam and are not affected. This way a metal layer, like the contact pads of the embedded die, can act as a laser stop. Via ablation down to the contact pad can hereby be accomplished without damaging the contact pad material. The disadvantage of this technology is that the minimum feasible via size is too large due to the larger wavelength of the CO_2 laser light and the diffraction at the used optics: minimum via diameters drilled in polyimide are about 80 μm. This means that the CO_2 laser is not so suitable as such, especially if we want to develop the UTCP technology for chips with fine pitch contact pads. Therefore the CO_2 laser has to be used in combination with a metal via etch mask. A metal layer can first be sputtered on the polyimide package before the CO_2 laser ablation. Cu is a suitable material for this, because Cu reflects the IR light of the CO_2 laser (much more for example than Al). Small via openings are etched in the sputtered metal mask after photolithographic patterning and the polyimide can be removed by the CO_2 laser through these small via openings.

A TiW Cu layer is sputtered on the polyimide package as via mask. Because the spincoated polyimide follows nicely the shape of the chip, also the contact pads are visible even through the sputtered metal layer. This way there is no need for extra alignment marks for the next lithography step. The litho mask can be aligned directly on the contact pads. We use a thin photoresist for this lithographic step: S1818 (Rohm and Haas), spun at 4000 rpm with final thickness of 1.8 μm. Alignment is done through the small 40 x 40 μm^2 openings of a dedicated photolithographic mask, fitting the contact pad pattern on the interconnection test chips. After lithography, the Cu is etched in a $FeCl_3$ based etchant and the TiW is etched for about 10 seconds in a hot 30% H_2O_2 solution (50°C), followed by a 10 seconds etch in a cold 30% H_2O_2 solution. Figure 2.10 (a) shows the result after patterning the via metal mask (note that all the bumps of the chip are clearly visible through the sputtered metal layer). The dimensions of the via openings in the mask after etching are about 50 x 50 μm^2.

freq.	speed	mask	# pulses	demagn.	fluence
100 Hz	5 mm/s	circular diam.: 2000 μm	40 (2 times)	4.56	3.8 mJ/cm^2

Table 2.8: Parameters for removing the polyimide material through the metal via etch mask by CO_2 laser drilling (the via are screened two times using these parameters)

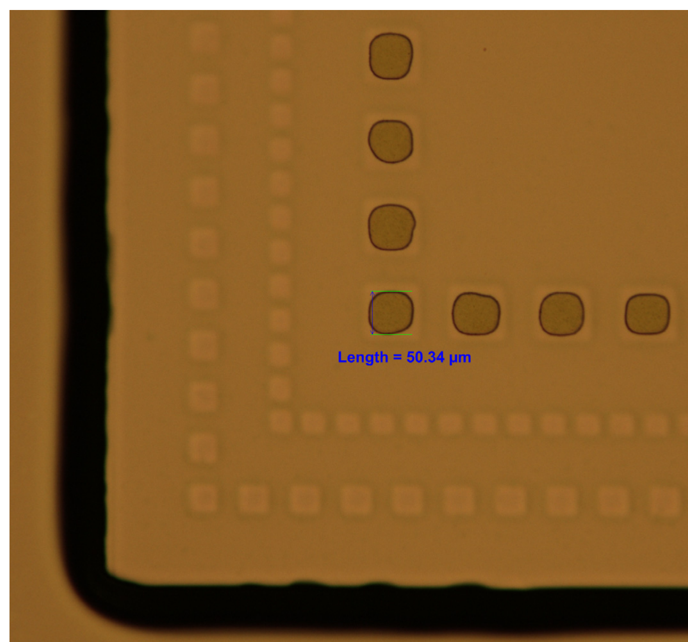
After metal mask etch and strip of the photoresist, the polyimide can be removed by the CO_2 laser ablation through the small via openings, the result is shown in Figure 2.10 (b). The optimized parameters for the CO_2 laser ablation are given in Table 2.8. The polyimide throughout the via is removed during a double screen by the CO_2 laser, with a speed of 5 mm/s.

Figure 2.11 gives a more detailed view of the metal mask and the bottom of the via after CO_2 laser ablation. A lot of debris is formed during laser drilling and deposited on the Cu metal mask. The Cu metal mask is also affected by the heat during CO_2 laser ablation.

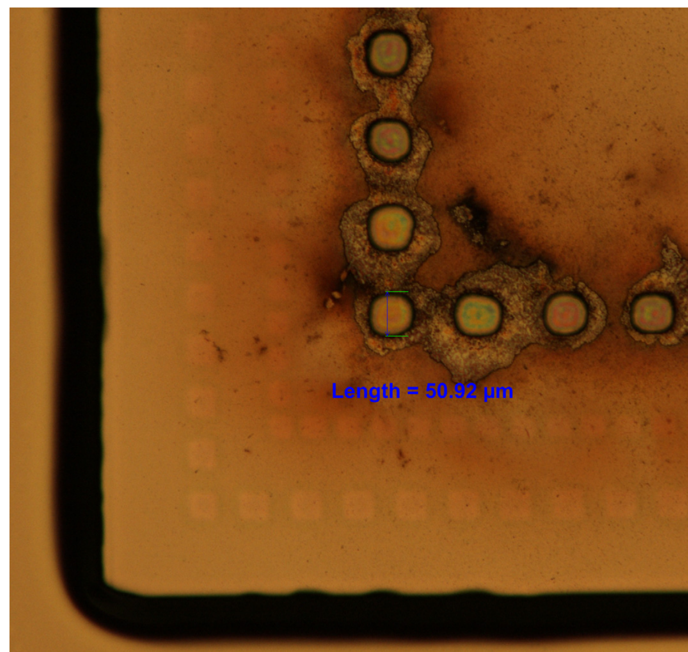
After CO2 laser drilling, a very thin residual polyimide film is observed at the bottom of the via, preventing electrical contacting to the chip pads. This is a well-known phenomenon for (CO_2) laser structuring films with thickness $<$ lambda/4n, and originates from interference between the incident laser beam and the reflected beam. As a result of this interference, the intensity at the surface becomes too low for material removal [22].

In general three methods can be applied for removing this thin residual layer (together with re-deposited particles): by an ultraviolet laser, by plasma etching, or by using chemical etching. The last method being applied in industrial PCB processes, where during laser drilling resin becomes heated resulting in the melting and smearing of the epoxy-resin base material across the inner-layer copper surfaces within the hole barrel to which subsequent through-hole plating must connect. If not corrected, the smear would constitute a dielectric layer between the inner-layer copper surfaces and the plated copper and the circuit would be defective. Industrial PCB processes rely on the use of strong chemical oxidizing agents. While this was historically approached via conditioning and oxidation with aggressive chromic and sulphuric acid chemistries, the conventionally accepted approach for common laminate types is now one combining solvent swell, alkaline permagnate oxidation and neutralization in a three stage integrated process.

Within this work, aggressive chemical etching is not used, but the other two methods are investigated: both UV laser cleaning and plasma cleaning.

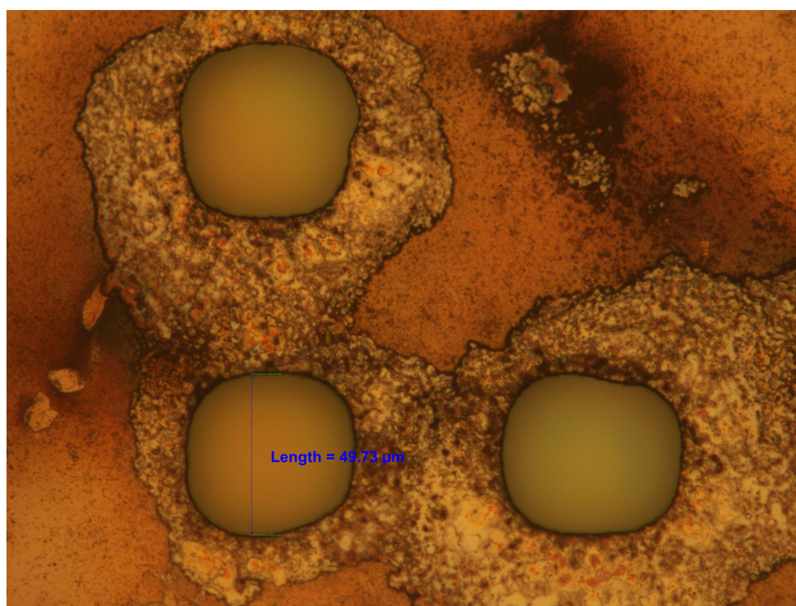


(a) Patterned via etch mask

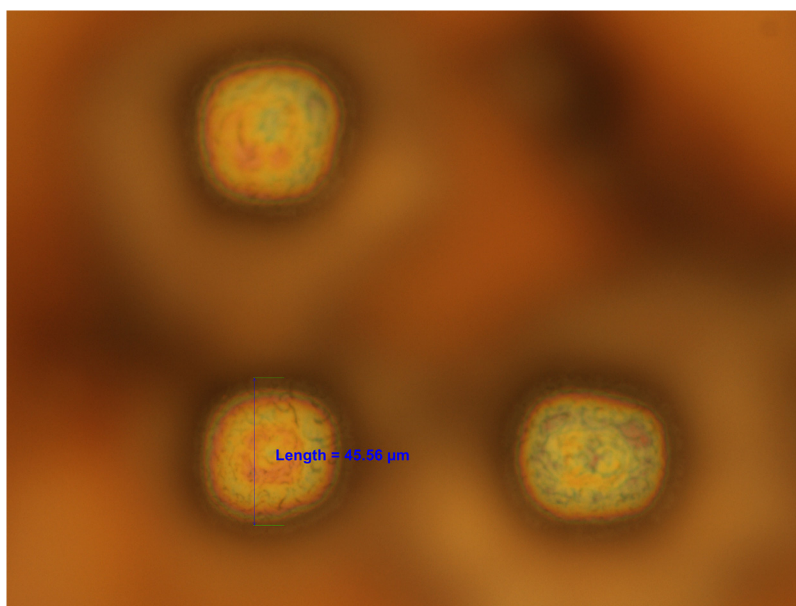


(b) Result after laser drilling

Figure 2.10: CO_2 laser drilling of the polyimide through the metal mask



(a) Metal mask



(b) Bottom of via

Figure 2.11: Detailed view of metal etch mask and bottom of the via after CO_2 laser ablation

Excimer cleaning step

A first possibility to remove this thin residual polyimide film on top of the contact pads of the embedded chips is the use of an UV laser. Since this residual polyimide layer is very thin, only low power is needed to remove this layer and only limited damage will be introduced to the contact pad metal.

With this extra clean step, the thin PI film is removed by the KrF excimer laser. During excimer laser ablation also chemical effects occur: these break the chemical bondings of the residual polyimide material on the pads. This way the residual thin film can be removed from the contact pads. Table 2.9 gives an overview of the different process steps for this combined CO_2 and excimer laser ablation technology.

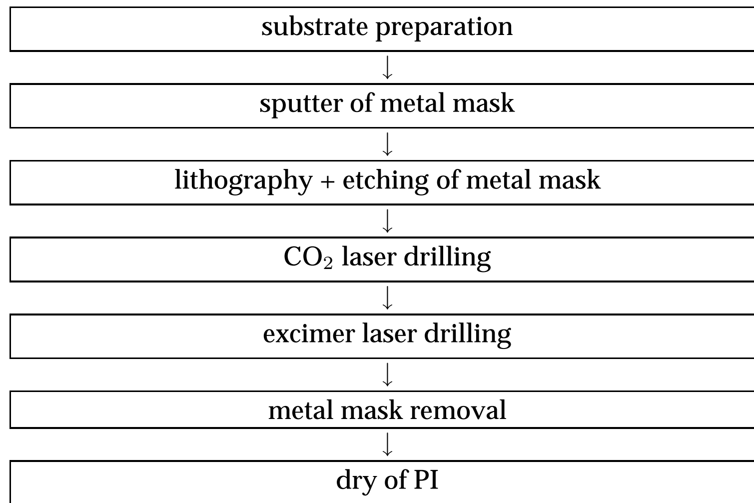


Table 2.9: Process flow for via ablation by combination of CO_2 and excimer laser ablation

The parameters for the KrF excimer laser ablation are shown in Table 2.10. The vias are scanned with the excimer laser at 10 mm/s, resulting in about 4 pulses per via.

freq.	mask	speed	# pulses	demagn.	fluence
140 Hz	3000 x 3000 μm^2	10 mm/s	4	7	0.490 J/cm^2

Table 2.10: Optimized parameters for removing the thin residual polyimide layer on the chip contact pads, through the metal via etch mask, by excimer laser drilling technology

The metal via mask has of course to withstand this excimer laser ablation step: 1 μm Cu thickness turned out to be insufficient, therefore 2 μm Cu is sputtered. Figure 2.12 shows the difference before and after excimer laser ablation: the vias in the left part of this figure had only CO_2 laser ablation, the thin residual polyimide film is visible at the bottom of the via. The vias in the right part of Figure 2.12 had an extra excimer clean. (Remark: Figure 2.12 gives also an impression of the amount of debris deposited mainly during CO_2 laser ablation, excimer laser removed the debris close to the via openings.)

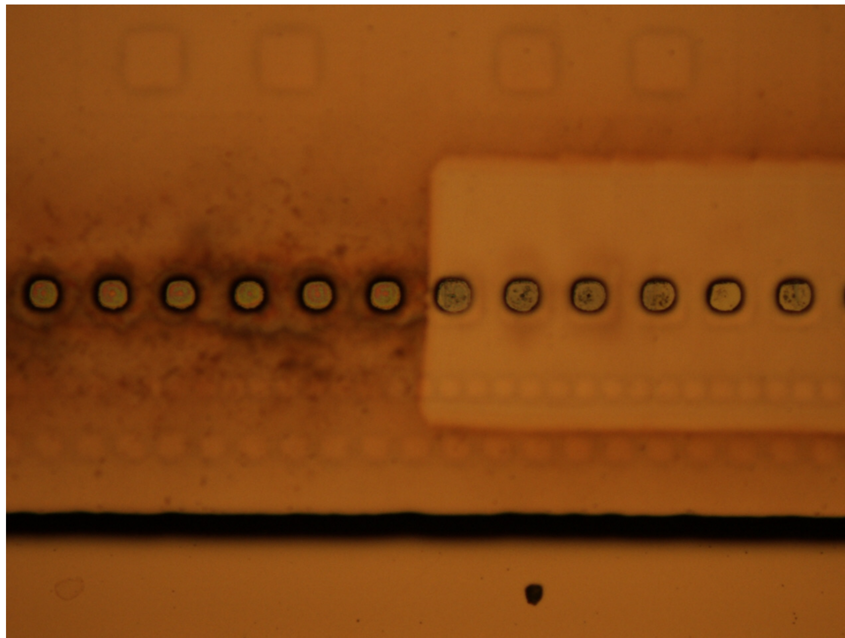
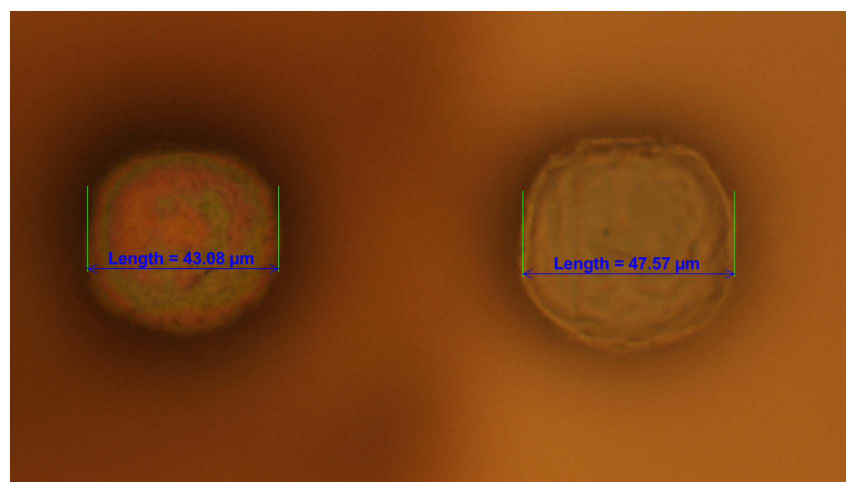
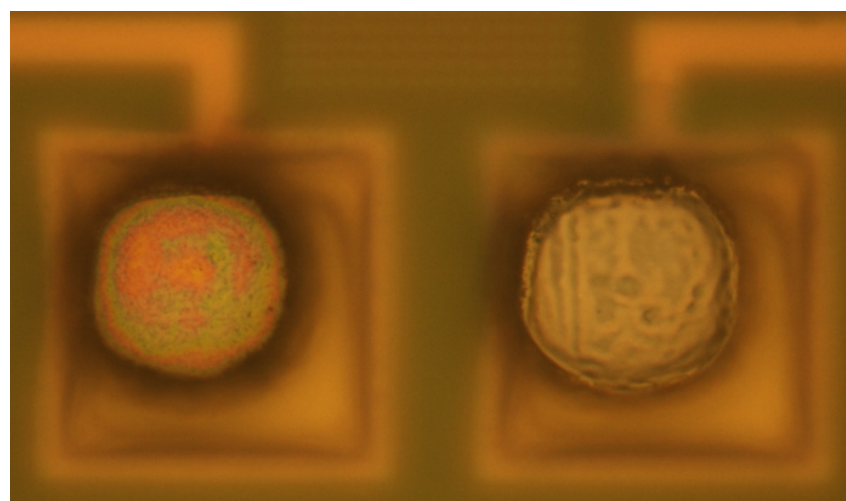


Figure 2.12: Difference before and after excimer laser clean step

After laser drilling the metal mask is removed: the Cu layer is etched in $FeCl_3$ solution and the TiW layer in the H_2O_2 solution. By etching the metal mask also all possible debris is removed from the surface. Figure 2.13 shows a more detailed view of the vias before and after metal mask etching: the left via has still a very thin residual polyimide on its contact, the film at the bottom of the right via was removed by an extra excimer clean step. (Size of the contact pads in this picture is 70 x 70 μm^2, bottom diameter of the vias is about 45 μm, and the contact pitch is 100 μm.) This picture shows also the damage introduced by the excimer laser at the contact pad metallization. The NiAu is affected, but can withstand this excimer laser drilling because only limited power is needed to remove the very thin residual film.



(a) Before metal mask etch



(b) After metal mask etch

Figure 2.13: Detailed view of bottom of 2 vias, after CO_2 laser drilling only (left via) and after an extra excimer laser clean step (right via)

RIE cleaning step

An alternative technology is a combination of CO_2 laser ablation followed by a RIE etch step. The process flow is shown in Table 2.11.

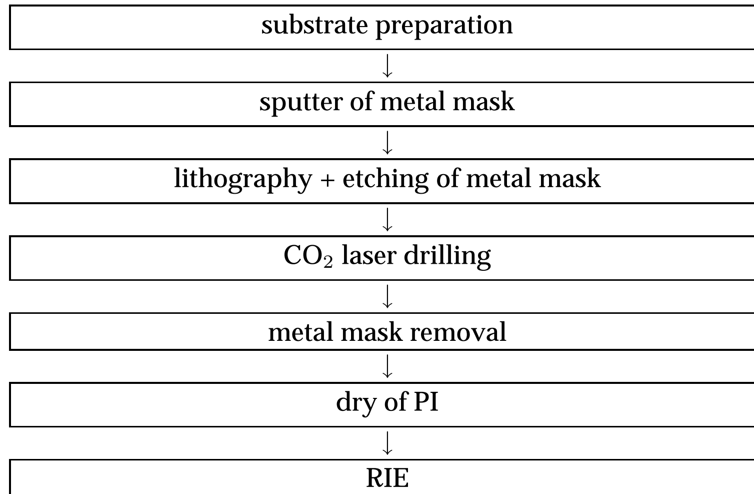


Table 2.11: Process flow for via ablation by CO_2 laser ablation combined with a RIE clean step

Since only a very thin polyimide layer is left at the bottom of the via, this can be removed by a short RIE step after laser drilling. The TiW/Cu etch mask is removed after CO_2 laser drilling, before the RIE step. The Cu is etched completely in a $FeCl_3$ based etchant and the TiW can be removed in 30% H_2O_2 solution (at 50°C). To enhance the removal of the metal etch mask, most of this debris can first be removed by rinsing the substrates in acetone, or even ultrasonic agitation (USA) in acetone, before etching the TiW/Cu mask away. Debris, deposited on the surface of the Cu during the CO_2 laser drilling, can act as an etch mask during the metal mask removal. An example of bad etching due to the debris is shown in Figure 2.14. This can also be removed by longer etching times: this way the dirt from debris on the surface can be underetched and ’lifted off’ from the surface.

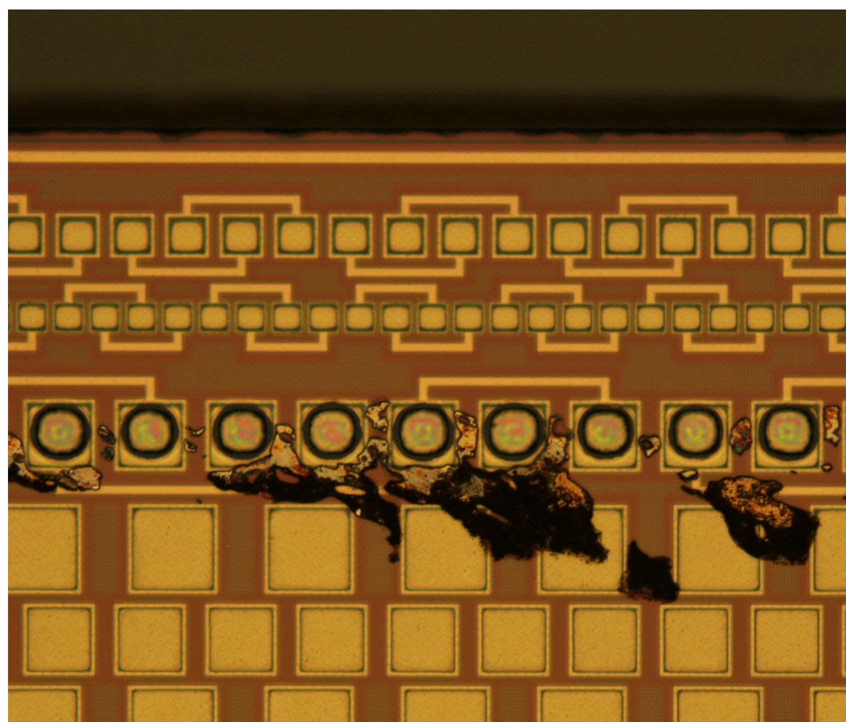
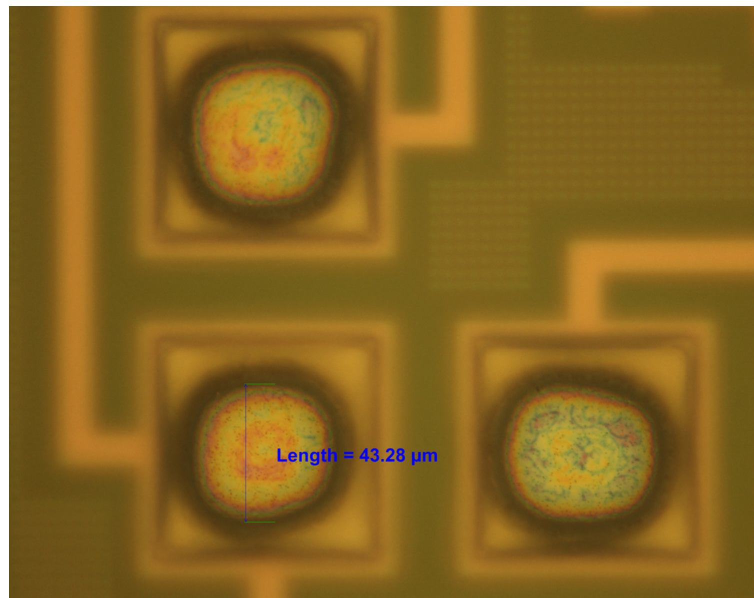


Figure 2.14: Debris, deposited during laser drilling on the metal mask, can prevent etching during metal mask removal

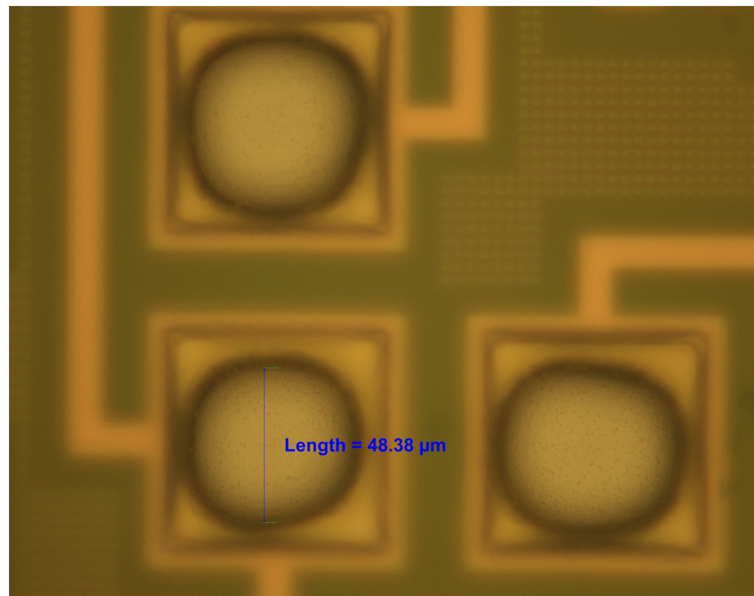
After stripping of the metal masks, the thin polyimide film is removed by a 10 min RIE step. The PI is dried before RIE (for 2 h 30 min at 150°C in a vacuum oven) to remove the water absorbed by the PI. Parameters for the RIE are shown in Table 2.12. A detailed picture of a via before and after the RIE etching step is shown in Figure 2.15.

CHF_3	O_2	Power	Pressure	Time
5.0 sccm	20.0 sccm	150 W	100 mTorr	10 min

Table 2.12: RIE parameters for residual polyimide layer removal



(a) Before RIE



(b) After RIE

Figure 2.15: Removal of the residual thin polyimide film at the bottom of a via by a RIE clean step

Figure 2.16 shows the difference in contact pad metal damage between a via realized by CO_2 laser ablation combined with a RIE cleaning step and a realized via with the combined CO_2 and excimer laser ablation technology.

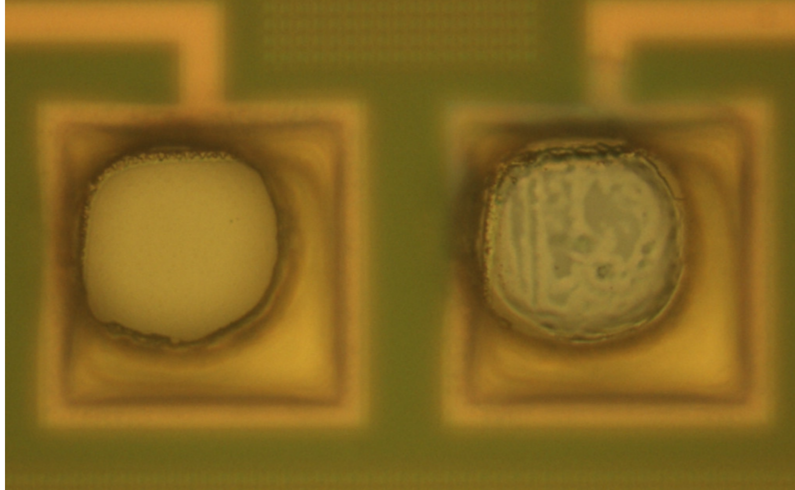


Figure 2.16: Comparison of contact pad metal damage after via drilling: the left via is realized by CO_2 laser ablation combined with a RIE clean step, the right via with the combined CO_2 and excimer laser ablation (for a picture of the same vias before RIE, see Figure 2.13)

This CO_2 laser ablation, combined with a RIE cleaning step, is the preferred via technology for the UTCP package. This technology prevents any contact pad damage to the NiAu metallization of the bumps, compared with YAG and excimer laser ablation processes. This technology also eliminates the use of a second laser (compared with the combined CO_2 and excimer laser technology). Note that the 'extra' RIE step in this technology is only an extended RIE treatment which is needed anyhow before the application of the top metal. This is discussed in the section on the metallization of the UTCP package below.

This via technology is also the technology used for the production of all test samples which are characterized in Chapter 3.

2.6.5 Dry etch of polyimide

Also the feasibility for dry etching of the vias in the polyimide layer has been studied. Based on experiments for dry etch of polyimide in the past, etch rates of the PI-2611 were characterized for the RIE using a mixed CHF_3/O_2 plasma. The parameters are shown in Table 2.13. Typical material removal rates on full polyimide layers are about 0.4 μm/minute.

CHF_3 [sccm]	O_2 [sccm]	Power [W]	Pressure [mTorr]	Time [min]	Material removal [μm]
5.0	20.0	150	100	15	7
5.0	20.0	150	100	30	11.5
5.0	20.0	150	100	45	18+/-2

Table 2.13: Dry etch of polyimide PI-2611

The same parameters were also tested for dry etching of the polyimide through a metal via mask. Al is a suitable material for the dry etch mask, since Al is not attacked by this plasma.

First an Al etch mask was sputtered on the polyimide layer and photolithographically patterned. During lithography, a dedicated illumination mask with small 40 x 40 μm^2 via openings, fitting the contact pad pattern on the interconnection test chips, is used for patterning. According to the etch rates of 0.4 μm per minute, expected dry etch time for this +/- 15–16 μm polyimide removal through this mask would be around 40 minutes.

Figure 2.17 shows the etched Al via mask. An RIE treatment of 45 minutes was applied on this sample. Figure 2.18 shows: (a) the bottom of the via after this 45 min RIE treatment and (b) the bottom of the same via after another 15 minutes RIE treatment: no change is visible, indicating all polyimide was already removed during the first 45 minutes. Figure 2.19 gives a 3D image, and Figure 2.20 the profile of these dry etched vias, both measured using a non-contact optical profiler (Wyko NT3300). The diameter of the vias is 50 μm and about 15 μm of PI was removed through the metal mask (the measured depth of the via includes also the Al layer thickness).

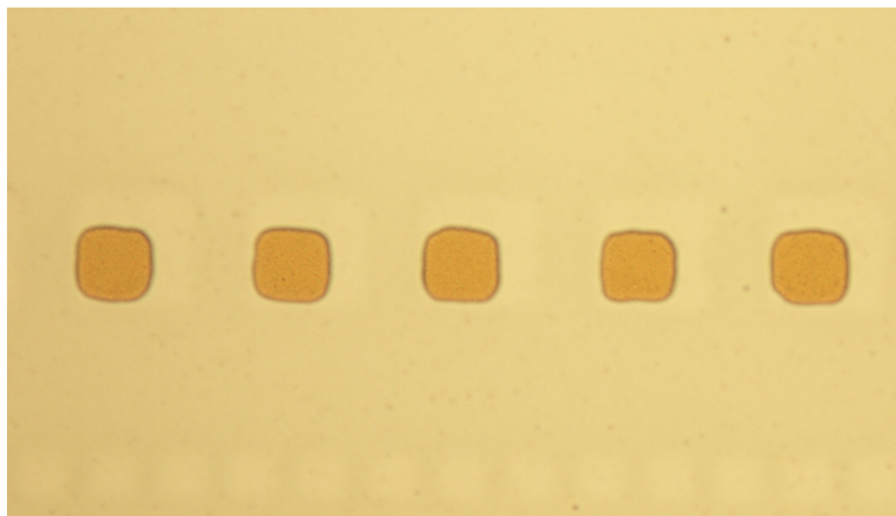
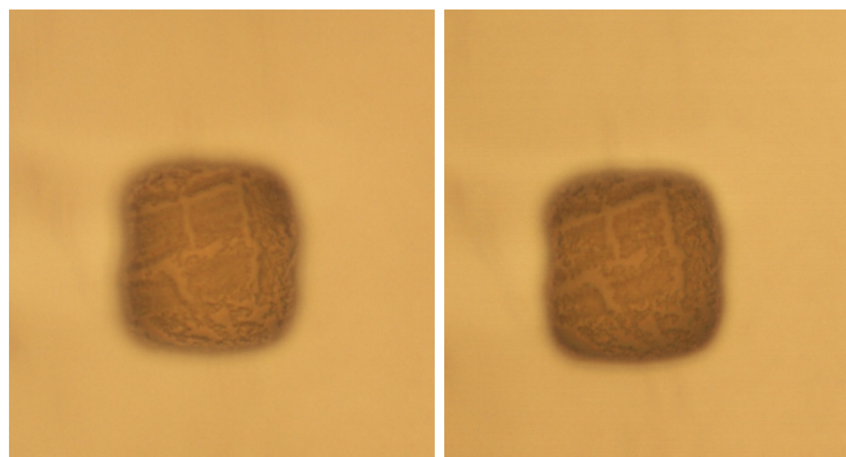


Figure 2.17: Al via etch mask, with 40 x 40 μm^2 via openings



(a) After 45 minutes (b) After 45 + 15 minutes

Figure 2.18: Bottom of via after RIE

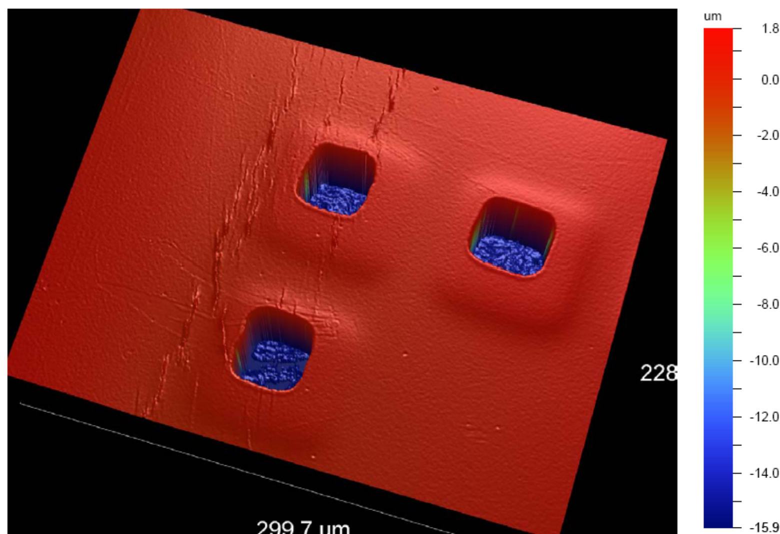


Figure 2.19: 3D image of dry etched vias through Al etch mask

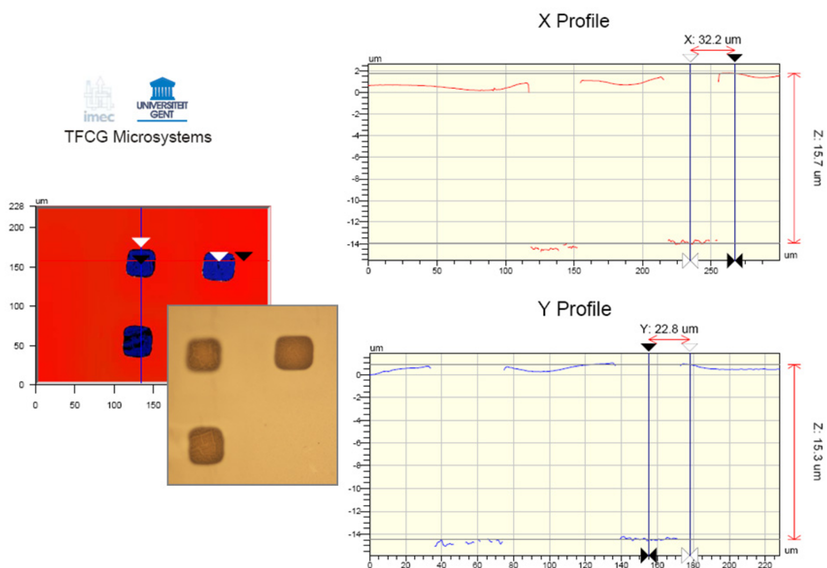


Figure 2.20: X- and Y-profile, measured using a non-contact optical profiler (Wyko NT3300)

An overview of the different process steps for this via dry etch process is given in Table 2.14. This overview includes already the dry step of the polyimide and the RIE, which will be needed before sputtering of the top metal, to compare this technology with the CO_2 laser drilling. Most of the process steps are the same as for the CO_2 laser based via technology, see Table 2.11. The main difference is the replacement of the CO_2 laser drilling by a 45 minutes RIE step.

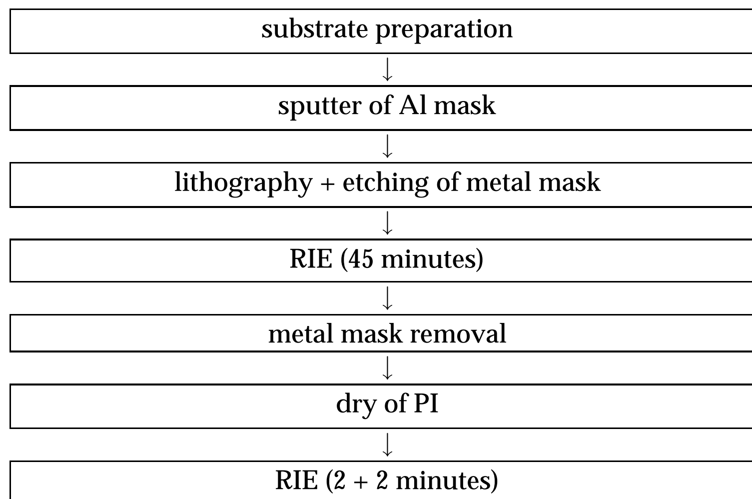


Table 2.14: Process flow for via ablation by RIE

2.7 Metallization

Once the dies are embedded in polyimide and the vias to the contacts of the chips are opened, the top metal layer can be applied. This metal can be very thin, but has to provide a good contact to the pads of the chip and the interconnection pattern of the package, and has also to ensure a good adhesion on the cured polyimide.

As only a thin layer thickness is required, a thin film metal can be deposited by evaporation or sputtering. Different metals are available in house for evaporation or sputtering as interconnection metals: aluminum, chromium, copper, gold, nickel, titanium-tungsten and nickel-chromium. An overview of the properties of these thin film metals is given in Table 2.15 [23].

Metal	Symbol	Resistivity ($x10^{-8}$ Ω.m)	Melting point ^oC	CTE ppm/^oC	Thermal cond. W/m.K
copper	Cu	1.67	1083	19.7	418
gold	Au	2.35	1064	14.2	297
aluminum	Al	2.65	660	23.0	240
tungsten	W	5.52	3415	4.5	200
nickel	Ni	6.9	1455	13.3	92
titanium	Ti	55	1667	8.9	22
platinum	Pt	10.52	1774	9.0	71
palladium	Pd	10.75	1550	11.0	70
chromium	Cr	12.99	1900	6.3	66
tantalum	Ta	15.63	2980	6.5	58

Table 2.15: Overview of material properties of typical thin film metals [23]

Cu is selected because of its low resistivity, so Cu can provide good interconnections to the contacts of the chip. In order to improve the interconnection to the other metal layer of the bumps, an extra layer of 50 nm titanium-tungsten (10% Ti, 90% W) is sputtered first. The titanium is able to reduce the oxides on the intermetallic contacts, this way titaniumoxide is formed which is conductive, resulting in a nice Ohmic contact to the contact on the chip.

TiW is also well known as adhesion layer. Adhesion of the metal on the cured polyimide film will also be improved by plasma treatment of the cured PI before sputtering of the interconnection metal layer. The optimization of the adhesion of sputtered TiW/Cu metal on cured PI is discussed in the section below.

2.7.1 Sputter deposition process

The TiW and the Cu layer are both deposited by DC magnetron sputtering in an Alcatel SCM600 system. This system, as installed in the cleanroom, is shown in Figure 2.21. A typical property of sputtered metal layers is a nice step coverage of the sputtered layer. This is important to ensure sufficient bottom and sidewall metal deposition, so the via can provide a good contact.

Figure 2.21: Alcatel SCM600 sputter system as installed in the cleanroom

The parameters of the sputter process for depositing TiW and Cu were already optimized and are given in Table 2.16. The metals are sputtered using an Argon plasma. Typical deposition rates of the Cu are about 100-125 nm/minute, and for TiW about 30 nm/min.

Material	Argon pressure	Power	Thickness	Sputter Time
TiW	1×10^{-2} mbar	1200 W	50 nm	1 min40 s
Cu	5×10^{-3} mbar	2000 W	1 μm	10 min

Table 2.16: Sputter parameters for TiW and Cu deposition

2.7.2 Adhesion study

In order to have optimum adhesion strength of this metal on the cured polyimide layer of the package, a plasma treatment is introduced.

Thin 50 nm TiW 1 μm Cu layers sputtered on untreated polyimide pass the Scotch tape test.

Peel strengths of the Cu/TiW/polyimide system were also measured. The 50 nm TiW 1 μm Cu is first enforced by electroplating up to 25 μm. This resulted in a very poor adhesion of this thick Cu layer on the untreated polyimide: peel strength is only 0.06 N/mm.

The adhesion of this metal on the polyimide layer is improved drastically by introducing a plasma pretreatment before sputtering the TiW Cu. The surface of the polyimide is first modified by an RIE pretreatment: first 2 minutes with a 5 sccm-CHF_3/20 sccm-O_2 gas mixture, followed by 2 minutes 25 sccm oxygen plasma; both applied with a power 150W of and a pressure 100 mTorr. On this RIE treated polyimide layer, 50 nm TiW and 1 μm Cu layer was sputtered and electroplated up to 25 μm. The measured peel strength after this plasma treatment is higher than 1.6 N/mm. The RIE pretreatment results in a significant improvement of the adhesion of the metal on the cured polyimide.

2.7.3 UTCP top metallization

The top metal layer will be sputtered on the RIE treated polyimide. Typical metal thickness of these sputtered layers are 50 nm TiW and 1 μm Cu. If thicker interconnection layers are needed, only a thin seed layer will be sputtered and can be enforced during a next electroplating process. This will be done by pattern plating.

Sputtered metal layer

If only limited metal layer thickness is required, a sputtered thin film metal layer can provide the interconnections to the contacts of the chips. Typical layer thicknesses are 50 nm TiW and 1 μm Cu, with typical resistivity of 10–15 mOhm per square.

Lithography For photolithographic patterning of this sputtered layer a photoresist AZ® 4562 (AZ Electronic Materials) is spincoated at 2000 rpm. After soft bake (30 min at 90°C in oven), the photoresist is illuminated through a glass mask and developed with a standard developer. After development, the photoresist is hard baked in an oven at 120°C.

During this lithographic step, it is important to optimize illumination and development conditions to ensure the resist pattern is well developed at the edges of the chip: residual photoresist between 2 adjacent tracks would prevent etching and introduce shorts in the package. For this application, the resist is illuminated at 400 mW/cm^2 and development time is 1 minute.

Etching In the next step the TiW Cu stack is etched. The Cu is etched in a $FeCl_3$ solution (25 g $FeCl_3$/1.5 l DI water). This 'slow' etchant was chosen since most of the standard Cu etchants are too aggressive, introducing too much underetch in the interconnect pattern. Typical etch time is 3–4 minutes.

Also the TiW layer is etched: for 10 seconds in warm 30% H_2O_2 (50°C) and then 10 seconds in cold 30% H_2O_2 solution (room temperature).

Finally the photoresist is stripped.

Sputtered seed layer

If thicker Cu layers are required, the sputtered thin film layer can be enforced by electroplating. This will be done using pattern plating. This semi-additive process starts on a thin Cu layer. The thin film metal is then imaged with a negative circuit pattern, created in photoresist. Next, the circuit is electroplated to the desired thickness. After plating, the resist is removed and the samples are etched shortly to remove the thin seed layer.

First a 50 nm TiW / 500 nm Cu layer seed layer is deposited by sputtering. Next the inverted pattern is aligned and defined in photoresist. The AZ® 4562 is spincoated at 2000 rpm with a layer thickness of 7.5 μm and dried at 90°C for 30 minutes in oven. After illumination for 400 mW/cm^2 and development, the resist is hard baked at 120°C.

Next, a thick second layer of copper is deposited on the uncovered traces by electrolytic deposition, targeting 6 μm. After this plating, the photoresist is stripped

and the seed layer is ready for etching. Finally the thin Cu layer is removed during a short etch step in $FeCl_3$ solution (25 g $FeCl_3$/1.5 l DI water), and the TiW is etched in H_2O_2 solution.

It is important that the photoresist is well developed, especially at the edges of the die. Remaining photoresist in the track prevents plating. This results in opens in the circuit after seed layer removal, see Figure 2.22.

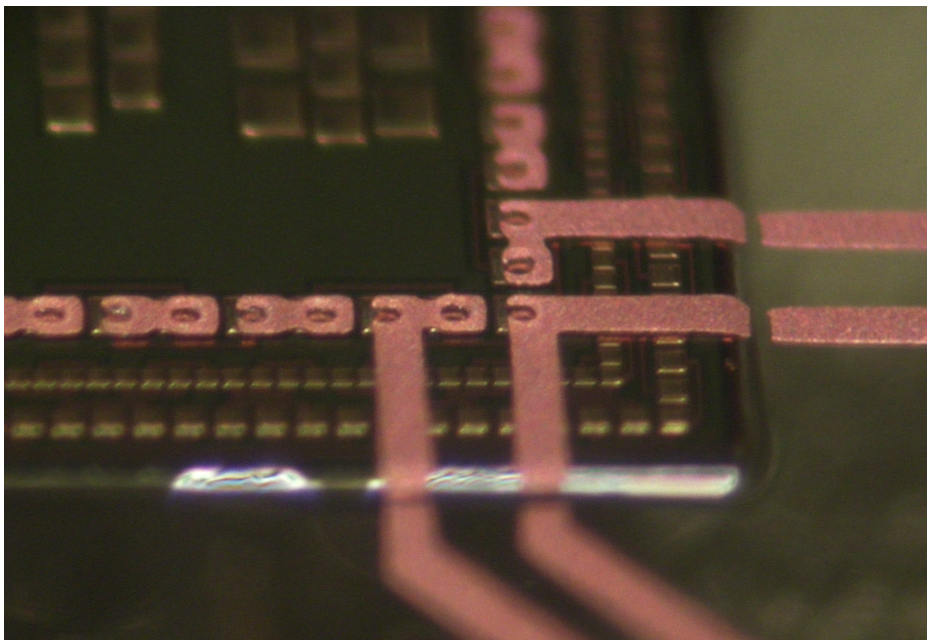
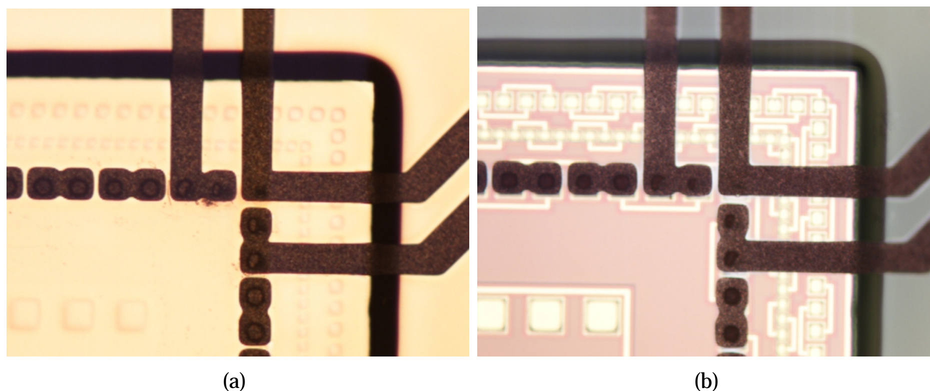


Figure 2.22: Open circuit after seed layer removal, due to bad lithography (the bottom of the vias were also not plated)

The result after Cu plating is shown in Figure 2.23, (a) before and (b) after seed layer etch.



(a) (b)

Figure 2.23: The result after pattern plating: (a) before seed layer etch, (b) after seed layer etch

2.8 Solder mask

Similar to conventional PCB or FCB manufacturing, a solder mask can be applied on top of the UTCP package. This solder mask forms a permanent protective coating for the copper traces, prevents bridging between conductors by solder and limits the risk for overplating during the application of a NiAu finish.

A dedicated flex solder resist (Elpemer SD 2463 Flex, Lackwerke Peters) is screen-printed on the UTCP substrate. Owing to the excellent adhesion on flexible base material (for instance, polyimide and polyester film) and outstanding flexibility, this resist is especially suited for application on flexible circuits. The solder mask is a green transparent, 20 μm thick, highly flexible layer.

The different process steps for the application of this solder mask are:

- screen print
- prebake during 40 minutes at 75°C
- illumation: 250 mJ/cm^2
- development in 1% Na_2CO_3 solution
- cure for 60 minutes at 150°C in convection oven

After screen printing, this solder resist is first prebaked during 40 minutes at 75°C. Next, the resist is illuminated and developed in a Na_2CO_3 solution. After development, the resist is cured at 150°C for 60 minutes.

2.9 NiAu finish

If desired, an extra NiAu finish can be applied on the Cu contacts of the UTCP packages, using a conventional PCB-like electroless nickel / immersion gold plating process. The different steps for this Ni/Au plating process can be described as follows:

- PCB cleaner: to remove any possible surface contaminants
- Cu microetch: to guarantee that all exposed copper surfaces are fresh and oxide-free
- Pd catalyst: a $PdCl_2$/HCl solution, selective deposition of Pd only on the exposed Cu surfaces
- rinse
- electroless nickel deposition
- rinse
- immersion gold: to convert the deposited nickel surface into a gold layer of around 0.1–0.15 μm.

The different baths used in this process are commercially available, and are listed in Table 2.17.

process step	bath	parameters
cleaner	Aureus™ 7910	3 min/40°C
microetch	Aureus™ 7920	4 min/RT
activator	Aureus™ 7930	4 min/25°C
electroless Ni	Enplate NI-865	8 min/90°C
immersion Au	Aureus™ 7940	8 min/70°C

Table 2.17: Commercial baths used for the electroless nickel / immersion gold plating process

Typical thickness for the deposited Ni layer is 3 μm (8 minutes in the Enplate NI-865 bath at 90°C). The application of solder mask on the UTCP package is required before plating, since overplating of Ni/Au is a major problem for fine-pitch patterns. The solder mask covers this fine-pitch area (i.e. the chip area) preventing shorts between adjacent Cu pads.

2.10 Release from carrier

After processing, the chip package can easily be cut out from the carrier. This can be done either manually or, if more precision is needed, by laser cutting. Finally the polyimide releases easily from the glass substrate. Figure 2.24 shows the manual release of a UTCP package from its rigid glass carrier after all UTCP process steps.

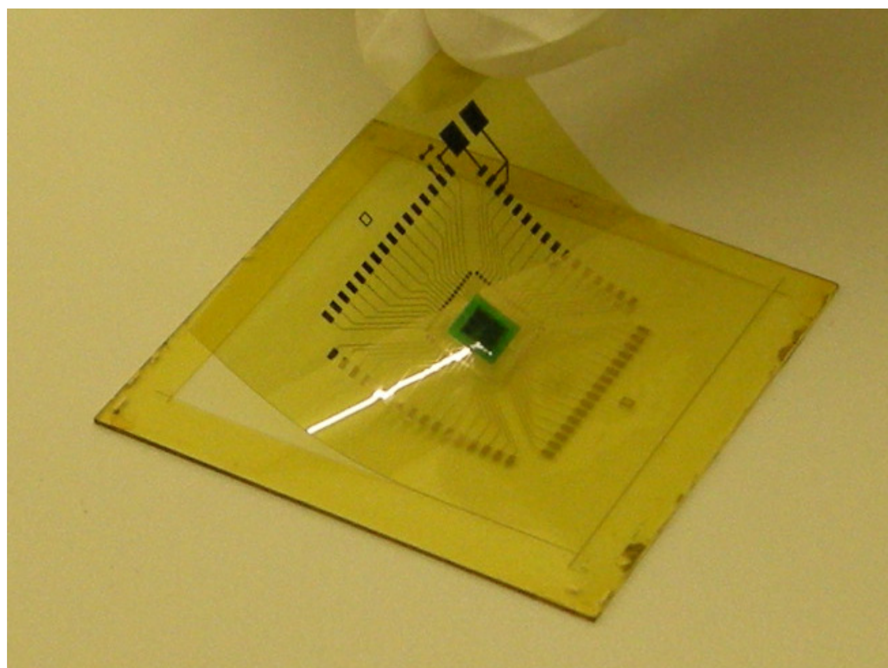


Figure 2.24: Release of a UTCP package from its rigid glass carrier

In order to prevent too much force applied on the chip and the interconnects, release can also be enhanced by ultrasonic agitation in water.

2.11 Conclusions

The different process steps of the Ultra-Thin Chip Package technology have been discussed in detail. Ultra-thin chips with thickness between 15 and 30 μm can be packaged in between 2 spin-on polyimide layers as UTCP. The result is a very thin chip package, with a total thickness of only 50–60 μm.

The base substrate is a uniform polyimide PI-2611 layer, applied (spin coated and cured) on a rigid carrier. Then the ultrathin chip is placed and fixed, using BCB as die attach material. Next, the second spin-on polyimide layer is applied and cured. Vias to the contacts of the chip can be laser drilled and the contact metal layer is sputtered and photolithographically patterned. This metal layer is providing a fan out to the contacts of the chips. Finally the whole package is released from the rigid substrate.

A special release technology has been developed: selective adhesion of the polyimide only to the edges of the glass carrier is easily obtained by selective application of adhesion promoter, the VM652, before spincoating the polyimide.

Polyimides and BCB were compared as die attach materials. Nice voidfree bonds were obtained using a dispensed BCB Cyclotene 3022-46.

RIE plasma treatments can be used to ensure good adhesion of polyimide PI-2611 on cured polyimide or BCB, and also to improve the adhesion of the TiW Cu layer on the top polyimide of the UTCP package. The application of adhesion promoter VM652, ensures sufficient adhesion of the polyimide on the chip surface.

Different laser ablation based technologies were developed and discussed. Also feasibility of dry etching of microvias using Reactive Ion Etching has been demonstrated.

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Chapter 3

Feasibility study of UTCP technology

This chapter gives an overview of the different feasibility test results on the UTCP technology. Electrical interconnection tests are performed on UTCP integrated interconnection test chips. Via and daisy chain resistances are characterized, also for the different via technologies. The first section describes the interconnection test sample production, including discussion of the test chip layout and the interconnection test design. The next sections focus on the reliability investigations, including thermal ageing up to 1000 h at 125°C and 150°C, high temperature / humidity testing at 85°C/85 relative humidity as well as thermal cycling between (-40°C and 125°C) up to 1000 cycli. The chapter also presents the UTCP embedding of ultra-thin, functional devices. A TI microcontroller and a Nordic radio chip have been integrated as UTCP package and tested: the back thinning and the UTCP integration has no impact on the functionality of these devices. The final section includes some thermo-mechanical simulation results, calculating the stresses introduced during the processing and confirming the bendability of the UTCP packages.

3.1 Interconnection test samples

3.1.1 Test chips

The test chips used for the production of the first UTCP embedding test samples are thinned-down silicon interconnection devices. These test chips were available at IMEC Leuven, and are specified as PTCK test chips, which stands for 'Package Test Chip version K'. The die size is 5 mm by 5 mm and the dies were thinned down to 16–17 μm.

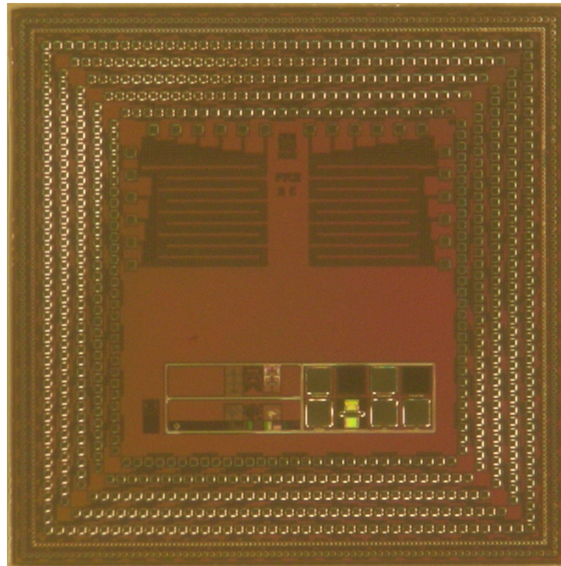


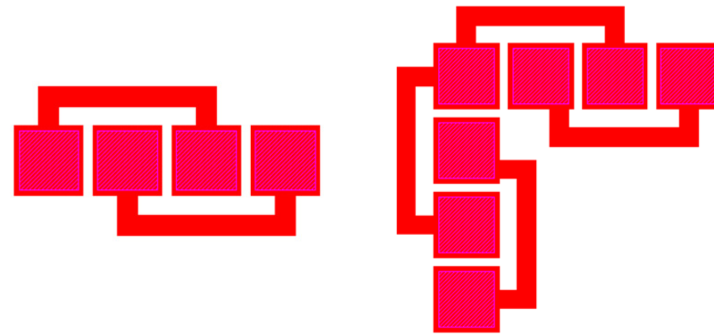
Figure 3.1: Bond pad layout of one version of the PTCK test chip

Figure 3.1 shows the bond pad layout of one version of the PTCK test chips. There are four different versions of these test chips, but all versions have identical peripheral bond pad layout, containing 3 daisy chains. The outer daisy chain has a 60 μm contact pitch, with pad sizes of 40 μm x 40 μm, and a total of 316 pads. The center daisy chain has 40 μm pitch, with pad sizes of 30 μm x 30 μm, and a total of 456 pads and the inner daisy chain a 100 μm pitch, with pad sizes of 70 μm x 70 μm, and a total of 172 pads. The contact pads are finished with 5 μm Ni and an Au flash.

All UTCP interconnection test samples are based on the 100 μm pitch daisy chain. Figure 3.2 shows the interconnection pattern of this daisy chain.

3.1.2 Test design

A dedicated test design is made, based on the layout of the PTCK test chips and fitting with the 100 μm pitch peripheral contact pads, see Figure 3.3. The test pattern allows for daisy chain patterns as well as for 4-point-measurements. The daisy chain pattern is provided between contacts DC 1 - DC 5 and the 4 point-measurement pattern for measuring the via contact resistances are X.1–X.4 are found at each corner of the die. The contact pads on this design have a diameter of 400 μm.



(a) Pad interconnections on the chip (b) Interconnections at the corner

Figure 3.2: Design of daisy chain pattern on the IMEC interconnection test chips

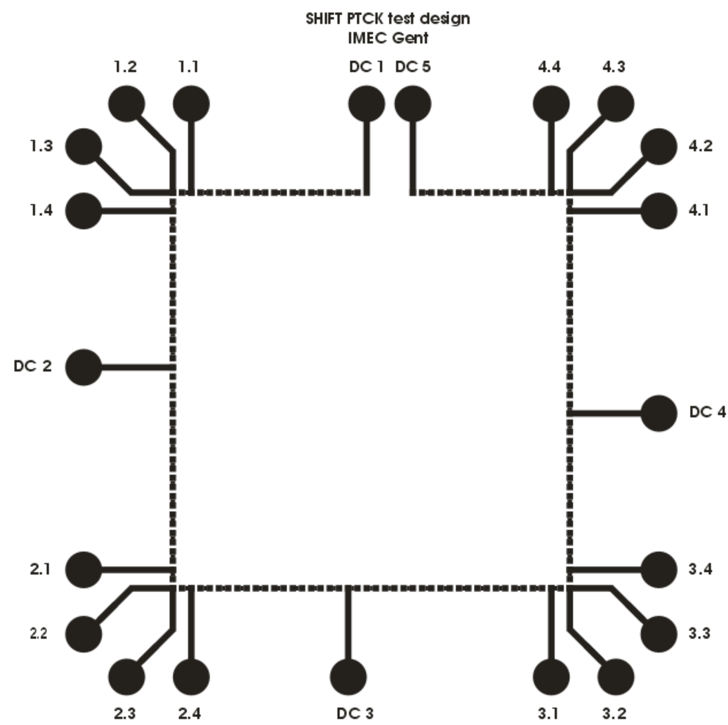


Figure 3.3: UTCP interconnection test design

3.2 Electrical measurements

3.2.1 Measurement set-up

Electrical tests are performed with a SMU, a Source Measurement Unit. The small via resistances are measured using a four-point technique: two probes are used to source current and two other probes are used to measure voltage. The use of four probes eliminates measurement errors due to the probe resistance, contact resistance between each metal probe and the contact pad, etc. A current of known value is caused to run through the via of interest, and the voltage drop across this via is measured with the 2 other probes: since the high impedance voltmeter draws only very little current, the voltage drops across the probe resistance, contact resistance, etc. are very small and can be neglected. Probes placed on the contacts X.1-X.2 will be used for sourcing current through the via, the other two are contacted on X.3-X.4 for measuring the voltage drop along the via. (Or vice versa, using X.3-X.4 for current sourcing and X.1-X.2 for voltage measurement.) The resistance value can be easily calculated using Ohms law. The set value for the current sourcing through the vias is +/- 100 mA, the via resistance value will be the average of the value for + 100 mA and the value for - 100mA.

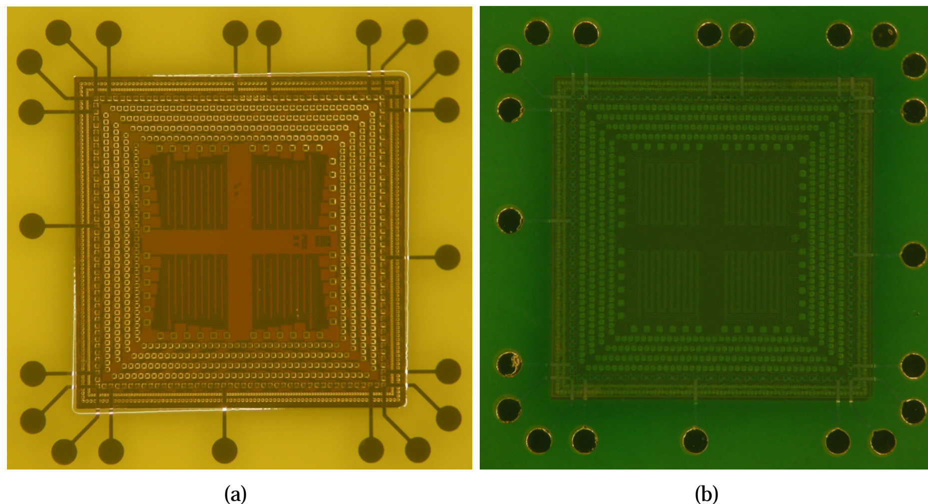
Also the daisy chain measurements are performed on a SMU. Due to design error, the contacts DC 1 and DC 5 are not properly connected to the daisy chain, so the daisy chain could only be evaluated between the contacts DC 2–DC 4, including 82 vias.

3.2.2 Optimized UTCP test samples

Interconnection test samples were produced following the optimized UTCP technology process, as discussed in detail in Chapter 2. An overview of different layers of these packages is listed here:

- base substrates: 20 μm polyimide applied on rigid glass carrier
- chip placed face-up using dispensed BCB as adhesive
- 20 μm top polyimide layer covering the chip
- vias opened by CO_2 laser ablation, followed by RIE clean step
- top metal: sputtered 50 nm TiW 1 μm Cu
- solder mask, covering fine pitch interconnections
- ENIG finish, deposited on larger contact pads not covered by solder mask.

The realized test samples are shown in Figure 3.4.



(a) (b)

Figure 3.4: UTCP integrated interconnection test chips (a) prior to solder mask deposition and (b) after NiAu deposition

The average value of 24 measured via resistances is 23.2 +/- 9.5 mΩ. An average value for 12 measured daisy chains between contacts DC 2–DC 4, is 40.80 +/- 1.42 Ω.

3.2.3 Test samples for alternative via technologies

Via resistance measurements were performed to check the via interconnections to the integrated device, to evaluate both the via technology as the metallization of the vias. During the development and optimization of the UTCP technology several UTCP test samples (with the different technologies) were produced and characterized.

An overview of the measurement results is listed below, per via technology. In most of the cases only few test samples were realized, only for demonstrating the feasibility for each of the different via technologies presented in Chapter 2. This section gives a very short overview of the available measurement results.

Shaped beam YAG laser

The first UTCP test samples were produced using the frequency tripled YAG laser with shaped beam (see Section 2.6.3). Due to instability of the beam shaping op-

tics, only very few samples were produced with this technology. Via resistances down to 20 mΩ have been measured on the available samples. Metallization on these samples was 6 μm pattern plated Cu.

YAG laser drilling through thinned top PI

An alternative technology is first thinning down the top polyimide down to 5 μm and opening the vias through this thin polyimide layer using the frequency tripled YAG laser, see Section 2.6.3. Only 1 sample was produced, the measurement results are given in Table 3.1. (Metallization was done by Cu pattern plating, up to 6–7 μm.)

This technology was characterized more extensively in the framework of the PhD work of Jonathan Govaerts, see also [1].

measured via	resistance [Ω]
4PT1	0.0469
4PT2	0.0475
4PT3	0.0484
4PT4	0.0476
DC 2–DC 4	35.72

Table 3.1: Measurement results on sample with vias drilled by frequency tripled YAG laser through thinned polyimide layer

CO_2 via ablation, followed by an excimer clean step

An alternative technology for the CO_2 via ablation followed by an RIE clean step was the CO_2 via ablation followed by an excimer clean step, see Section 2.6.4.

Both technologies were compared on the same sample: only one part of the sample had the extra excimer cleaning step. The metal mask was removed and the residual PI film was removed during an 10 minutes RIE step. This sample was shown in Figures 2.12, 2.13 and 2.16. The sample was metallized with a sputtered 50 nm TiW 1 μm Cu layer. The via resistances on this sample were the same for the RIE cleaned part (42 mΩ) as for the part only cleaned during the RIE step (40 mΩ).

This indicates that both technologies will give very similar interconnection results.

Dry etched vias

The feasibility for dry etching of the vias in the polyimide layer was demonstrated in Section 2.6.5.

One sample was characterized and had average via resistance value of 47 mΩ. (This sample had 1 μm sputtered Cu and was dry etched at HighTec MC AG.)

3.3 Reliability investigations

This section describes the reliability testing of the UTCP technology. Test vehicles were subjected to thermal cycling tests between -40°C and +125°C, temperature/humidity testing conditions at 85°C/85 r.h., and to thermal ageing at 125°C and 150°C.

3.3.1 Thermal cycling

The thermal cycling test is used to assess the integrity of the package via interconnections under cyclic strain. This test is conducted to determine the ability of the package to withstand mechanical stresses induced by alternating high and low temperature extremes. While the thermal cycling test is not a simulation of use environment, it however constitutes an accelerated life test. It enables to identify weak links in the packages in question: one can determine the reliability of the microvia interconnections, weak interfaces inside the package and the reliability of the different materials in the package.

Thermal cycling exposes samples to a series of high and low temperature excursions, as defined in JEDEC Standard JESD22-A104C [2]. The test is performed in a Vötsch temperature chamber VTS 7040-15, under following conditions (in air):

- min. temperature: -40°C
- max. temperature: 125°C
- dwell at extremities in temperature: 4 min
- ramp rate: 15°C per minute
- total cycle time: 30 minutes.

The temperature profile of the first cycle is shown in Figure 3.5. The cycle starts at room temperature, total ramp time between the extremities is 11 minutes and the total cycle time is 30 minutes (2 cycles per hour).

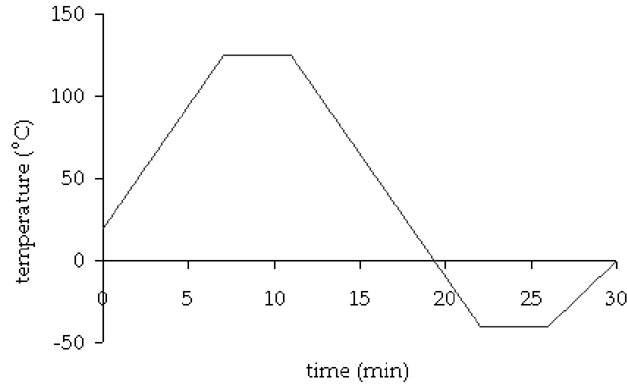


Figure 3.5: Temperature profile of a thermal cycle, starting and ending at room temperature, cycling between 40°C and +125°C

Three UTCP packaged interconnection PTCK test chips were subjected to the test. Daisy chain (between DC.2 - DC.4, containing 82 vias) and four point Kelvin resistances (one at each corner, 12 in total) have been measured after specified periods to characterize the interconnections and monitor degradation effects. All samples reached the 1000 cycles without any failure.

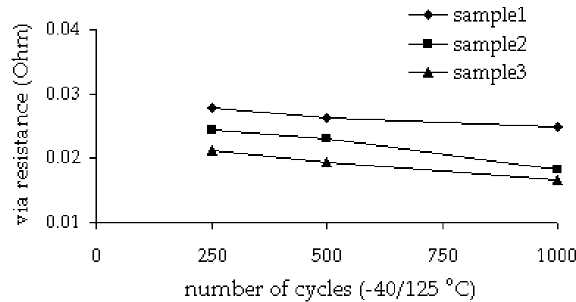


Figure 3.6: Average via resistance per sample under thermal cycling until 1000 cycles

The average values for the via resistances are depicted in Figure 3.6. The measurement results during the first 250 cycles are not included in this graph because

of a measurement error due to incorrect measurement set-up. All 12 characterized vias showed a decrease in resistance value under thermal cycling conditions.

The daisy chain measurement results on the same samples are found in Figure 3.7. Also these daisy chain interconnections reached the 1000 cycles. Only low increase in resistance after 1000 cycles was noted: increase of DC resistance on sample 3 was 2.3 %, on sample 2 0.8 % and sample 1 showed even a decrease of 1.3 %.

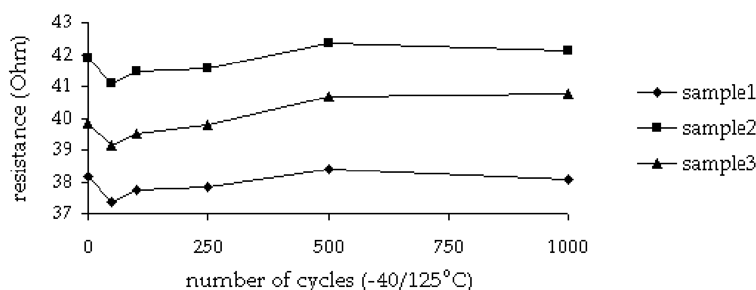


Figure 3.7: Daisy chain resistances under thermal cycling until 1000 cycles

3.3.2 Humidity storage

The purpose of the temperature/humidity testing is to evaluate the performance of the assemblies in humid usage environments. The packages are subjected to moisture resistance test and are stored at 85°C and 85% relative humidity (see also JEDEC Standard EIA/JESD22-A101-B). The test is carried out in a CTS Climate chamber CS-40/200. This climate chamber maintains the temperature within 1°C of the set temperature and humidity within 1% of the set value.

Three samples were subjected to these conditions up to 1000 h. Daisy chain as well as four point Kelvin electrical measurements were performed at specified periods. All samples passed the 1000 hours without any failure.

The values of the via resistances are depicted in Figure 3.8. Also this graph does not include the measurement results during the first 250 cycles because of a measurement error due to incorrect measurement set-up. None of the 12 measured vias increased significantly during 1000 h humidity storage. Only sample 1 shows an increase in via resistance, but after 1000 h of storage the average via resistance value measured on this sample is still very low: only 12.8 mOhm.

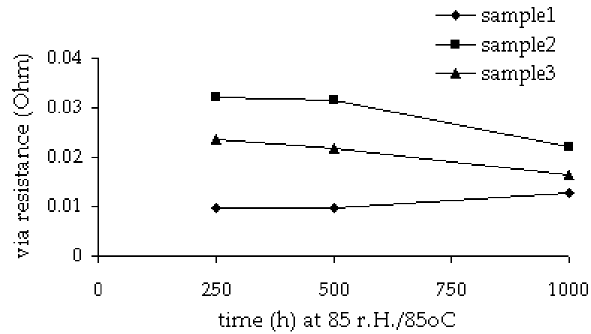


Figure 3.8: Average via resistance per sample under humidity storage up to 1000 hours

The daisy chain measurement results on the same samples are found in Figure 3.9. All daisy chain interconnects passed the 1000 h humidity storage. Sample 1 shows the largest increase of about 3.6 % after 1000 h, compared with the initial value.

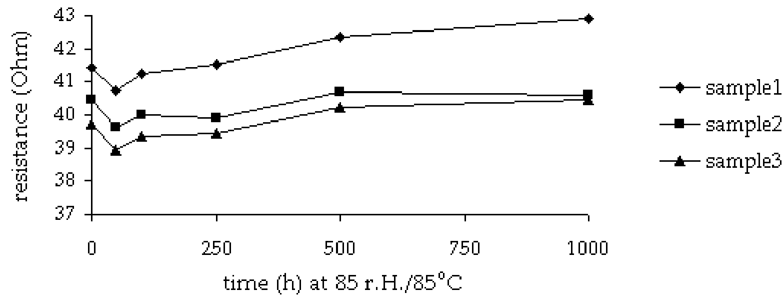


Figure 3.9: Daisy chain resistances under humidity storage up to 1000 hours

3.3.3 Thermal ageing

High temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices. During the test, elevated temperatures (accelerated test conditions) are used without electrical stress applied, see also JEDEC standard JESD22-A103C.

High temperature storage up to 1000 h, both at 125°C (Condition A) as well as storage at 150°C (Condition B) has been investigated.

High temperature storage at 125°C

Three samples, from the same batch as the samples that passed the 1000 h hot humidity testing and the 1000 thermal cycles, were subjected to high temperature storage at 125°C up to 1000 h, in air.

None of the samples reached the 1000 hours without serious increase in via resistance (although similar samples from the same batch passed 1000 cycles between -40°C and 125°C). The average value of the 12 measured via resistances after 250 h was already 63.06 mΩ (with maximum of 217.65 mΩ), after 500 the average four-point value was 96.8 mΩ (with maximum of 284.3 mΩ) and after 1000 h the vias had already an average resistance of 358.62 mΩ (with maximum of 1.326 Ω).

This study was also repeated with two other samples from a different, previous batch. These two samples were processed using the same technology as the samples described above (including same via technology and metal finish), but the samples did already pass 1000 thermal cycles between -40°C and 125°C during an initial, preliminary reliability investigation.

Both samples passed the 1000 h of storage at 125°C successfully: the measured values of the via resistances even decreased during the testing. The evolution of the average 4PT via resistance value per sample is depicted in Figure 3.10.

All four 4PT structures of sample 1 could be measured, only 2 of the 4PT structures of sample 2 (due to processing: bad lithography + overetching) could be measured. The average value of the 6 characterized via resistances before the high temperature storage was 22.75 +/- 9.8 mΩ and decreased during the test, down to 18.39 +/- 8 mΩ after 1000 h.

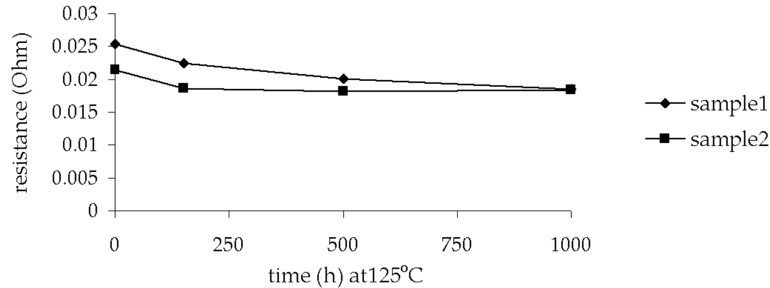


Figure 3.10: Evolution of average 4PT via resistance value per sample, during the second high temperature storage study at 125°C, up to 1000 hours

High temperature storage at 150°C

Also for the high temperature storage study at 150°C three samples were tested, from the same batch as the samples that passed the 1000 h hot humidity testing and the 1000 thermal cycles between -40°C and 125°C. None of these samples reached the 1000 h of storage.

The average value of 12 measured via resistances after storage for 250 h at 150°C was 140.18 mΩ. After 500 h of storage already 3 out 12 vias were unmeasurable; after 1000 h even 9 out of 12 vias were open circuits.

This study was repeated on two other samples from a previous run (from the same batch as the samples used for the second high temperature storage test at 125°C). These samples were processed using the same technology as the UTCP interconnection test samples used for the first test (including same via technology and metal finish). These samples had already been subjected to 1000 thermal cycles, between -40°C and 125°C, during a preliminary reliability study.

Five 4PT structures were measurable on these 2 samples. The measurement results are given in Figure 3.11. After 150 hours of storage the average via resistance value was 19.85 +/- 13.73 mΩ (compared with initial value of 26.75 +/- 12.81 mΩ). After 500 hours of storage at 150°C the average via resistance was 26.67 +/- 34.02 mΩ (one via had increased resistance of 86.6 mΩ). During the next 500 h of storage, the resistances increased up to 79.25 +/- 51.74 mΩ in average (with max. value of 131.05 mΩ).

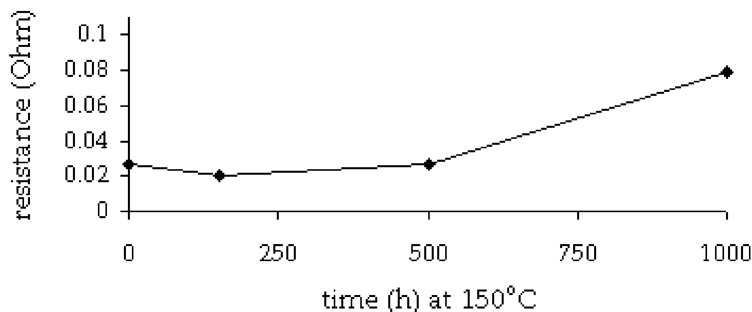


Figure 3.11: Evolution of average via resistance value, during the second high temperature storage study at 150°C, up to 1000 hours

Failure analysis

First high temperature storage testing indicated early failures, but these bad results were not confirmed in a second study, using similar UTCP test samples.

Cross sections were made from both samples. Inspection using an optical microscope, could not indicate any delayering or cracks in the metal interconnection layers of the failed samples.

The cross sections of both samples were also inspected using SEM/EDX analysis. This SEM/EDX analysis could only indicate the presence of Cu interconnects on the failed interconnection test chips.

A possible point of interest can be the sidewall roughness of the laser drilled vias. Figure 3.12 illustrates some of the cross sections. (a) and (b) show cross sections of vias on a sample that passed the high temperature storage, (c) and (d) give a cross sectional view of vias on a failed test samples.

The sidewalls on the failed samples seem to have a higher roughness, than the sidewalls on the 'good' samples. This could be another indication for the early failure. But this failure analysis is too limited to draw clear conclusions.

Further investigations on this problem are required to study the influence of the Cu interconnects on the chip, and the influence of sidewall roughness of the vias.

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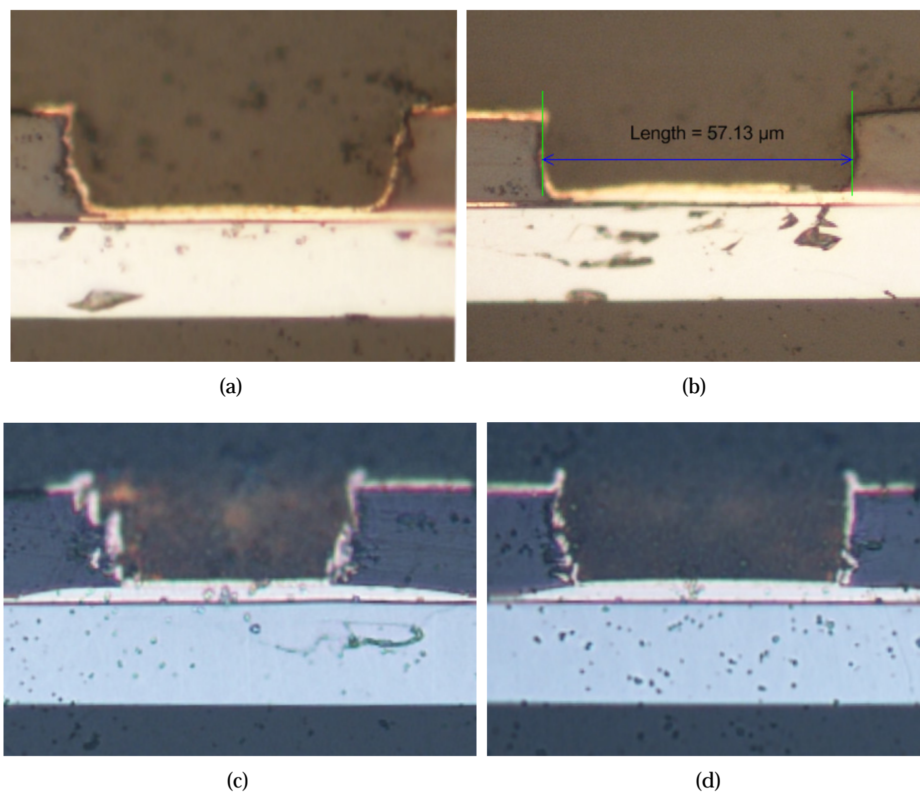

(a) (b)

(c) (d)

Figure 3.12: Cross section of vias: on a sample which survived high temperature storage at 150°C (a, b), on a test sample which failed during high temperature storage at 150°C (c, d)

3.4 UTCP packaged microcontroller

3.4.1 Introduction

Another important part of the feasibility program was the demonstration of the UTCP technology for functional devices.

A first functional demonstrator is the UTCP embedding of an ultra-thin microcontroller chip. The selected microcontroller is the MSP430F149, a member of the low-power MSP430 family by Texas Instruments [3].

The chips were available at IMEC Leuven, in unthinned naked die form. The controllers and the basic control software were verified before the processing.

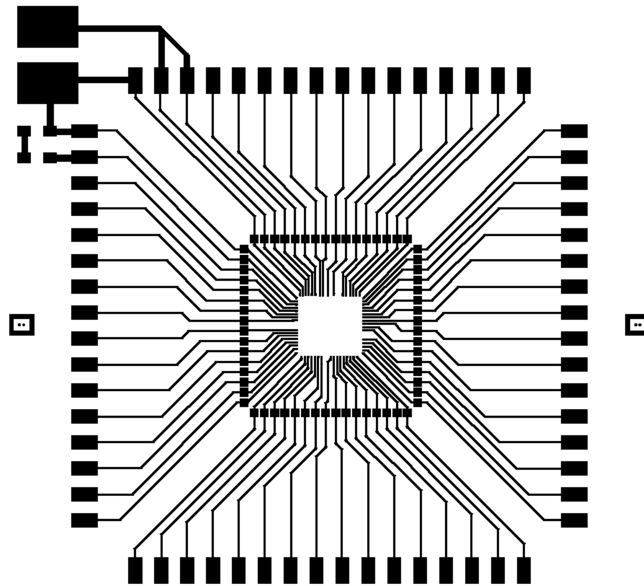

Figure 3.13: Fan-out design for the UTCP integration of the TI MSP430F14 microcontroller

3.4.2 Test design

A dedicated test design was made, fitting the microcontroller contact pads and providing a fan-out metallisation to these contacts.

This layout is shown in Figure 3.13: it includes a small fan-out of the 64 die contacts to 400 x 400 μm^2 contacts with pitch of 500 μm, and a larger fan-out to 650 x 1300 μm contacts. The outer, large contacts will be used to easily connect the integrated microcontroller for programming and testing. The inner contacts will be used for embedding the UTCP package in multilayer flex boards (see Chapter 4). Outer dimensions are 9 x 9 mm^2 for the small fan-out and 3 x 3 cm^2 for the large fan-out.

The design also includes solder pads to solder mount an SMD resistor and a LED component on top of the package for visual functionality demonstration after processing.

3.4.3 Preparation of the single dies

The microcontroller devices were provided by IMEC Leuven and were only available as bare, unthinned single dies. To be able to integrate these dies as UTCP package, some preparatory process steps were necessary:

- application of under bump metallurgy (UBM) on single dies, an extra metal finish on the Al pads is required to prevent contact pad damage during the via drilling process
- back thinning of the individual chips, from original die thickness down to 20–25 μm.

The results of these preparatory processing are discussed below.

NiAu bumping

The application of Electroless Nickel / Immersion Gold (ENIG) is a typical process to deposit under bump metallurgy (UBM) as finish of the chip contact pads. This process is normally done on wafer scale. A process dedicated for application of ENIG on single chips was available at CMST and this process is used to deposit 5 μm Ni and a Au flash.

The first batch of microcontrollers had only poor ENIG deposition on some contact pads. This thin NiAu layer turned out to be too thin to withstand the laser-drilling, see below. The process was further optimized, resulting in better, more uniform NiAu deposition on the Al contact pads.

Figure 3.14 shows a picture of an ENIG metallized chip contact pad, Figure 3.15 gives the profile of a bumped contact.

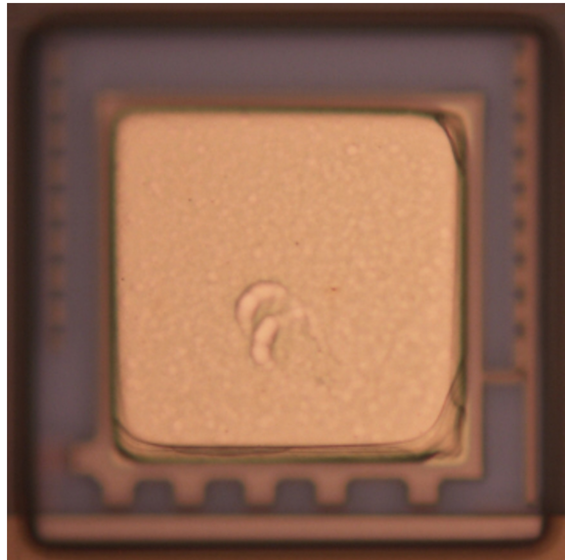

Figure 3.14: ENIG metallization on chip contact pad

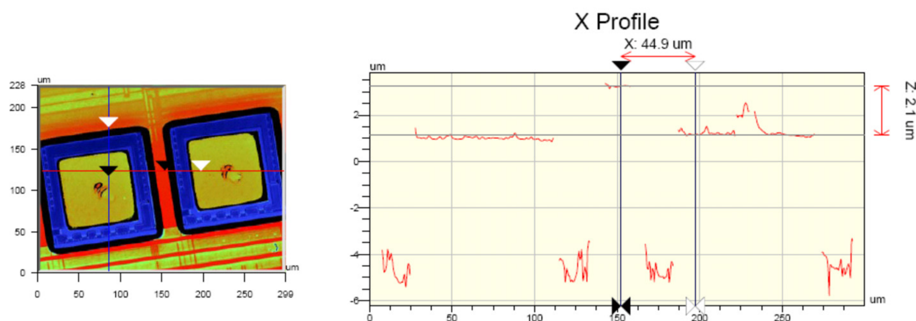

Figure 3.15: Profile of ENIG metallisation of contact

Individual die thinning

After NiAu plating the single microcontroller devices were thinned down, using the individual die thinning process as presented in Chapter 6. Original die thickness was +/- 260 μm, and thinned die thickness between 20–25 μm. More details and process parameters for the back thinning of the individual microcontrollers is discussed in detail in Section 6.3.3.

Basic electrical functional tests of the thinned microcontrollers were performed partly during the assembly process (after die thinning and attachment to the bottom substrate, but before encapsulation or metallization). This gives an idea on the influence of the thinning down of the Si for this functional microcontroller. Electrical tests were done after attachment with BCB on the base substrate since probing would be too difficult on brittle very thin single dies.

Measurement was done with a manual needle probing setup, and verified the following items:

- power consumption is correct
- microcontroller can be programmed and retains its program (flash memory OK)
- microcontroller properly executes its program (control logic and oscillator functionality OK).

Out of 10 tested half-assembled samples from the first run, only 2 failed (80% yield):

- 1 sample had a large visible crack in the die (failure in the thinning process); this microcontroller draws excessive power and was not functional

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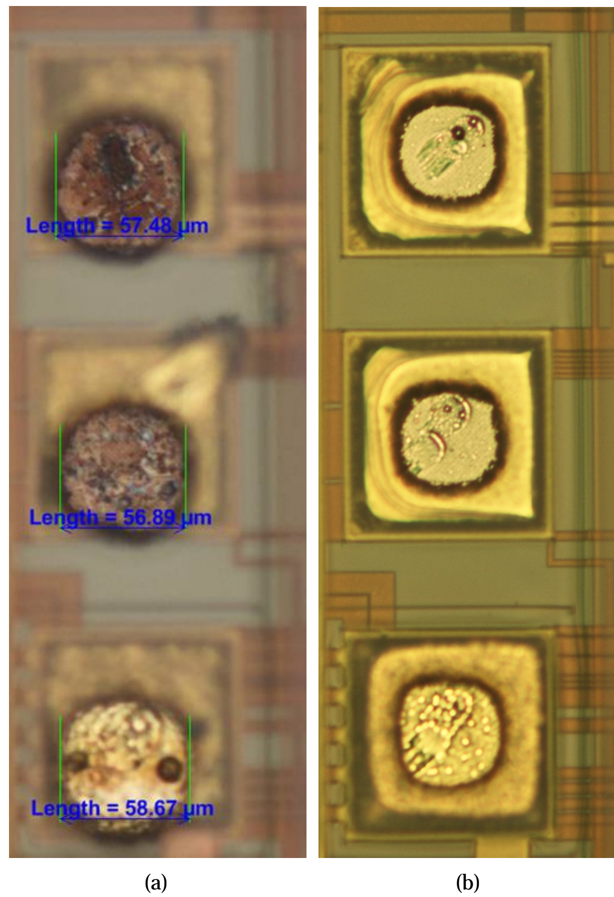
- 1 sample does not retain its program (failed flash memory); possibly non-visible damage from thinning in some parts of the die.

Also more extensive tests are performed on the characterization of the analog-to-digital converter of theses embedded microcontrollers, monitoring the effects of the silicon thinning. The linearity and also the AC specs (including signal to noise ratio (SNR), effective number of bits (ENOB), total harmonic distortion (THD), spurious free dynamic range(SFDR)) were compared, between an unthinned microcontroller die and a thinned microcontroller die. These measurements indicated no measurable degradation of the linearity: both the differential nonlinearity (DNL) as the integrated nonlinearity (INL) were still below 0.5 LSB after thinning. Also the difference for the AC specs before and after the die thinning process were tiny and within measurement error.

3.4.4 UTCP packaging

The thinned microcontroller devices were finally integrated as UTCP package (using the optimized UTCP process flow).

The crucial process step was the via drilling to the ENIG finished contact pads. During the first plating trials, some contact pads on the microcontroller dies were skipped or poorly plated. This caused problems during the CO_2 via ablation: almost all contact pad metallization is removed during via drilling and this prevented the contacting to these contact pads. In a next run the plating process was optimized and more electroless Nickel was deposited, also on the ’critical’ contact pads. This is illustrated in Figure 3.16. The left picture shows the contact pad damage introduced during via drilling, the right picture shows the same ’critical’ pads having better UBM quality.



(a) (b)

Figure 3.16: First UTCP embedded microcontrollers could not be connected on the contact pads with poor ENIG quality (a), this problem was solved in a second run (b)

Figure 3.17 shows the fan-out metallization to the microcontroller on the UTCP package. Figure 3.18 shows a finalized UTCP integrated microcontroller on its carrier: including solder mask and NiAu finish of the contacts on the package.

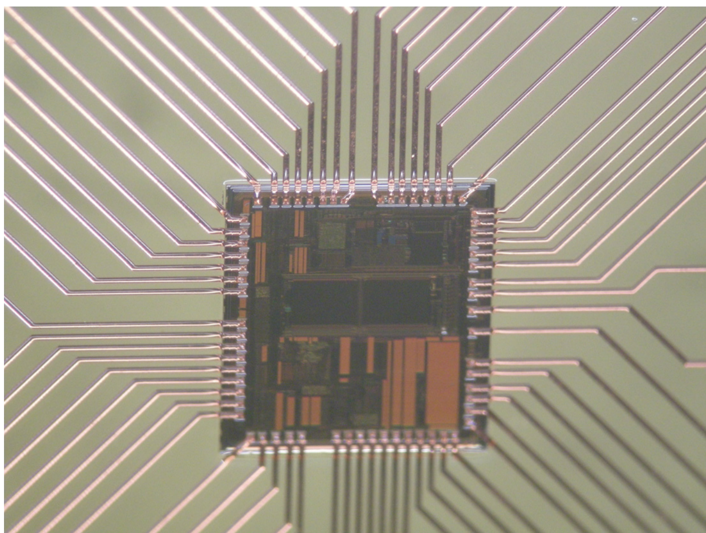


Figure 3.17: Fan-out metallization to the contacts of the integrated microcontroller

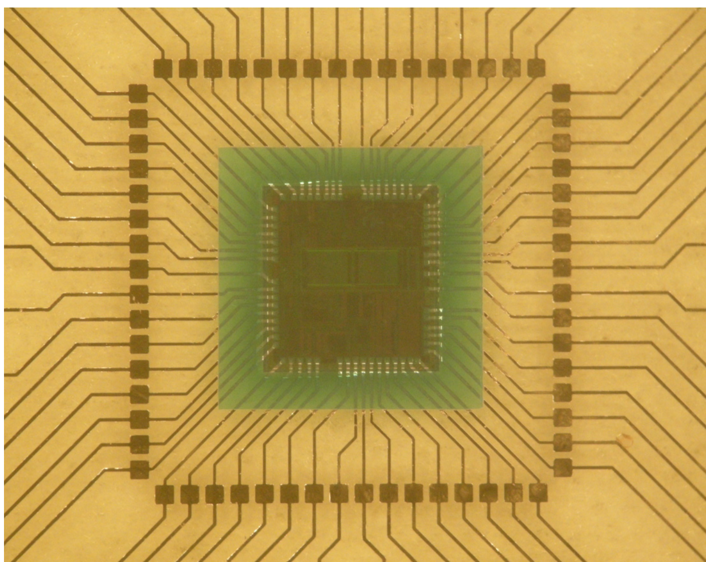


Figure 3.18: UTCP integrated microcontroller

3.4.5 Testing and characterization

Testing of the packaged microcontrollers was done after assembly, but before release from its carrier. This way it is easier to solder the connector and the components on the (rigid) package. The microcontroller was programmed to generate a blinking sequence on the LED to demonstrate its functionality. This is shown in Figure 3.19.

Figure 3.20 shows a sample released from the carrier and bent around a pen with 5 mm radius. Because the thin die is still more rigid than the surrounding polyimide flex, its bending radius is a bit larger (estimated visibly to be ≅ 8 mm). The sample is still perfectly functional in this condition.

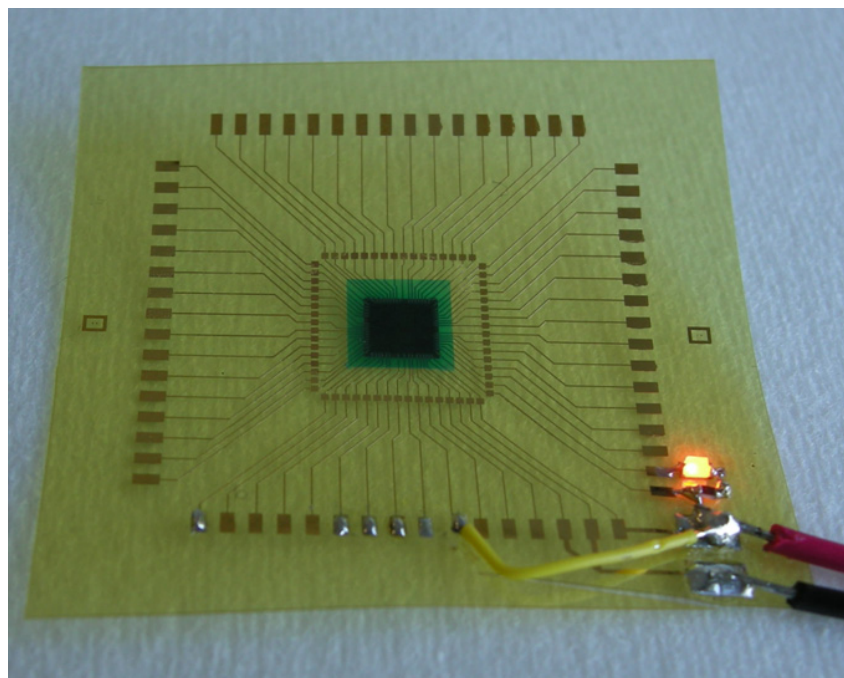
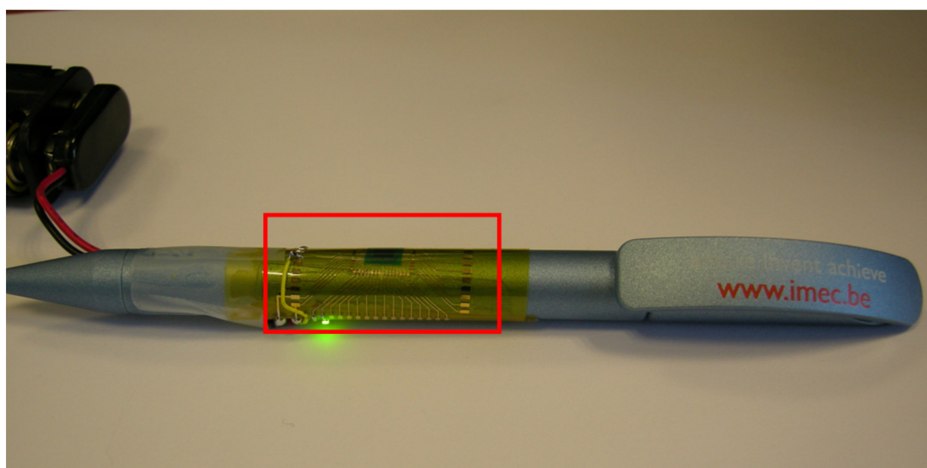
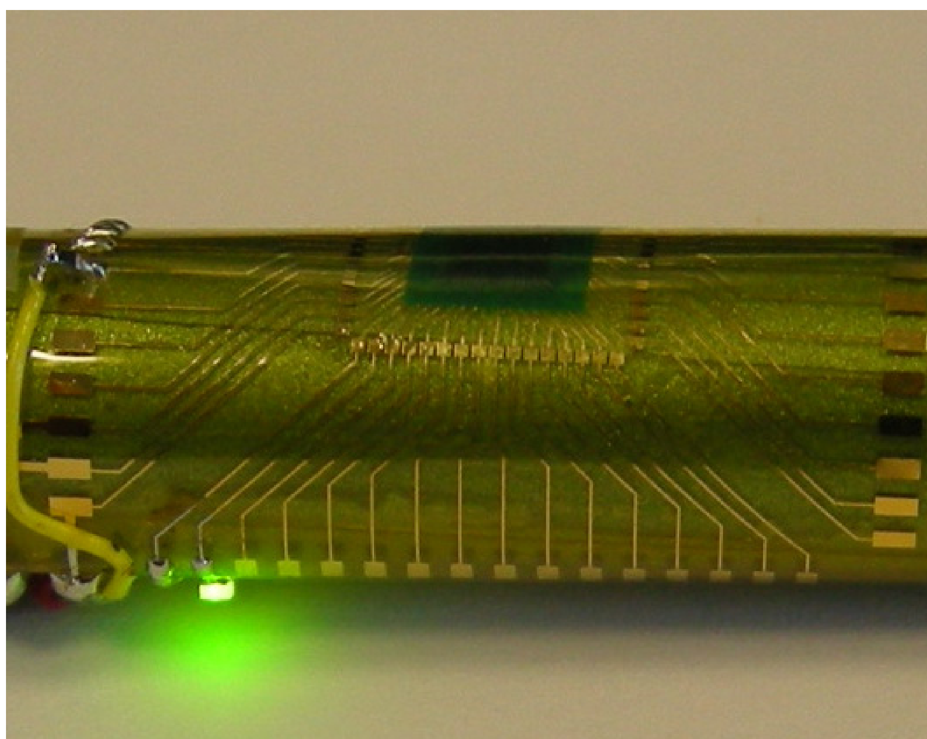


Figure 3.19: UTCP embedded microcontroller programmed to generate a blinking sequence on the LED to demonstrate its functionality



(a)



(b)

Figure 3.20: (a) Microcontroller bended around a pen with 5 mm radius is still perfectly functional, (b) close-up view of the area in the red frame

Also extensive tests of the analog-to-digital converter of the embedded microcontrollers are performed after UTCP integration, similar as done after silicon thinning (see Section 3.4.3 above). The linearity and also the AC specs (including signal to noise ratio (SNR), effective number of bits (ENOB), total harmonic distortion, spurious free dynamic range) were compared, between a thinned microcontroller die and UTCP packaged thinned microcontroller.

The UTCP packaged microcontroller has somewhat worse DNL and INL: below +/-1 LSB, instead of below 0.5 LSB on a naked die. Also the AC specs for the UTCP packaged device are slightly worse. So the UTCP performs slightly worse than the naked thin die which was wire-bonded to a rigid PCB. But the small deviations are limited and will have only little effect on the usability of the packaged microcontroller. And they may most probably be caused by factors external to the chip, e.g. thin wires that introduce parasitics in the reference and supply voltages during resolution of the LSBs, rather than the die itself.

All these measurements results are courtesy of Tom Torfs, IMEC Leuven.

3.5 UTCP integrated radio device

3.5.1 Introduction

A second functional demonstrator for the UTCP technology was the integration of a thinned down 2.4GHz low power radio transceiver (Nordic nRF2401A) [4].

These commercial radio devices were available at IMEC Leuven, in unthinned, bare die form. The single chips were first thinned down using the Si thinning process as presented in Chapter 6, and next integrated in the ultra-thin chip package.

The UTCP integrated radio devices were verified after the processing.

3.5.2 Design

A dedicated test design for this Nordic radio device was made by IMEC Leuven, based on an existing 'rigid' design. The design of this test circuit is shown in Figure 3.21. This design includes a fan-out metallization to the contacts of the devices (to 400 x 400 μm^2 contacts with a pitch of 500 μm), 12 SMD components and also some large contact pads to be able to solder small wires on the UTCP package, for testing.

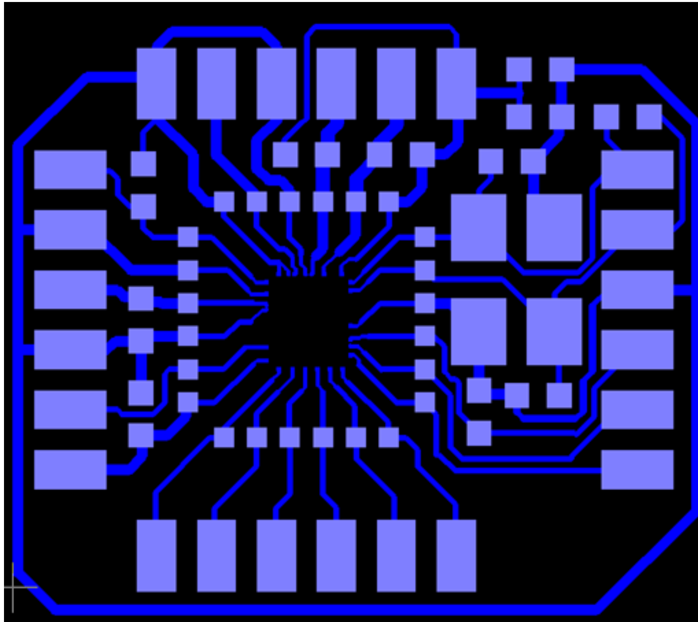


Figure 3.21: Test circuit design for the Nordic nRF2401A

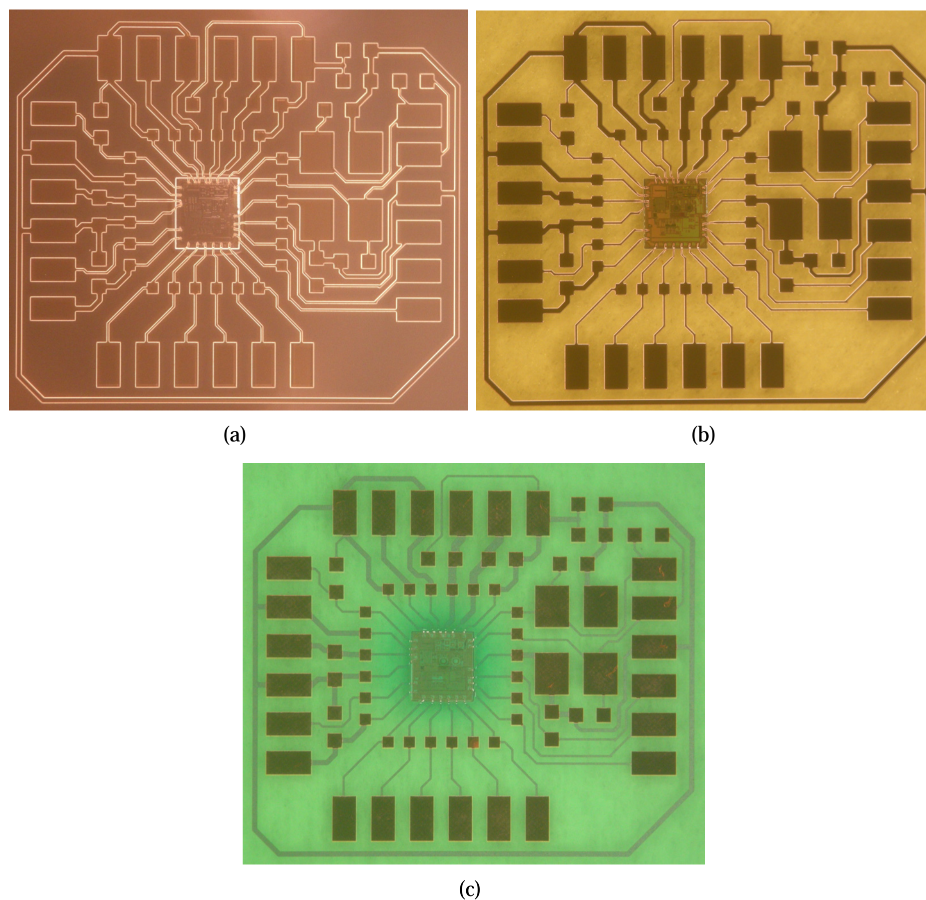
3.5.3 UTCP test sample production

The Nordic radio chips were available at IMEC Leuven only as bare, unthinned single dies. To be able to embed the devices as UTCP package, some preparatory process steps were necessary:

- application of under bump metallurgy (UBM) on single dies: an ENIG finish of the Al contact pads will prevent contact pad damage during the via drilling process (see UTCP integration of TI microcontroller)
- thinning down of the individual chips, from original die thickness down to 20–25 μm.

First 5 μm Ni and a Au flash was deposited on the Al contact pads using the CMST individual die ENIG plating process. Next, the radio devices were thinned down from about 250 μm to 25 μm, using the single die thinning process as described in Chapter 6, Section 6.3.3.

Finally the ultra-thin Nordic radio devices are UTCP integrated, following the optimized UTCP process flow (i.e. the same process as used for the reliability test samples, see Section 3.2.2). Different intermediate process steps during the UTCP production are shown in Figure 3.22.



(a) (b)

(c)

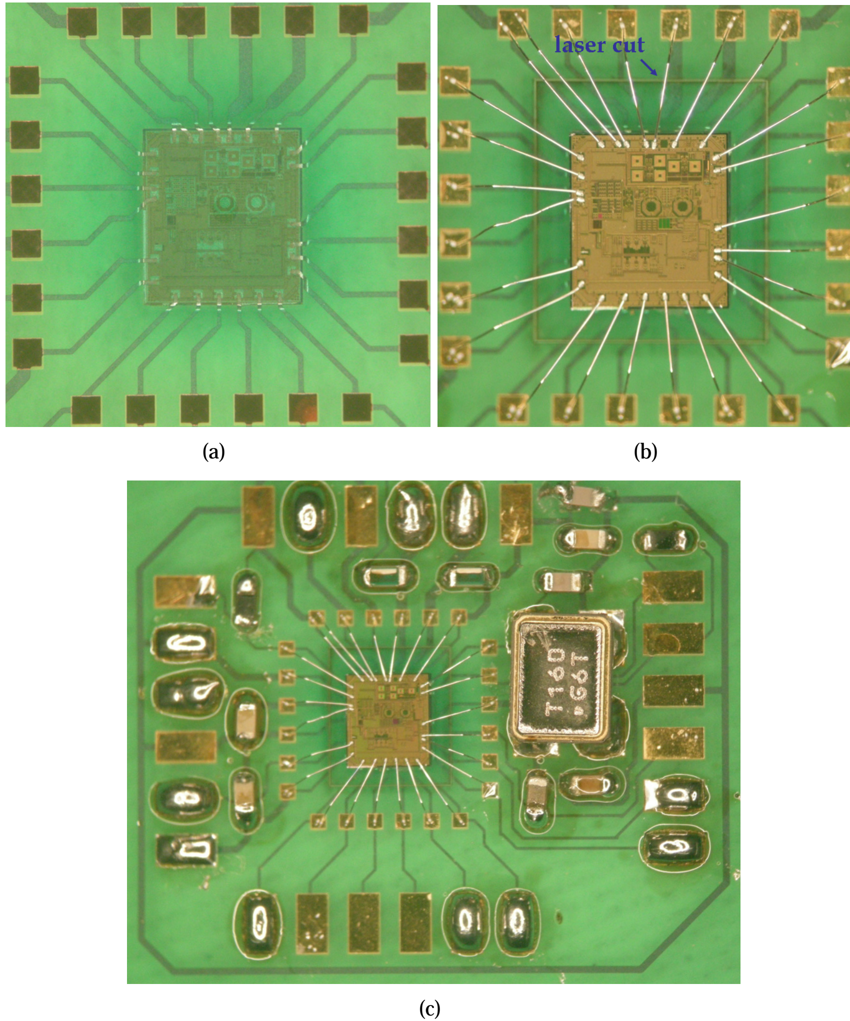
Figure 3.22: UTCP integrated Nordic radio device during different process steps: (a) lithography on sputtered TiW Cu layer, (b) etched metal interconnections and (c) solder mask cover layer

3.5.4 Testing and characterisation

On top of the UTCP packages, the SMD components were first solder assembled. This was done manually. Testing was done at IMEC Leuven and performance was compared with the existing rigid test set-up, using a packaged Nordic radio chip.

5 UTCP packaged radio chips were produced. The first tested sample showed a much lower transmission performance, compared with the rigid set-up. This 'limited' functionality was also compared with the behavior of the unthinned

naked dies. This is shown in Figure 3.23: the interconnections in the package to the embedded thinned radio chip are first cut through by laser, and an unthinned radio chip was mounted on top of the embedded thin die and wire bonded to the UTCP package. This unthinned functional radio showed similar performance as the embedded, ultra-thin radio chip.



(a) (b)

(c)

Figure 3.23: Comparison of functionality of a thinned, integrated radio device with an unthinned radio chip using the same test circuit: (a) original UTCP package, (b) unthinned radio chip wire bonded on the UTCP substrate (connections to the integrated device cut through by laser) and (c) test circuit with wire bonded radio device and SMD components

Closer investigations on other test assemblies using the bare Nordic nRF2401A radio die had shown in the meantime that the reason for this non-functionality is most likely to be found in the low yield of the radio chips on the purchased diced wafer. On the limited number of test assemblies, yield seemed to be around these orders of magnitude:

- around 1/5 of the dies are completely dead
- around 1/2 of the dies are 'functional' but with a terrible radio link quality, so in practice also not usable (this explains the poor transmission performance)
- only around 1/3 of the dies are good.

The other 4 UTCP packaged Nordic radio chips were also assembled and tested. One sample (out of 5 tested packages) showed perfect functionality, at least as good as could be achieved for a conventional packaged Nordic radio device: achieved line-of-sight range of at least 25 m with low error rate at 1Mbit/s with 0dBm power (characterization done by IMEC Leuven).

So the total yield on the tested UTCP samples was only 20 %, but this is most probably only due to the low yield of the available bare radio chips.

3.6 Thermo-mechanical simulations

The technological developments were also supported by FEM simulations in order to qualify the technology. These simulations were done by the colleagues of IMEC/MCP/HDIP group in Leuven.

At IMEC Leuven, the general FEM code Msc.Marc is used. It allows simulation of complex 3D structures for pure mechanical but also coupled phenomena as thermal-mechanical. FEM has been used to calculate the stresses induced in the UTCP caused by first processing succeeded by a mechanical bending [5, 6].

The first part of the FEM simulation is the deformation and stress calculation after processing: stress induced during processing is mainly due to CTE mismatches. Figure 3.24 shows the 2D FEM of the Ultra-Thin Chip Package. Both the polymer and BCB are cured at 350°C, so the whole structure (excluding the copper metallization) gets a cooling down from 350°C to 20°C. The silicon chip (169 GPa, 2.6 ppm/^{o}C) and the polyimide (8.5 GPa, 3 ppm/^{o}C) have almost the same coefficient of thermal expansion (CTE) so there will be not so much induced stress. However, the thin BCB (2.9 GPa, 42 ppm/^{o}C) layer has a much higher CTE which will cause high tensile stresses in the BCB layer itself. Figure 3.25 shows the real deformation after processing. Thanks to the almost similar CTE of Si and PI, the flexible package stays almost flat. In the BCB layer, a uniform 'tensile' stress equal

to 61 MPa is found. Near the chip edge, also tensile stress in the silicon chip is found (+74 MPa).

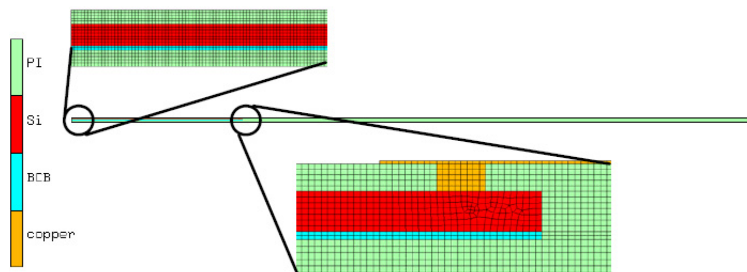


Figure 3.24: 2D FEM of the Ultra Thin Chip Package, different layers are: polyimide, BCB, Si and Cu

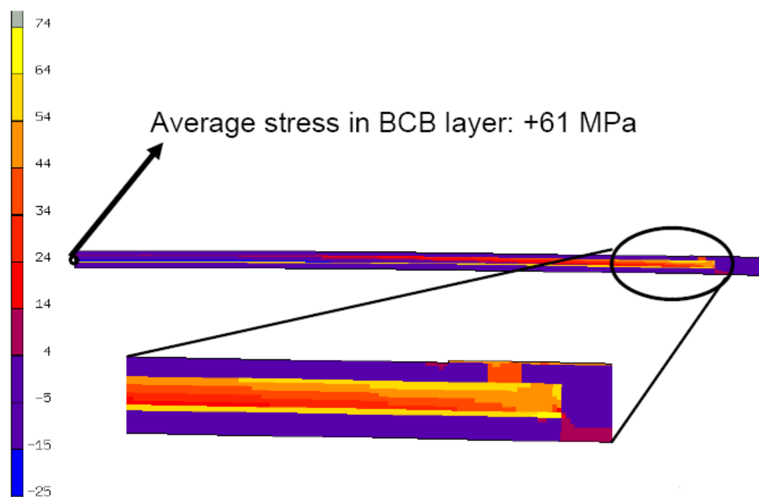


Figure 3.25: Deformation and in-plane stress (σ_x) in UTCP after processing

The second part of the FEM simulation was the mechanical bending of this UTCP. It is possible to manually bend this package with a curvature of about 5 mm without damaging the silicon chip nor the BCB layer. The FEM result is shown in

Figure 3.26. For the silicon chip, the maximum allowable tensile stress is around 300 MPa. For BCB, the ultimate tensile stress is 87 MPa. For the downward bending, a curvature of 5 mm is feasible, as it compensates the tensile stress in BCB by compressive stress. The stress in the silicon chip is near the maximum allowable stress. For the upward bending, it is much more critical, as additional tensile stress in the BCB layer is induced due to the upward bending.

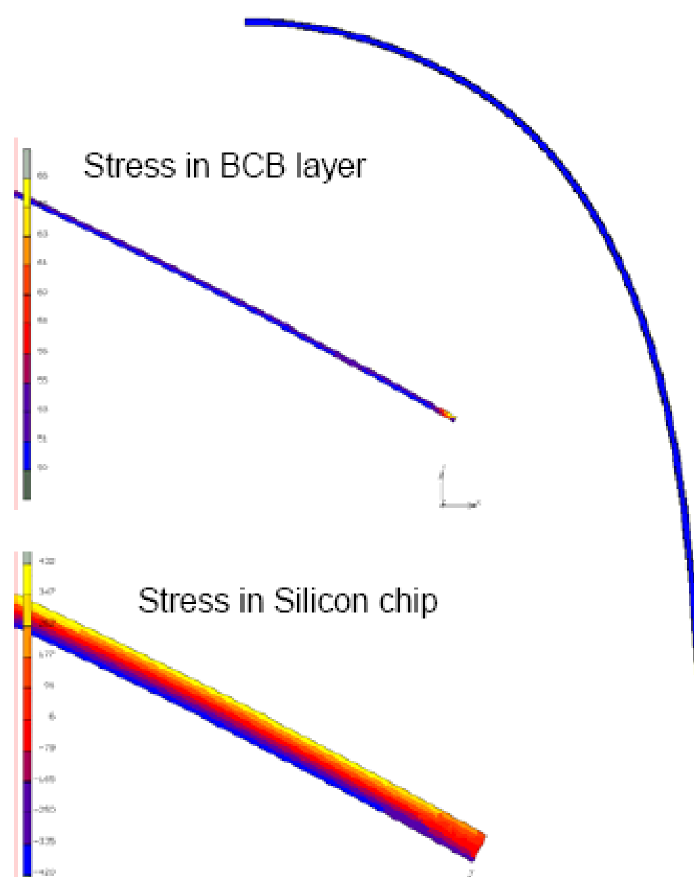
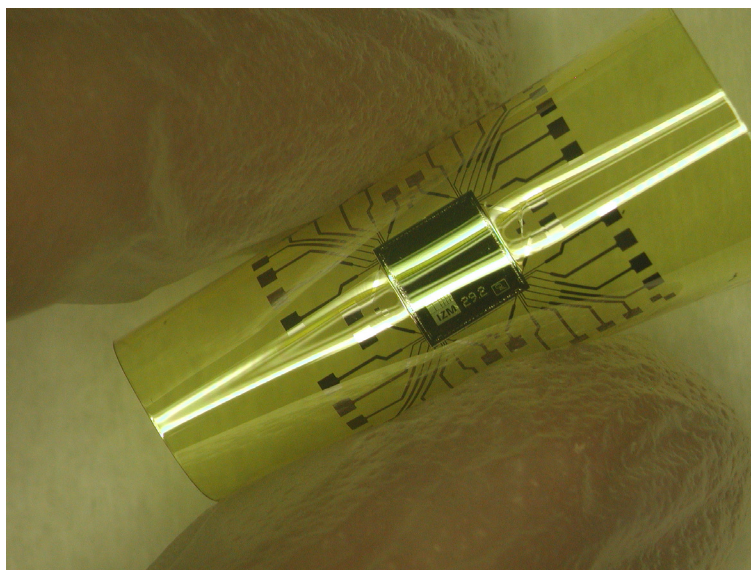


Figure 3.26: FEM of downward bending of the UTCP (curvature 5 mm)

Figure 3.27 shows the bendability of a UTCP packaged interconnection test chip. Initial bending test results are also presented in Section 3.4.5 above: functionality of a UTCP packaged microcontroller under bending (curvature $\cong$ 8 mm) is

demonstrated there.



(a)

(b)

Figure 3.27: Bendability of the UTCP

3.7 Conclusions

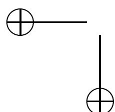
Feasibility tests were performed on UTCP packaged PTCK interconnection test chips. A dedicated test design allowed to characterize the via and daisy chain resistances.

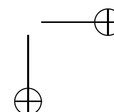
The preferred via technology for the UTCP is the CO_2 laser ablation followed by an RIE clean step. Reliability test samples were produced using this laser drilling technology. Typical via resistance values for the chip contacting are below 30 mΩ. Feasibility of the other via technologies is also demonstrated, with typical resistance values below 50 mΩ.

Different reliability investigations are reported. Test vehicles were subjected to thermal cycling test between -40°C and +125°C, temperature/humidity testing at 85°C/85 r.h., and to thermal ageing at 125°C and 150°C. No failures occurred during 1000 h storage at 85°C/85% relative humidity or during temperature cycling between -40°C and +125°C up to 1000 cycles. High temperature storage at 125°C indicated a serious increase in via resistance already after 250 h; during temperature storage test at 150°C some vias were already unmeaserable after 250 h. These bad results were not confirmed in a second study, using similar samples with the same layer build-up, but from a seperate batch. These samples passed the 1000 h storage at 125°C even without any increase in via resistance. After 1000 h of storage at 150°C, the via resistances increased to an average of 79.25 mΩ. Failure analysis on the failed samples, compared with the samples for the other batch (cross sections, EDX) only indicated the presence of Cu interconnects on the failed interconnection test chips.

The UTCP technology has also been demonstrated for the packaging of ultra-thin, functional devices. Bare TI microcontroller and Nordic radio devices were first thinned down, using the individual die thinning process described in Chapter 6. The thinned devices were next UTCP packaged, and functionality was demonstrated after embedding. UTCP embedded microcontrollers could be programmed (and retained their program). Extensive tests of the analog-to-digital converter of the embedded microcontrollers indicated that the UTCP performs only slightly worse than the naked thin die which was wire-bonded to a rigid PCB. These small deviations are limited and will have only little effect on the usability of the packaged microcontroller. Most probably they are caused by parasitics on the UTCP package. Also a UTCP packaged Nordic radio device showed perfect functionality after embedding, at least as good as could be achieved for a conventional package Nordic radio device.

Finally, also some FEM simulation results are included in this chapter. These simulations confirm the limited stresses introduced in the package during the processing. This is explained by the material selection: combination of the low CTE polyimide with the silicon material. Simulations on mechanical bending of the UTCP packages confirm the bendability of the UTCP packages.





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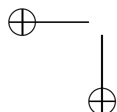
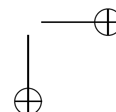



Chapter 4

Integration of active devices in flexible multilayer circuit boards

This Chapter demonstrates a technology for integrating functional active devices inside the inner layers of flexible multilayer circuit boards. The first part of this chapter introduces the concept of UTCP packages, 3D integrated in (multilayer) flex substrates. The second section gives a general overview of the typical different manufacturing process steps for commercial multilayer flex boards production. Next, a suitable process flow for the integration of UTCP packages in commercial flex multilayer laminates is presented, followed by the discussion of the embedding trials: starting with the integration of dummy packages, over the integration of interconnection test chips and concluding with the demonstration of a 3D integrated, UTCP packaged, functional microcontroller. Also some reliability investigations are discussed.

4.1 UTCP embedding concept

On typical flex substrates, only pure electronic assembly is performed up to flip-chip components. Embedding of passive or active components in flexible printed circuits is at least not state of the art. The presence of relatively large rigid components, only on front and back side of the flex laminate, is an important factor limiting not only the miniaturization, but also the mechanical flexibility of the circuits.

This chapter will present a technology for integrating thin, flexible UTCP packages inside flexible substrates. The extremely low package thickness of the UTCP

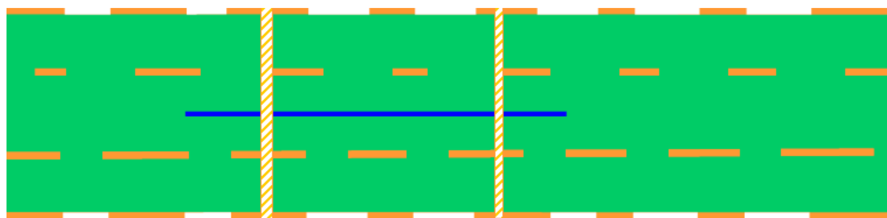


Figure 4.1: Concept for integrating the UTCP package in multilayer flex boards

packages, will enable for integrating packaged devices as an alternative for the direct integration of bare dies. UTCP packages will be laminated inside the inner layers of the multilayer boards, and connected to the wiring of the boards by means of through hole vias. This concept for the UTCP embedding in multilayer flex boards is shown in Figure 4.1. Of course, the integrated unit itself should be extremely thin, using ultra-thin interposer layers and chips.

After embedding, other components can be mounted above and below the embedded chip, leading to a high density of integration. In addition, the embedded thin silicon chip is mechanically flexible itself, leading to an increased flexibility of the resulting system.

This 3D approach for integrating UTCP packages, which serve as interposers, to be embedded in a conventional multilayer PCB or FCB, also offers some very interesting extra advantages compared with the different direct die embedding technologies:

More relaxed pitch Fine pitch interconnection to the chip is possible with the UTCP technologies (pitch down to 60 μm). If the UTCP is used for embedding into a printed circuit board or flex board, this leads to a high density interconnect area around the chip, built into a lower density, low cost substrate. A fan-out interconnection pattern on the UTCP package relaxes the alignment constraints for die embedding and excludes the need for using expensive fine pitch PCB or FCB.

Known Good Die UTCP packages offer the possibility for easy testing of the (ultra-thin) chip integration, thus avoiding KGD issues.

Stress relief Thermo-mechanical stresses in the thinned silicon die are minimized by selecting a polyimide that has a CTE close to that of silicon. (Thermo-mechanical simulation results are found in Chapter 3). In its function of intermediate fan-out package in 3D-stacks or embedded circuits, the UTCP can thus distribute thermo-mechanical stresses. This will prevent the introduction of very high stresses in the (ultra-thin) embedded silicon devices.

This 3D technology will be used for the integration of the functional TI microcontroller, MSP430F149, device for a wireless ECG application. The UTCP packaging of this microcontroller was already discussed in Section 3.4, and these UTCP packages will be integrated inside a standard double-layer flex PCB, with even smaller SMD components mounted above and below the embedded chip, realizing a fully functional, wireless biopotential system.

All technological development of this 3D integration technology is discussed below.

4.2 Multilayer flex board manufacturing process flow overview

This section depicts a very short overview of some typical processing steps for the manufacturing of multilayer flex boards [1].

Multilayer flexible circuits can have three or more layers of metal conductors. Over the years, they have become more popular as a packaging scheme in some applications in spite of their higher relative cost. Unlike single-sided and double-sided flex circuits, which can be processed in a reel-to-reel fashion, multilayer circuits are typically only fabricated in panel form.

There are many similarities between multilayer flexible circuits and standard rigid PCBs, but the actual processing of multilayer flex is often much more challenging. In flex multilayer board processing, flexible laminates that are to be the circuit layers, are provided with tooling holes. Drilling of holes in what will be flexible appendages or breakouts may also occur at this time. The layers are then imaged and etched (and possibly plated through, depending on the design needs). Coverlayers can be laminated to the etched patterns while providing access to interconnect points through openings in the coverlayer.

The flex circuit layers are then laminated together using flexible bondplies. The outermost layers are commonly still coated fully with copper foil. The panel is drilled, and the holes are next cleaned using a plasma process or other suitable method and then metallized by electroless copper deposition or an other acceptable technique, then electroplated with additional copper, either to meet requirements for full plating or simply to 'lock' the electroless plating on. For an additive process, a negative image of the outer circuit pattern is next applied to the copper foil. The open area or circuit pattern is plated with an etch-resistant metal such as tin or tin-lead. The resist image is then stripped and the pattern etched from the background foil. The metal etch resist is stripped from the circuit and the surfaces cleaned, providing a bare copper surface. Next, an outer coverlayer is laminated to the circuits, providing openings to the interconnection features of interest. A solder coating process may be prescribed at this time. If not soldered, the circuit

is punched or cut from the laminate.

Some alternative methods and approaches for producing multilayer flex circuits include sequential lamination, and solid state in-diffusion.

4.3 Process flow for UTCP package integration in FCB

The first step towards the integration of UTCP packages inside multilayer flex boards was the establishment of a suitable process flow. This process flow was discussed together with ACB, a Belgian flex manufacturer and project partner within the European SHIFT project.

The proposed process flow for the 3D integration of ultra thin UTCP package in the inner layers of a multilayer flex substrate is given in Table 4.1.

This process flow was optimized for the integration of the packages in between two flex panels. Integration in multilayer substrates will be very similar.

The principle is as follows: the UTCP packages are aligned and fixed (heat tack) on a patterned inner layer of the multilayer substrate. Before the mounting of the package, first an adhesive sheet is prelaminated on the patterned inner layer. The packages are fixed by heat tack on this panel, before the multilayer stack is built-up and laminated together using exactly the same process as for conventional multilayer board production.

Processing was optimized and characterized for the integration of different types of UTCP packages (dummy UTCP, interconnection test chips, as well as for UTCP embedded TI microcontroller) in between two commercial flex panels.

ACB uses 305 x 457 mm^2 polyimide laminates, 25 μm Kapton polyimide + 18 μm Cu: type Pyralux AP-8515 (single sided version) or Pyralux AP-8525 (double sided version). Adhesive material are Pyralux LF-0100 sheets.

First a flexible (double sided) laminate is patterned at only one side (using photolithography and etching) and an adhesive sheet is laminated on top of the patterned side. The pattern contains also a copy of the contact pad layout as on the UTCP fan out. Next, the UTCP package is aligned manually with it contacts on the alignment contacts of the panel and it is fixed by heat tack (using a solder iron). Once the package(s) are fixed on the adhesive top layer, a single sided laminate is laminated on top of these packages. Next, the through holes are drilled, for the interconnection between both sides of the panel, but also for the interconnections to the UTCP contact pads.

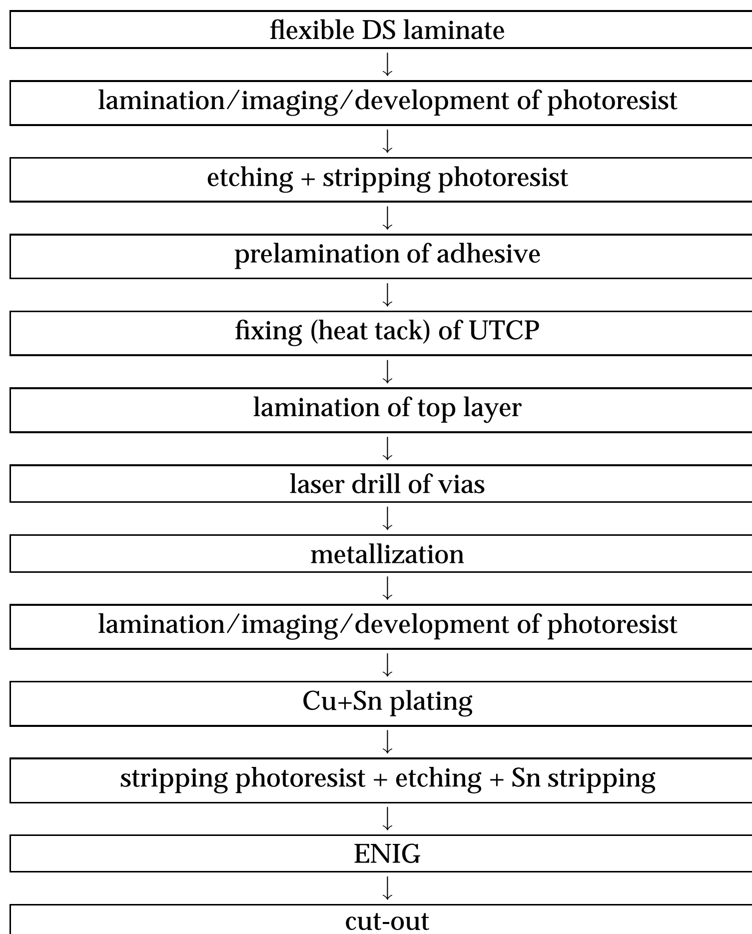


Table 4.1: Process flow for UTCP embedding in multilayer flex boards

Once through holes are opened, the holes are cleaned by plasma treatment and a Cu seed layer is deposited. Next, lithography is done and Cu + Sn are pattern plated. After plating, the photoresist is stripped, the panel is etched (removing the Cu) and finally also the Sn etch mask is stripped. The panels are finished with solder mask and ENIG (electroless nickel / immersion gold) deposition.

Note also that all alignment during this processing (eg. during through hole drilling, patterning, etc.) is done based on mechanical tooling holes, foreseen at the side of the each flex panel.

4.4 Technology demonstration

4.4.1 Introduction

This technology was demonstrated in different steps. First integration trials were done using dummy UTCP package, in order to demonstrate the feasibility of embedding small flex substrates in between the large ACB flex panels. Special points of interest are the alignment and the metal interconnection between the UTCP and the wiring of the flex multilayer. Also reliability investigations of the interconnections are included.

In the next step, the 3D integration of packages in the (flex) multilayers is demonstrated for a UTCP packaged interconnection test chip (similar test packages as presented in Chapter 3). Via resistance values on the package are characterized before and after 3D embedding, to check if the integrated devices and their interconnection pass the ACB embedding process flow successfully.

4.4.2 Interconnection test

First embedding trials at ACB aimed for the demonstration of the concept of integrating small UTCP flex substrates in between large ACB flex sheets. Also the possibility for integrating samples with ENIG finish was investigated.

Design

A test vehicle was designed for embedding small 2 x 2 cm^2 UTCP packages in between large conventional flex panels. The design is shown in Figure 4.2. The metallization on the UTCP package is indicated in blue, the metallization on the outer layer of the conventional flex is indicated in red.

The design of the UTCP package includes also a fan-out to a test chip, but this part of the design will not be used. The most relevant part of the design is the daisy chain interconnection pattern between the package and the outer layers of the flex substrates. This daisy chain, containing 164 through holes, will be used to characterize the interconnections between package and substrate. The design also provides some pads to solder mount SMD components on top of the integrated package (size: 0402 and 0603).

Of course this design was based on the design rules provided by ACB:

- via drill size: 200 μm
- min. diameter via land pads: 300 μm (= contact pad size on UTCP package)
- min. via land pitch: 400 μm (= contact pad pitch on UTCP package).

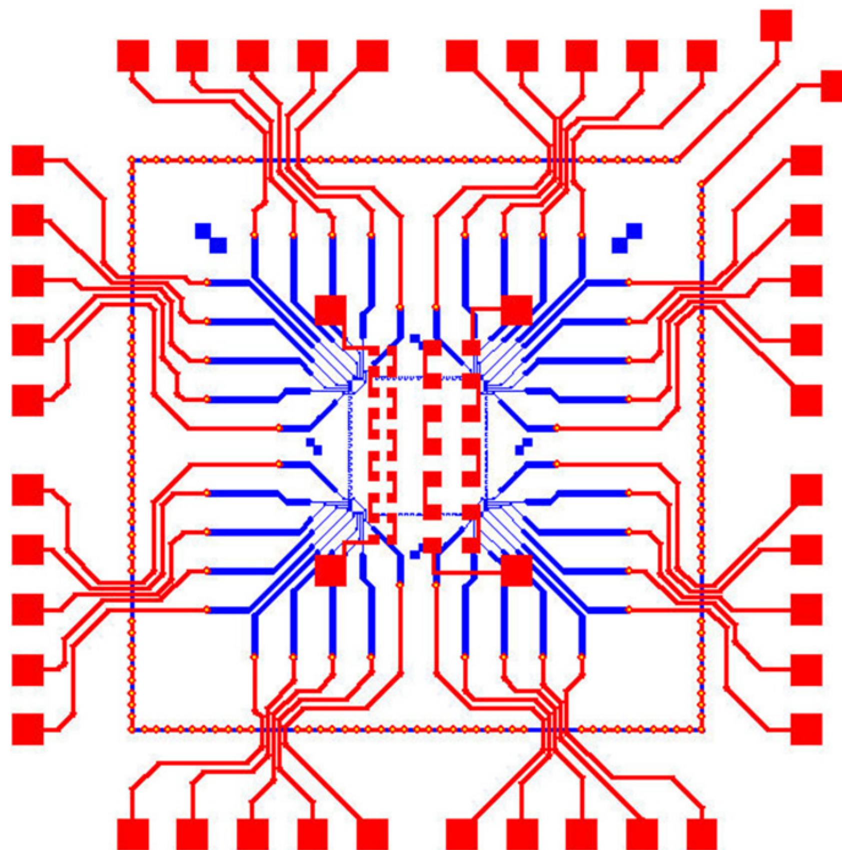


Figure 4.2: Test design for dummy package embedding in large ACB flex panels

Dummy packages

First dummy UTCP packages were produced using the UTCP technology presented in Chapter 2. This production process includes several spincoating steps, dry etching, sputter deposition of a TiW Cu seed layer and Cu pattern plating. The total polyimide thickness is 40 μm (identical to conventional UTCP package, see cross section Figure 2.4). Cu thickness on these samples ranged from 3.5 up to 13 μm, in order to check minimum required Cu thickness on the UTPC to ensure nice through hole interconnection to the package after embedding.

More dummy packages were produced by ACB, on standard single sided flex foil, Pyralux AP-8515. These packages had the same design and the same dimensions (2 x 2 cm^2) as the spin-on PI dummies. These packages have 6 μm Cu thickness. Half of the samples had also an extra ENIG finish (8 μm Ni + 0.05 μm Au) on top of the 6 μm Cu. These ENIG finished samples are used to check if the presence of the Ni and the Au reduces through hole metallization quality.

ACB integration

The dummy packages were integrated inside the flex multilayer substrates at ACB, following the process flow described in Table 4.1.

Some illustrative pictures of the different individual process steps of the integration process are given in Figures 4.3 - 4.8. Figure 4.3 shows the placement of 5 2 x 2 cm^2 dummy UTCP packages spread over the large ACB flex sheets (panel size: 305 x 457 mm^2).

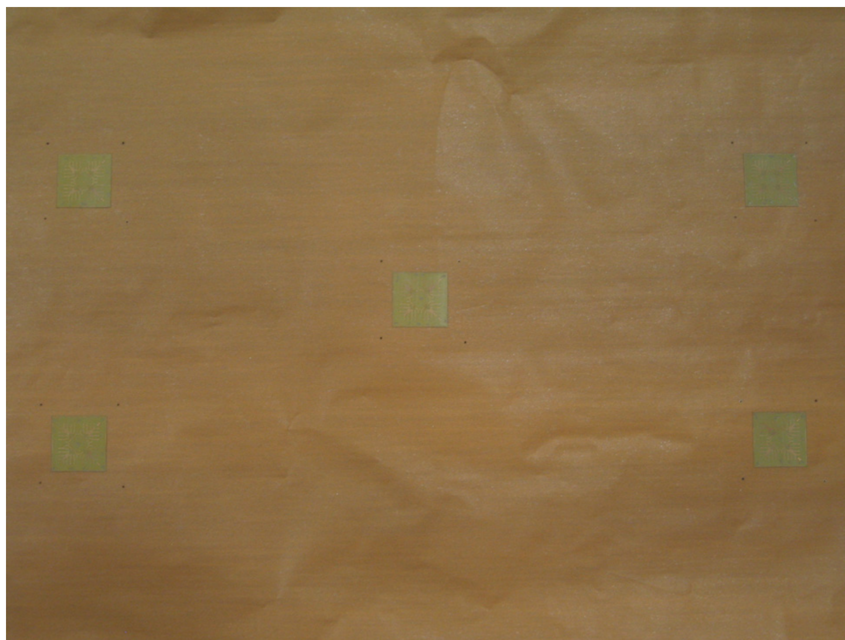


Figure 4.3: Placement of 5 small, 2 x 2 cm^2, UTCP dummy packages all over the large commercial ACB flex sheets (panel size: 305 x 457 mm^2)

On top of these a next single sided flex substrate is laminated, using a Pyralux LF-0100 adhesive sheet. Following pictures illustrate the different process steps:

- through hole laser drilling (Figure 4.4)
- imaging of the outer Cu layers (Figure 4.5)
- Cu + Sn plating and photoresist removal (Figure 4.6)
- Cu seed layer removal (Figure 4.7)
- ENIG finish (Figure 4.8).

All these pictures are courtesy of ACB.

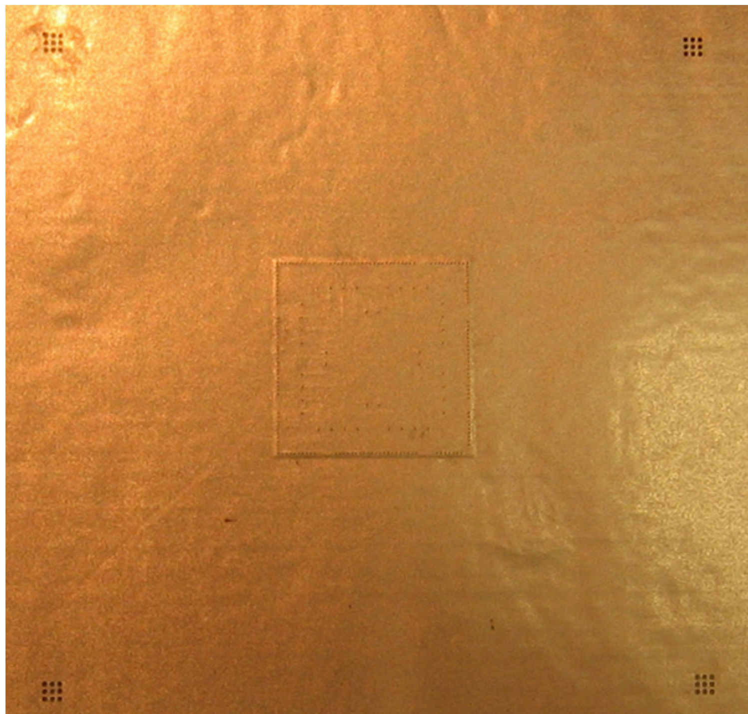


Figure 4.4: Via hole drilling in the flex boards

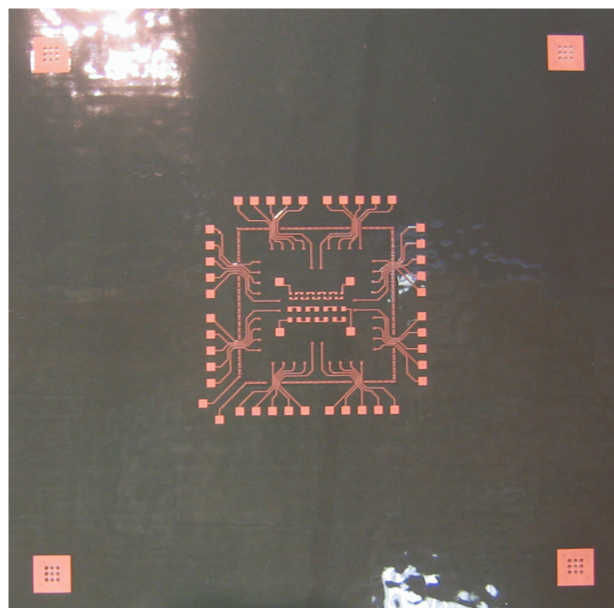


Figure 4.5: Imaging of one embedded UTCP package

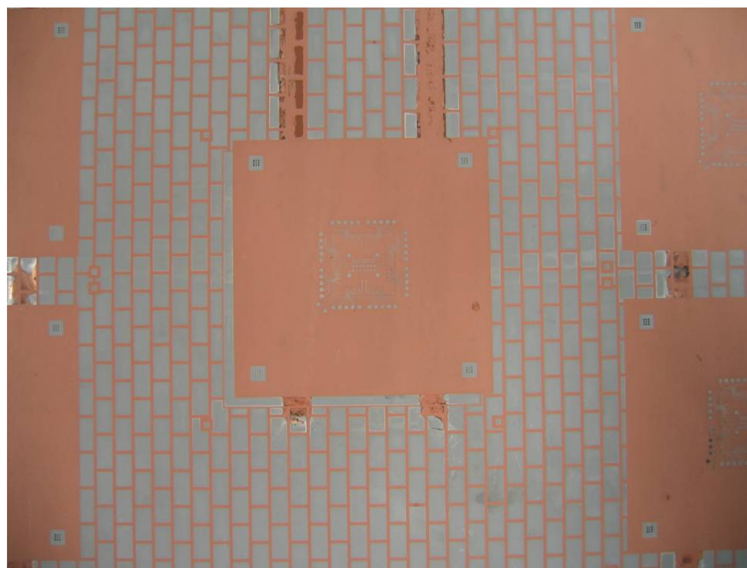


Figure 4.6: Plated flex board

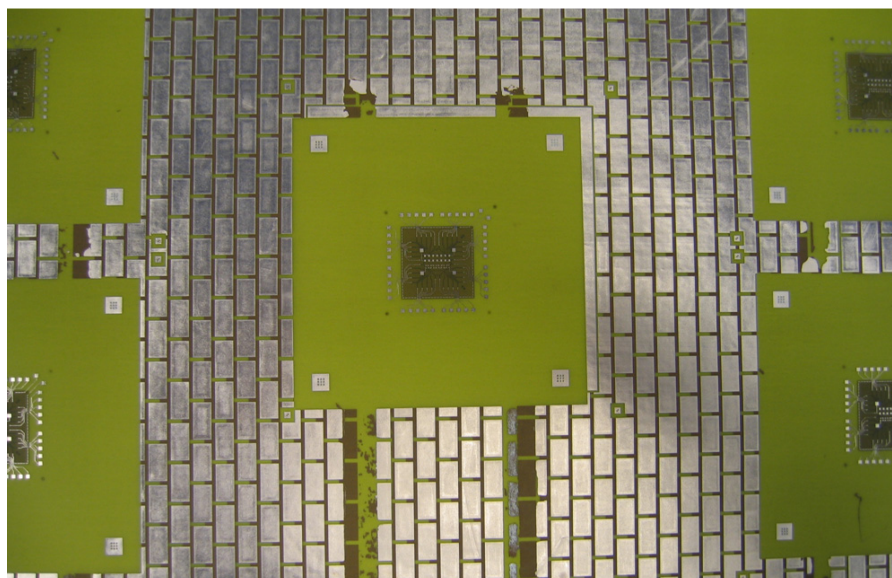


Figure 4.7: Etching of the flex panel

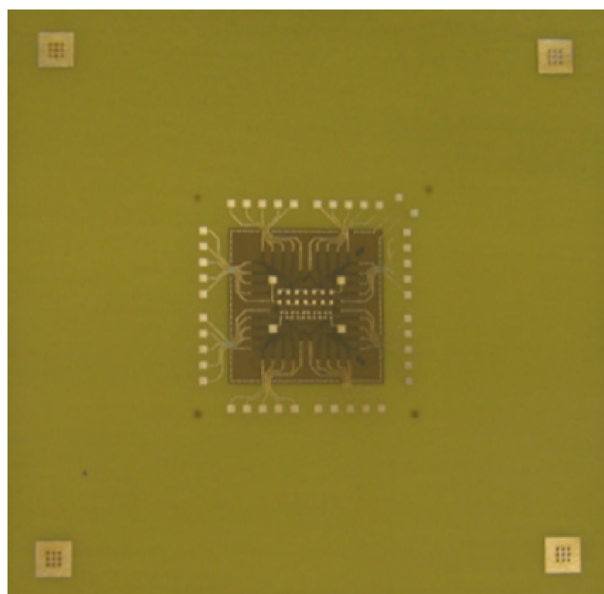
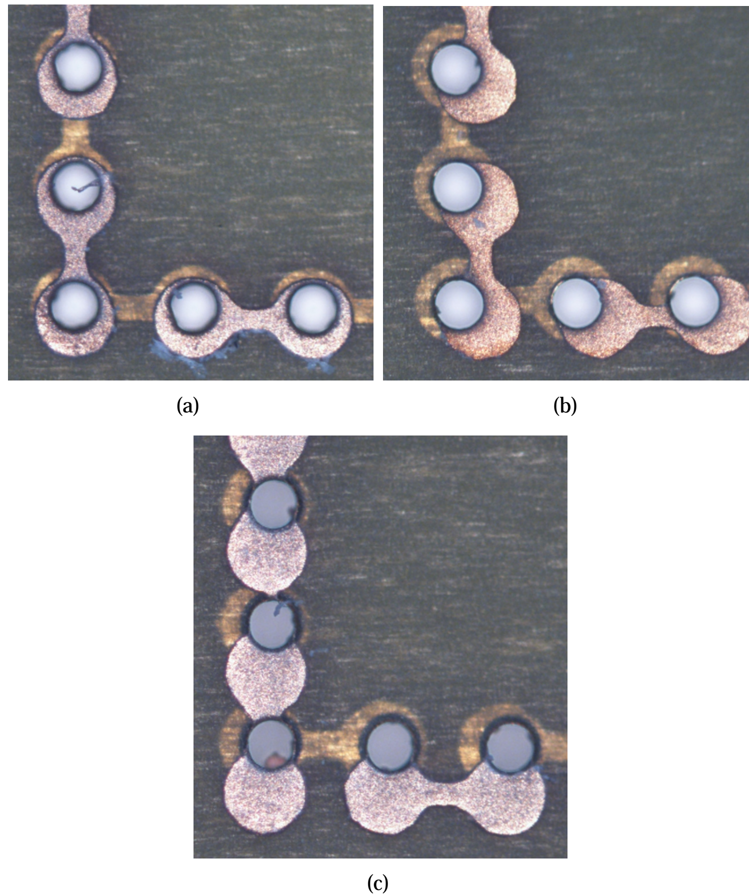


Figure 4.8: Finally an electroless NiAu finish is applied

Characterization

10 spin-on polyimide based samples, with variable Cu thickness ranging between 3.5 up to 13 μm, were successfully integrated in between 2 single sided flex substrates. The resistance of the daisy chain containing 164 via interconnections was measured. Values ranged from 0.9–3 Ω, also after reflow of the SMD components. This demonstrated that even the 3.5 μm Cu layer on the UTCP can be sufficient to ensure the through hole interconnections. The variation of daisy chain resistances between 0.9 and 3 Ω could not be explained by the varying Cu thickness, but was due to the poor alignment of the through hole drilling. This is illustrated in Figure 4.9. These first samples were fixed on the inner layer of a single sided flex sheet based on pre drilled laser holes.



(a) (b)

(c)

Figure 4.9: Variation in daisy chain resistance is depending on the alignment

Two of those integrated dummy samples were available at CMST. These two samples are also used for reliability testing, see below (Section 4.4.3). The resistance value of the daisy chains is given in Table 4.2.

The alignment issue has been solved by ACB by the introduction of an extra Cu layer, on which the copper pads of the UTCP are present. These pads are used for alignment during placement. (As presented in the optimized process flow, see Table 4.1).

The other dummy packages were produced by ACB on standard single sided flex foil, Pyralux AP-8515. These packages have the same design and the same dimensions (2 x 2 cm^2) as the spin-on PI dummies. Cu thickness on these samples is 6 μm. Half of the sample also have ENIG finish (8 μm electroless Ni + 0.05 μm immersion Au). The daisy chain measurements on these samples are listed in Table 4.2. Average DC value for the samples having only Cu is 1.35 Ω, and for the ENIG finished samples 1.54 Ω. This indicates that an extra ENIG finish on the UTCP packages does not cause many problems during the 3D integration.

substrate	metallization	resistance [Ω]
spin-on PI	7 μm Cu	1.24
spin-on PI	12.5 μm Cu	1.22
Pyralux AP-8515	6 μm Cu	1.23
Pyralux AP-8515	6 μm Cu	1.39
Pyralux AP-8515	6 μm Cu	1.44
Pyralux AP-8515	6 μm Cu + 8 μm ENIG	1.53
Pyralux AP-8515	6 μm Cu + 8 μm ENIG	1.54
Pyralux AP-8515	6 μm Cu + 8 μm ENIG	1.56

Table 4.2: Overview of typical daisy chain resistance values for the different integrated dummy UTCP packages

ACB also checked through hole plating quality by cross sections. Figure 4.10 shows the through hole metallization to an embedded dummy package, with 12 μm Cu metal. About 6 μm Cu was deposited in the via and also about 7 μm ENIG was deposited.

Figure 4.11 shows a through hole interconnection to an integrated dummy UTCP, having also ENIG finish. The extra ENIG finish (8 μm Ni + 0.05 μm Au) did not cause any problem during through hole plating.

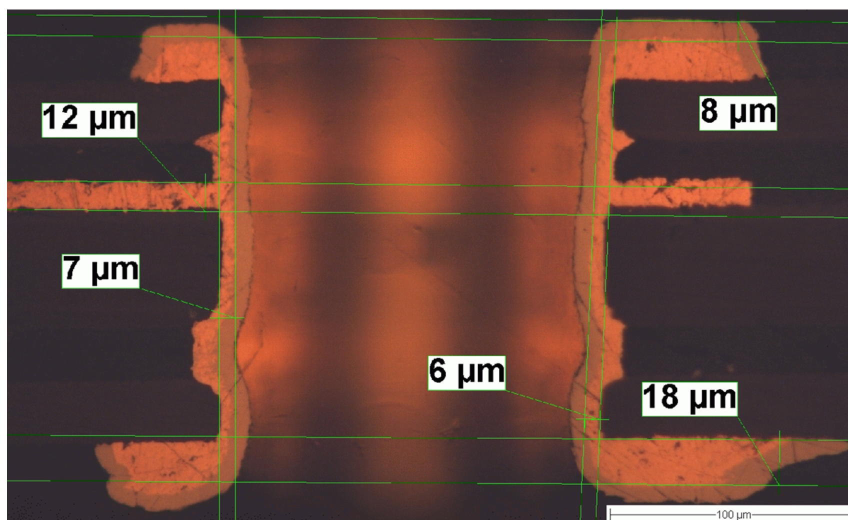


Figure 4.10: Cross section of metallised through hole via connection to a UTCP package, embedded in double sided flex substrate, embedded sample had 12 μm Cu metallization (picture courtesy of ACB)

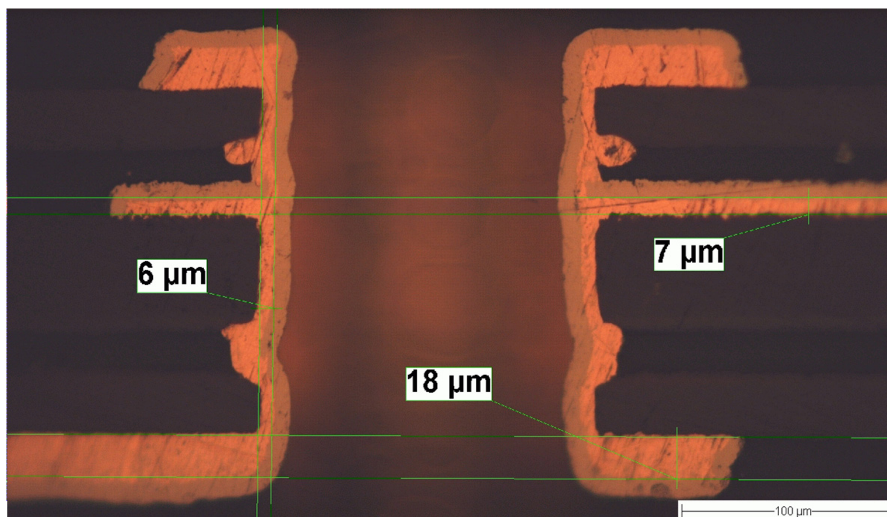


Figure 4.11: Cross section of metallised through hole via connection, embedded sample had Cu metallization and NiAu finish (picture courtesy of ACB)

4.4.3 Reliability investigations

This section describes the reliability testing of the interconnections between the embedded UTCP and the FCB. Test vehicles were subjected to thermal ageing at 150°C, to thermal cycling test between -40°C and +125°C and to temperature/humidity testing conditions at 85°C/85 r.H.

Thermal ageing

Two samples were subjected to high temperature storage at 150°C. The daisy chains (with 164 vias) have been measured after specified periods to characterize the interconnections and monitor degradation effects. Both samples passed the 1000 hours of thermal ageing with only a low increase in via resistance. The measurement results are shown in Figure 4.12 and Table 4.3.

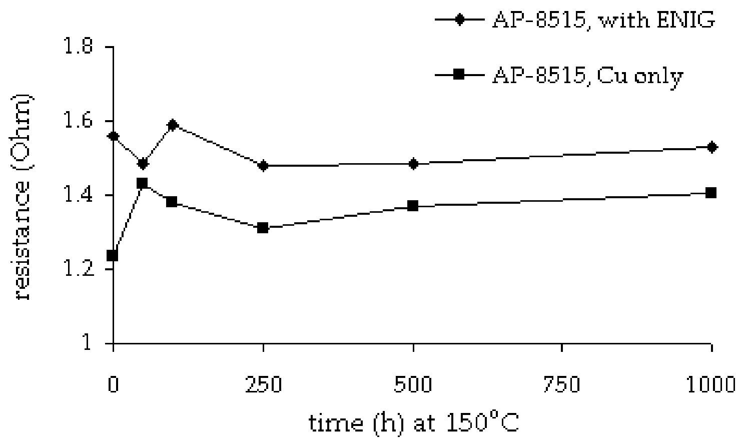


Figure 4.12: Daisy chain resistance value per sample under high temperature storage up to 1000 hours at 150°C

substrate	metallization	resistance [Ω]	
		initial value	after 1000 h
Pyralux AP-8515	6 μm Cu	1.23	1.40
Pyralux AP-8515	6 μm Cu + 8 μm ENIG	1.56	1.53

Table 4.3: Daisy chain values after 1000 h of high temperature storage, compared with the initial values

Humidity storage

Three different samples were stored at 85°C and 85% relative humidity, up to 1000 h. Daisy chains were measured at specified periods. All samples passed the 1000 hours without any failure. Only one sample showed a small increase in daisy chain resistance.

The measurement results are depicted in Figure 4.13 and Table 4.4.

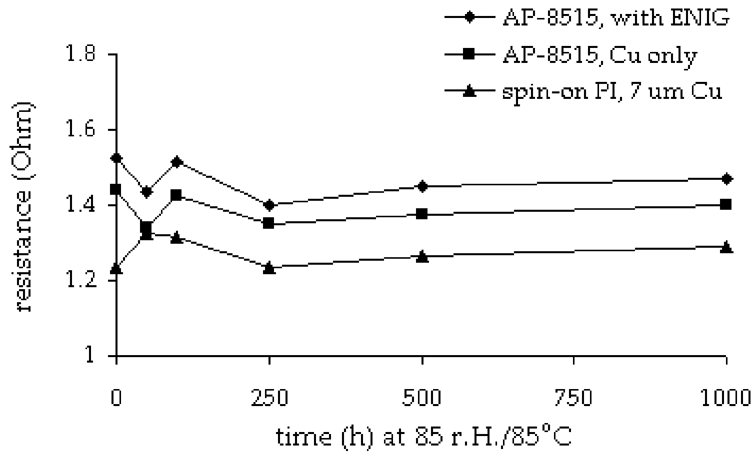


Figure 4.13: Daisy chain resistance value per sample under hot/humidity storage up to 1000 hours, at 85°C/85 r.h.

substrate	metallization	resistance [Ω]	
		initial value	after 1000 h
spin-on PI	7 μm Cu	1.24	1.29
Pyralux AP-8515	6 μm Cu	1.44	1.40
Pyralux AP-8515	6 μm Cu + 8 μm ENIG	1.53	1.47

Table 4.4: Daisy chain values after 1000 h temperature/humidity testing at 85°C/85 r.H., compared with the initial values

Thermal cycling

Thermal cycling test was done on three different test samples. The integrated dummy UTCP packages were exposed to 1000 cycles between -40°C and +125°C. Conditions are the same as discussed in Section 3.3.1. Total cycle time is 30 minutes and the temperature profile for 1 thermal cycle can be found in Figure 3.5.

Also these daisy chain interconnections reached the 1000 cycles. Even a small decrease in resistance after 1000 cycles was noted. Results are depicted in Figure 4.14 and Table 4.5.

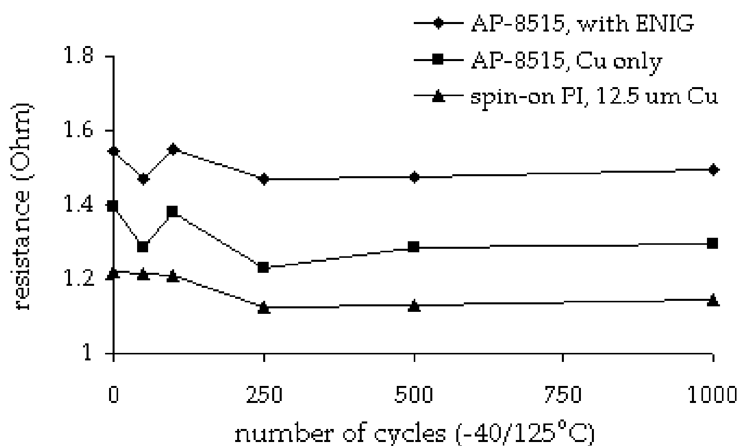


Figure 4.14: Daisy chain resistance value per sample under thermal cycling until 1000 cycles, between -40°C and +125°C

substrate	metallization	resistance [Ω]	
		initial value	after 1000 cycles
spin-on PI	7 μm Cu	1.22	1.15
Pyralux AP-8515	6 μm Cu	1.39	1.30
Pyralux AP-8515	6 μm Cu + 8 μm ENIG	1.54	1.50

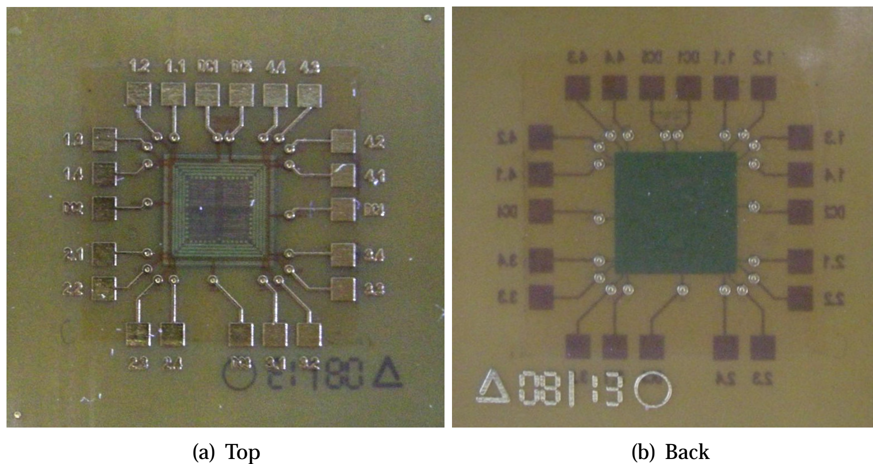
Table 4.5: Daisy chain values after 1000 thermal cycles between -40°C and +125°C, compared with the initial values

4.4.4 3D integrated interconnection test chip

The next step for the technology demonstration was the study of the impact of the integration process on the interconnections on the UTCP packages. Therefore a UTCP packaged interconnection test chip is integrated inside a multilayer flex substrate by ACB, following the optimized process flow given in Table 4.1.

These interconnection test vehicles were presented in Chapter 3, and the design is shown in Figure 3.3. The embedded package is connected to the wiring of the flex substrate by metallized through hole interconnects, drilled through the 400 μm diameter sized UTCP contact pads. The result after 3D integration is shown in Figure 4.15.

The top layer of the flex substrate provides a fan-out of UTCP contact pads to 1 x 1 cm^2 contacts.



(a) Top (b) Back

Figure 4.15: 3D integrated interconnection test chip

Via resistance values of the UTCP integrated interconnection test chip are characterized, before and after 3D embedding. The results are depicted in Table 4.6.

These measurements demonstrate that the 3D embedding of the UTCP package did not have any significant influence on the connections to the integrated device.

measured via	resistance before embedding [mΩ]	resistance after embedding [mΩ]
4PT1	47.0	46.0
4PT2	47.1	45.0
4PT3	45.4	44.4
4PT4	46.7	47.0
average	46.55	45.6

Table 4.6: 4PT measurement results on UTCP embedded interconnection test chip, before and after integration inside multilayer flex board

4.5 Functional ECG demonstrator

4.5.1 Introduction

This section presents the functional demonstration of the UTCP technology: the integration of UTCP packaged functional devices in the inner layers of multilayer FCB.

UTCP packaging of functional devices was successfully demonstrated for a TI microcontroller, MSP430F149, and the 2.4 GHz low power radio Nordic, NRF2401A, in Chapter 3. Such UTCP packaged functional dies will now be further 3D integrated in the inner layers of conventional FCB or PCB, using the process flow given in Table 4.1. Feasibility of this integration process has been demonstrated in the section above, for UTCP packaged interconnection test chips.

This section now demonstrates the 3D integration of functional microcontroller device for a wireless ExG application. Starting point is an existing, functional ExG circuit, fabricated and tested on conventional double sided flex substrate. This demonstrator uses an MSP430F149 TI microcontroller, wire bonded on the substrate for this double sided flex version. This Texas Instruments MSP430F149 low-power microcontroller, thinned down to 25 micron thickness and embedded in a flexible ultra-thin chip package, can in turn be embedded inside a standard double-layer flex PCB.

Also SMD components can be mounted above and below the embedded chip, leading to a high density of integration. In addition, the UTCP packaged thin silicon chip is mechanically flexible itself, leading to an increased total flexibility of the resulting system.

Finally the functionality of this ExG substrate including 3D integrated microcontroller, is successfully demonstrated and compared with the functionality of the similar flex circuit with the wire bonded microcontroller.

4.5.2 ExG demonstrator

The demonstrator consists of a high-density flexible ExG circuit for personal health or wellness applications. IMECs ExG system is a bio-potential wireless sensor node, able to monitor the vital body signs provided by portable electrocardiogram (ECG, which monitors the heart activity), electromyogram (EMG, which monitors muscle contraction) and electroencephalogram (EEG, which monitors brain waves). The system collects and processes data from (external) human body sensors and wirelessly transmits the data to a central monitoring system. Small size and low power consumption of the system enables non-invasive and ambulatory monitoring of vital body parameters.

The block scheme of e.g. an EMG circuit is given in Figure 4.16. The system uses IMECs proprietary ultra-low-power bio-potential readout ASIC (application specific integrated circuit) to extract the bio-potential signals produced during the ECG, EMG or EEG measurements. The low power microcontroller MSP430F149 drives the bio-potential chip, also digitalizes the samples with its A/D converter. The signals are finally sent by the 2.4GHz low power radio Nordic NRF2401A using a coplanar antenna. Information can be transmitted to a pc by a 'USB stick' receiver for visualization and recording.

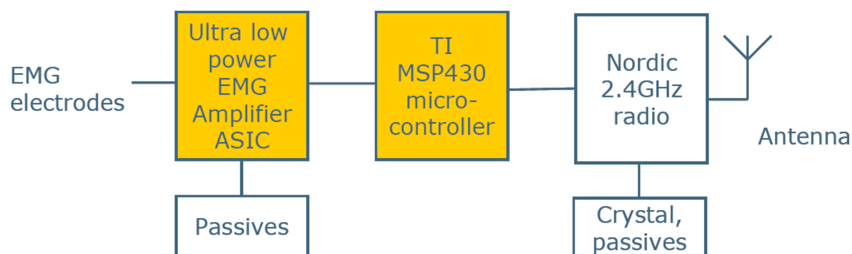
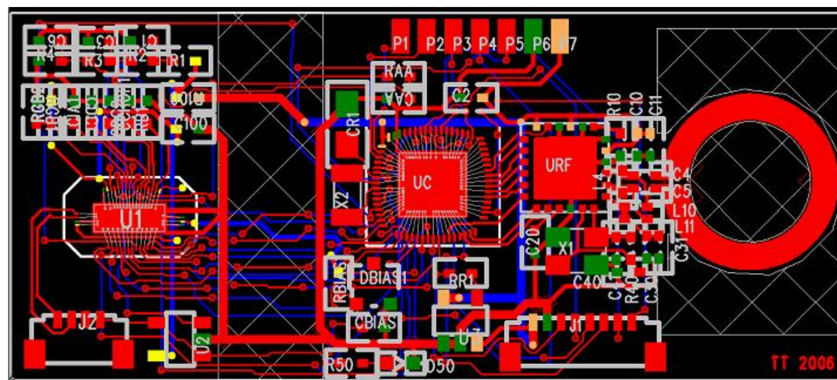


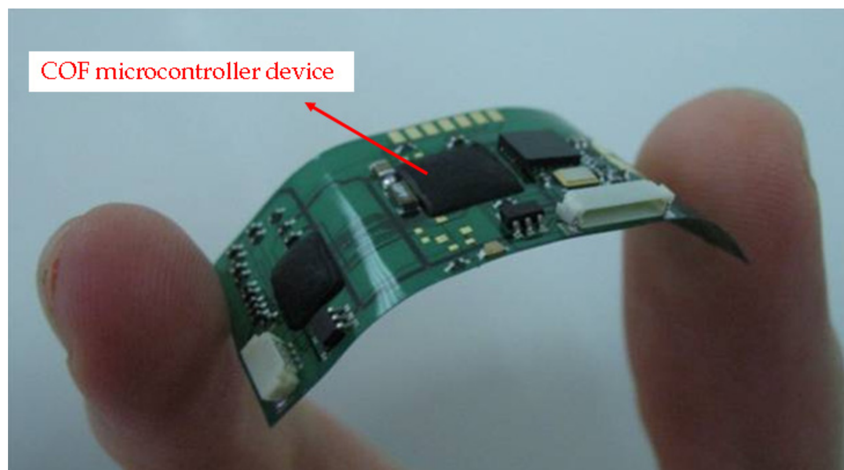
Figure 4.16: Block scheme of an EMG circuit

4.5.3 (Re)design

Starting point for the redesign of this ExG demonstrator was an existing realization on double sided flex substrates. This double sided flex realization has been subject of a Master Thesis, see [2]. The layout and the realization of the demonstrator is shown in Figure 4.17.



(a) Design



(b) ExG demonstrator on double sided flex substrate

Figure 4.17: Design and realization of ExG demonstrator on double sided flex substrate

In this design the microcontroller design is mounted by wire bonding on the flex substrate (Chip on Flex - CoF). This is also visible in the design: component indicated by 'UC'.

In the updated design this microcontroller is removed and embedded inside the flex substrate, see Figure 4.18. The embedded microcontroller will be connected to the wiring of the board by through hole interconnects. The UTCP package includes a fan-out of the 64 contacts of the microcontroller device to contacts of 400 x 400 μm^2 contacts with pitch of 500 μm, see small fan-out on Figure 3.13. On the design of Figure 4.18 only the 9 x 9 mm^2 square of the 400 x 400 μm^2 contacts are visible (in the center area of the layout).

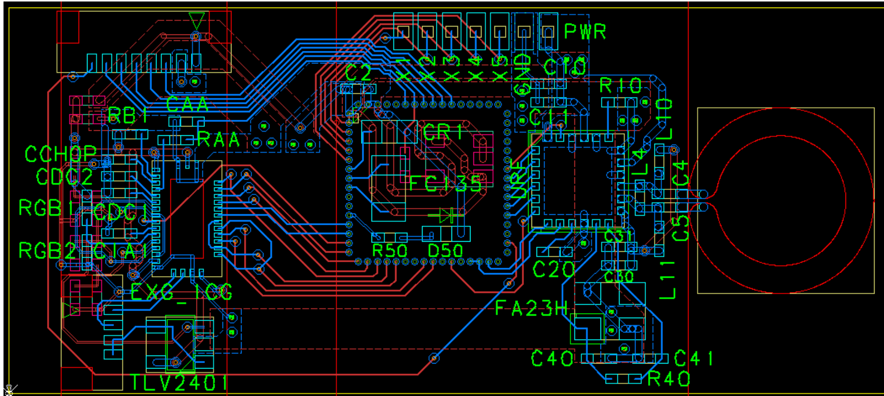


Figure 4.18: Design of ExG substrate with 3D integrated microcontroller

The updated layout has the same dimensions as the double-sided layout (21 x 47 μm^2), also the same loop antenna design is used. Small SMD components are also placed on top and bottom of the integrated chip.

4.5.4 Demonstrator production

Demonstrator production includes different process steps:

- UTCP packaging + testing of the ultra-thin microcontroller
- flex substrate production, with embedded microcontroller in the inner layers
- assembly of the components on the flex substrates.

UTCP integrated microcontroller

The UTCP integration of the Texas Instruments microcontroller MSP430F149 was presented in Section 3.4. Starting from the naked individual dies, NiAu bumps are deposited using the individual die bumping process. The individual chips are thinned down starting from the initial die thickness of 300 μm down to 25 μm, using the developed individual chip thinning process as discussed in Chapter 6. Finally, these very thin, functional microcontroller devices are embedded as an Ultra-Thin Chip Package.

This UTCP packaged microcontroller could easily be tested after assembly, but before release from its carrier. After testing the UTCP packaged microcontrollers are cut out from the glass substrates, resulting in +/- 1 x 1 cm^2 square UTCP packages.

Flex substrate production

In the next step the UTCP packaged microcontrollers are integrated in the inner layers of the multilayer flex substrates at ACB. The process flow is presented in Table 4.1. The double sided flex substrate with embedded microcontroller is shown in Figure 4.19.

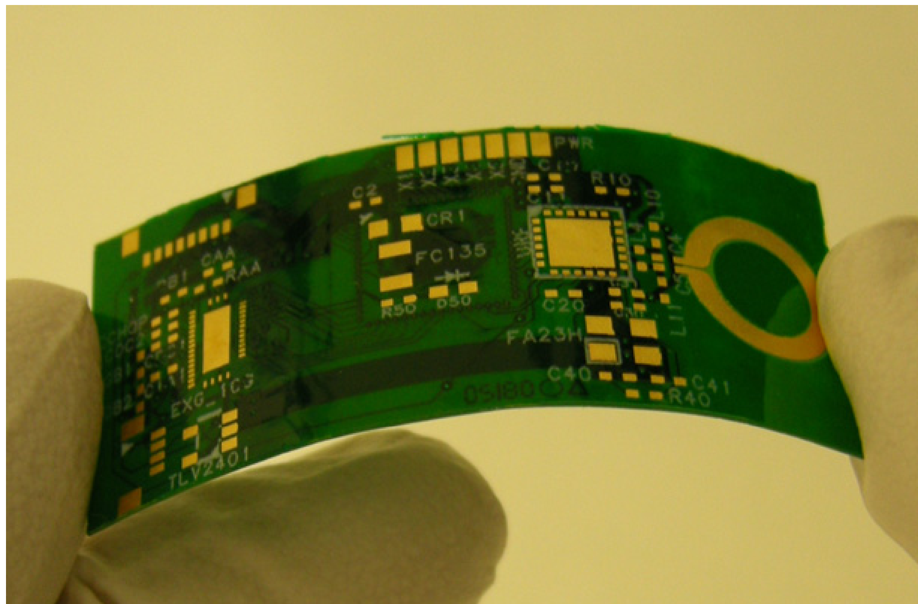


Figure 4.19: ExG substrate with integrated microcontroller

Component assembly

After substrate production, the components are assembled on both sides of the flex substrates. Most of the components to be mounted are SMT components, except for two active devices: the IMEC biopotential ASIC and the Nordic radio chip nRF2401A. These actives will be wire bonded on the substrates (Chip-On-Flex, COF), after the SMT components are assembled.

As flex substrates are known to take up moisture, they are first baked for 2 hours at 120°C to dry out the circuits before assembly. This pre-bake prevents outgassing of trapped moisture and the possible creation of defective conditions such as blistering or delamination of the substrate.

One of the most important points of attention during assembly of components on flex substrates is the flatness of the substrate. Even a slight curvature of the

substrate can cause a tombstoning effect creating opens. Therefore the flex is attached to a rigid substrate. This rigid substrate used in our lab is called the Flex-Fixer. It consists of a rigid base with on top of that a film to hold the flexible circuits in place and flat. The Flex-Fixer can withstand is 260°C, which is sufficient for the reflow process. The carrier can be used throughout the whole process of solder paste printing, component placement and even wire bonding without having to remove the flexible substrate.

Once the flexible substrate has been fixed on a carrier, the solder paste (3% Ag, 0.5% Cu and 96.5% Sn) is dispensed and the components for the ExG demonstrator are placed manually. The solder is reflown in a vapour phase oven at 240°C.

Finally the wire bonding (CoF) of the active devices is done at IMEC Leuven.

The assembled flexible wireless biopotential system is shown in Figure 4.20

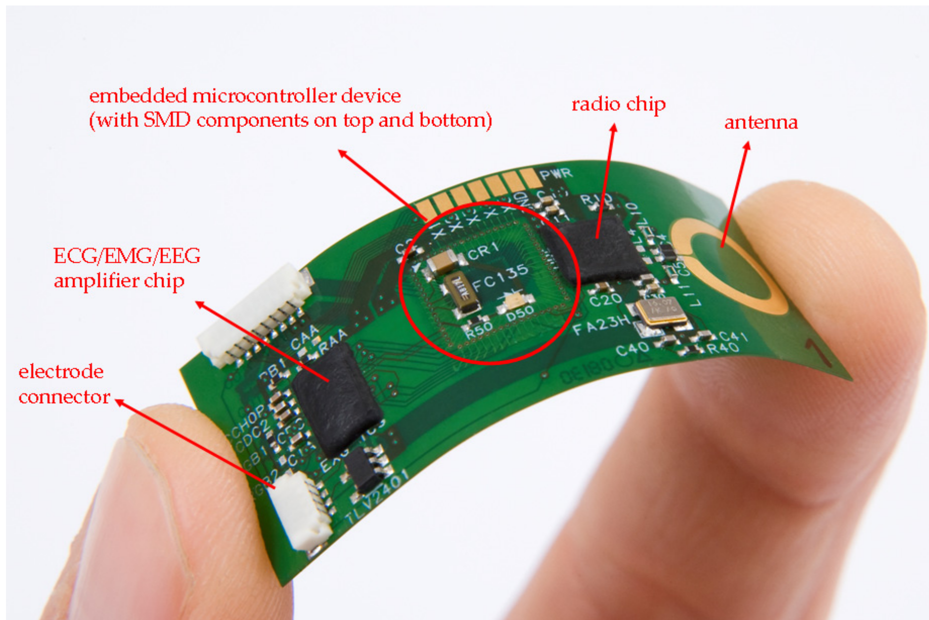


Figure 4.20: The flexible wireless biopotential system and its components (excluding battery)

4.5.5 Functionality demonstration

The functionality of the wireless biopotential system was tested at IMEC Leuven. The final ExG demonstrator with integrated microcontroller device is completely functional and able to monitor ECG signals. Figure 4.21 shows an example ECG waveform recorded with the wireless system using standard disposable stick-on Ag/AgCl foam electrodes.

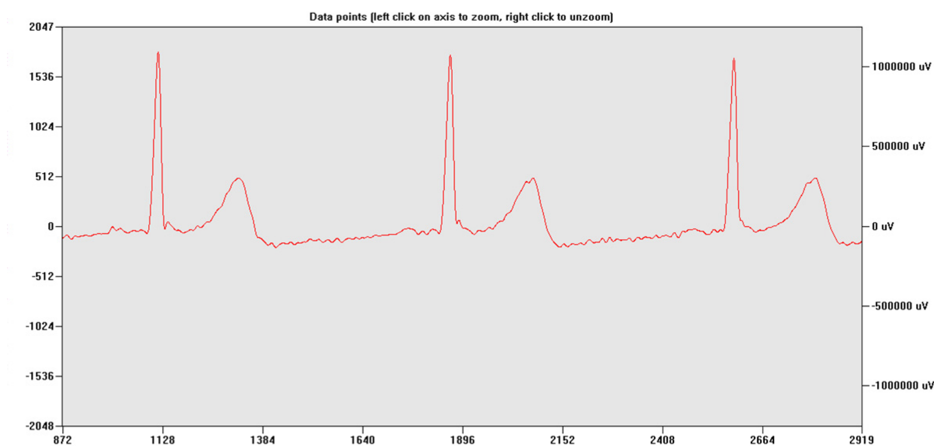


Figure 4.21: An example ECG waveform recorded wit the wireless system

4.6 Conclusions

A technology for 3D integration of functional active devices inside the inner layers of conventional flexible multilayer circuits has been established. Ultra-thin active devices are first integrated in a flexible ultra-thin chip package, which is in turn embedded inside a standard double-layer flex PCB. The UTCP packages serve as interposers to be embedded in a conventional multilayer flex substrate.

UTCP packages are aligned and fixed (heat tack) on a patterned inner layer of the multilayer substrate. Connections between package and wiring of the PCB or FCP is done by through hole interconnects.

3.5 μm metal thickness on the UTCP package turned out to be sufficient to ensure good interconnects. Also the presence of ENIG finish on the integrated samples did not cause interconnection problems.

Daisy chain interconnects between integrated dummy packages and the FCB were characterized, and monitored during reliability investigations. High temperature storage at 150°C (up to 1000 h), hot humidity storage at 85°C/85 r.H.

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(up to 1000 h) and thermal cycling between -40°C and +125°C (up to 1000 cycles) did not introduce any failure at the interconnects.

The integration process did also not affect the values of the 4PT via resistance of the interconnects on the UTCP package.

Finally this technology was used for the 3D integration of functional microcontroller device for a wireless ECG application. A Texas Instruments microcontroller MSP430F149 was successfully integrated inside a standard double-layer flex PCB, with even smaller SMD components mounted above and below the embedded chip, realizing a fully functional wireless biopotential system.

3D integration of UTCP packages leads to high density integration, since SMD components can be mounted on top and bottom of the integrated devices. In addition the UTCP packaged thin silicon devices are mechanically flexible itself, leading to an increased total flexibility of the resulting system.

References

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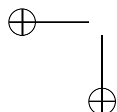
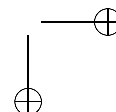
[2] P. Bauwens and A. Deridder. *Realisatie van Interconnecties op Dubbelzijdige Flexibele Substraten.* Master Thesis, Ghent University, 2005–2006.

Chapter 5

Alternative UTCP technologies - use of photodefinable polyimides

This chapter deals with two alternative UTCP technologies. Both technologies introduce photodefinable polyimides in the UTCP process flow. The first part of the chapter presents the concept of flat UTCP packages. This flat technology has an extra photodefinable polyimide inner layer, in which cavities are defined, in which the chips will be placed, realizing more flat packages. The second part presents a UTCP with photodefined vias: vias are photolithographically patterned in the top polyimide layer.

5.1 Flat UTCP

5.1.1 Introduction

A possible disadvantage for the 'standard' UTCP technology can be the non-planarity of the packages: this was already shown in Figure 2.4. The top polyimide layer is poorly planarizing and follows the shape of 'die + glue' on top of the base polyimide, this results in a height difference of about 20–25 μm between the middle and the outer sides of an UTCP package. This non-planarity can limit the resolution during the lithographic step for patterning the top metal layer. Also for possible stacking purposes flat packages could add some advantages.

The idea is to realize flat UTCP packages by the introduction of a cavity in an inner layer of the package. Dies can be mounted in these cavities on a dispensed

adhesive. The dimensions of the cavity have to match well with the dimensions of the die. Also the amount of adhesive dispensed in the cavity before chip placement has to be well controlled, making sure die + adhesive are nicely filling the cavity.

A possible approach for producing these cavities could be a dry etch of a cavity in the base polyimide layer using RIE. The PI-2611 can be dry etched with an etch rate of approximately 0.4 μm per minute, see Chapter 2. A sputtered Al layer is a suitable etch mask during the RIE. This method requires a thicker base PI-2611 layer (for cavity thicknesses 20–25 μm at least 3–4 extra PI–2611 are needed), 1 sputter deposition step, 1 photolithographic step for patterning the metal etch mask, 2 metal etch steps (one for patterning the metal before RIE and 1 for etch mask removal after RIE) and of course an RIE step.

An interesting alternative approach is presented here: the application of a photodefinable polyimide inner layer. The thick polyimide inner layer is spincoated, and the cavities are photolithographically developed in this polyimide layer. The concept and the process optimization for realizing flat UTCP packages making use of a photodefined cavity are discussed below.

5.1.2 Photodefined cavity

Flat UTCP packages can be realized by the introduction of an extra photodefinable polyimide inner layer. The photosensitive film is spincoated and cavities can be developed away after illumination. Thin devices will then be placed in these cavities, filling the cavities and realizing flat chip packages this way.

Figure 5.1 gives an overview of the different process steps for the production of flat UTCP packages by means of a photodefined cavity [1].

The base substrates are PI-2611 spincoated on a rigid glass carrier. Next the photodefinable PI is spincoated and cavities are photolithographically patterned in this PI layer. Chips are placed in these cavities, using BCB as adhesive material. The 'BCB + chip' is filling the cavity. Finally the chip is covered with a 5 μm thin PI2611 film. Vias are opened to the contacts of the chip through this top polyimide. Top metal is sputtered and photolithographically patterned providing a fan-out to the embedded chip. The result is a very thin, flat, flexible chip package, with chips placed in the cavity in between two PI-2611 layers.

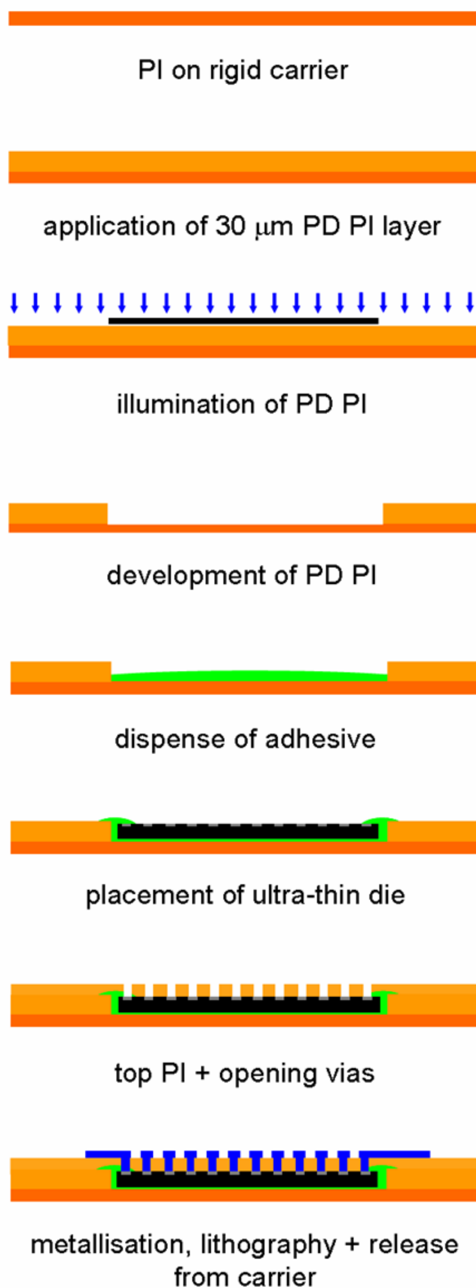


Figure 5.1: Process flow overview of the flat UTCP

Most of the photodefinable polyimides available on the market have a much higher CTE than the PI-2611. This can introduce a lot of stress in the different materials of the package. Therefore the symmetric build-up is necessary.

As discussed already for the standard UTCP technology, a CTE match is important to limit stresses introduced during processing in the ultra-thin silicon devices. Since chips are placed in the cavities there is no interface chip–photodefinable polyimide, so stresses introduced in the thin silicon devices will be similar as for the UTCP technology, see Chapter 3.

Two different types of thick spincoatable polyimides were tested for the flat UTCP: first the HD-4012 and also the HD-7012 (both from HD Microsystems).

5.1.3 HD-4012

First processing and optimization experiments were done using the photodefinable polyimide (PDPI) HD-4012 from the HD-4000 Series Polyimides (HD Microsystems).

The HD-4000 is a negative tone, solvent developed, self-priming photodefinable polyimide. The product HD-4012 of this series was formulated for thicker films: soft baked and cured film thicknesses of the HD-4012 are shown in Figure 5.2. Cured film thicknesses up to 60 μm can be achieved [2].

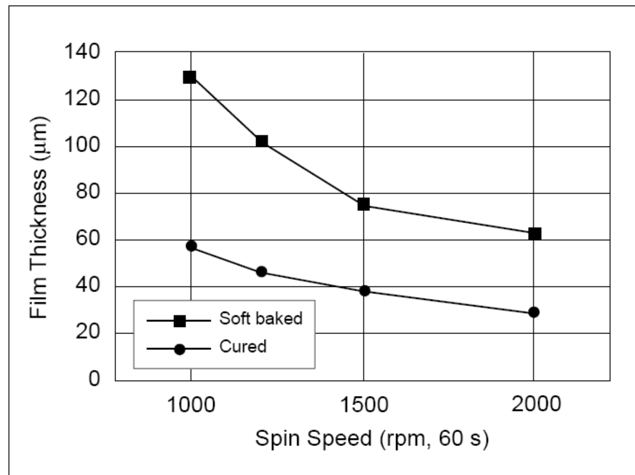


Figure 5.2: Soft baked and cured film thickness of HD-4012 in function of the spin speed

This photodefinable polyimide is applied by spin coating. After a hotplate soft bake step, the polyimide layer can be illuminated on a standard lithography tool.

(With negative tone photo mask.) After imaging, the substrates are developed in the dedicated developer PA400D and rinsed in PA400R (both HD Microsystems). Finally the polyimide layer is cured up to 375°C.

Different process parameters such as optimal softbake time and temperature, illumination time, post exposure bake (PEB) conditions and development time were optimized, as also described in [3]. An overview of these process parameters for the HD-4012 is given in Table 5.1.

Process	Unit	Parameters
spincoating	rpm/s	500/5 + 1000/10 + 2000/60
hot plate soft bake	^{o}C/s	90/120 + 110/420
exposure	mW/cm^2	200–450
PEB	^{o}C/s	110/60
develop (PA400D)	min	5 in beaker + 1 using USA
overlap	s	10
rinse (PA400R)	s	10
cure	^{o}C	up to 375

Table 5.1: Process parameters for patterning HD-4012 polyimide films

The process optimization was not fully finalized, since the production was stopped and the PI was not longer available during optimization work (after summer 2005). An alternative polyimide was purchased: HD-7012 (HD Microsystems).

5.1.4 HD-7012

HD-7012 is a photodefinable, spincoatable polyimide for ultra thick applications, with built-in adhesion promoter. Cured film thicknesses range between 20–70 μm. These films have high Tg and excellent mechanical properties to survive the thermal and chemical exposures of post application processing and excellent elongation to prevent cracking [4].

Table 5.2 gives an overview of different process steps for the application of a photodefined polyimide HD-7012 film. The basic process involves the spin coating of the liquid polyimide and a drying step using hot plates. The polyimide layer can then be exposed on a standard lithography tool. (Requiring a negative tone photo mask since the photodefinable polyimide is negative acting.) After imaging, the substrates are developed and rinsed. Finally the polyimide layer is fully cured to both imidize the film and remove the photo package.

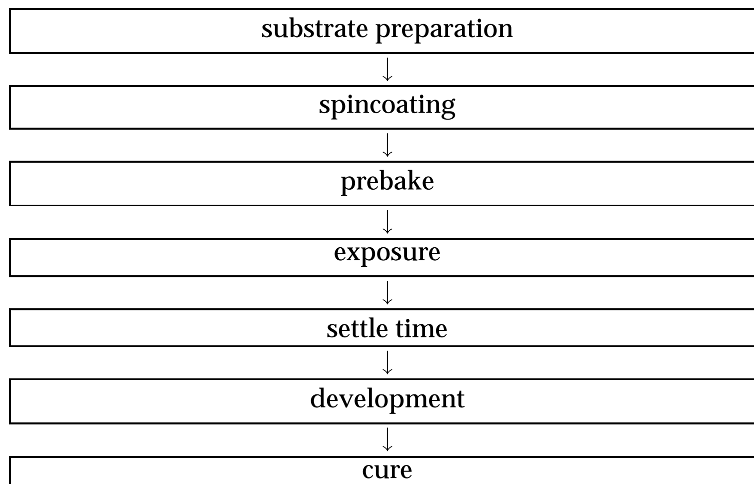


Table 5.2: Process flow for the application of a photodefinable HD-7012 polyimide layer

The individual process steps and the optimization are discussed below more in detail.

Process optimization

Substrate Preparation Base substrates for the flat UTCP are a 5 μm PI-2611 film deposited on a rigid glass carrier, similar to the base substrates for the standard UTCP technology, including selective application of adhesion promoter only at the edges of the substrates, but with only one 5 μm PI-2611 layer.

The photodefined polyimide film will be applied on top of this cured PI-2611 film. An RIE treatment enhances the adhesion of the HD-7012 on the cured PI-2611. (Parameters RIE: first 2 minutes with a 5 sccm-CHF_3/20 sccm-O_2 gas mixture, followed by a 2 minutes 25 sccm oxygen plasma; both applied with a power of 150 W and a pressure of 100 mTorr.)

Spincoating and film thickness HD-7012 is applied by spincoating. The liquid polyimide is first dispensed statically in the middle of the substrate. The PI is spincoated first at low spinspeed (5 s at 500 rpm), in order to allow the polyimide to gradually cover most of the surface, before accelerating to final spin speed. Spin time is 45 sec at final speed. Cured film thicknesses are defined for different spin speeds, the result is shown in Figure 5.3.

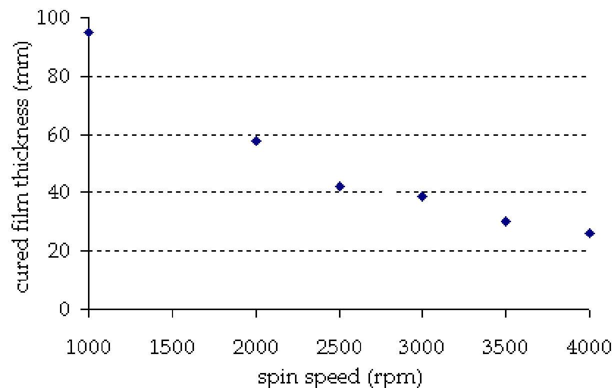


Figure 5.3: Spin speed cure of polyimide HD-7012

Prebake Once the substrates are coated with the polyimide HD-7012, they are first prebaked. During this step already part of the solvents are driven off, and this provides enough chemical resistance and adhesion so that the exposed areas of the coating will not be attacked or delaminated by the developer. This prebake is done on a hotplate. Parameters for this prebake step are:

- 60°C for 240 s
- 90°C for 240 s
- 110°C for 240 s

After prebake the substrates have to cool down to room temperature prior to exposure.

Exposure The photodefineable films can be patterned directly by exposure to UV light: they harden with exposure. The softer areas are then removed afterwards with the suitable developers. The polyimide is exposed and illuminated, with an exposure dose of 280 mW/cm^2 (illumination time: 28 s).

Development The standard developer for the HD-7012 is PA400D (solvent based developer, based on gamma butyrolactone). Substrates can be rinsed in PA400R.

The polyimide can be developed in a beaker with the dedicated developer PA400D for 90 s using USA, an intermediate rinse in a 1:1 solution of PA400D : PA400R and finally a 10 s rinse in PA400R.

For better results an additional settle step of 30 minutes can be introduced after illumination and before development: this ensures much smoother cavity edges after development. This is illustrated in Figure 5.4 and 5.5 [5, 6]. Figure 5.4 shows a cavity defined in the HD-7012 photodefinable polyimide layer with residual polyimides at the edges. The cavity shown in Figure 5.5 was developed after an additional settle time.

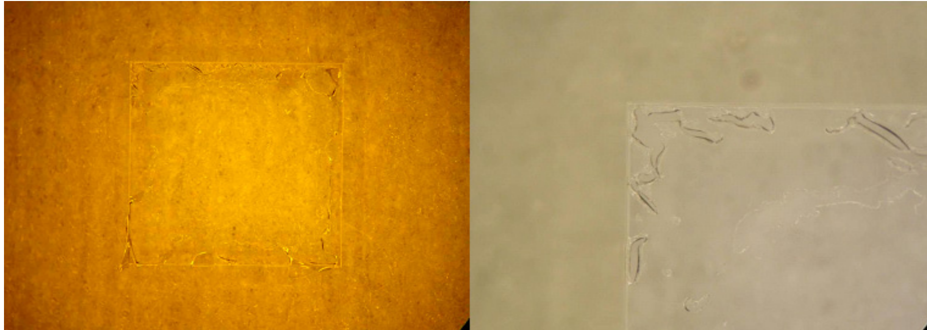


Figure 5.4: Cavity in HD-7012 photodefinable polyimide layer with residual PI at the edges [5, 6]

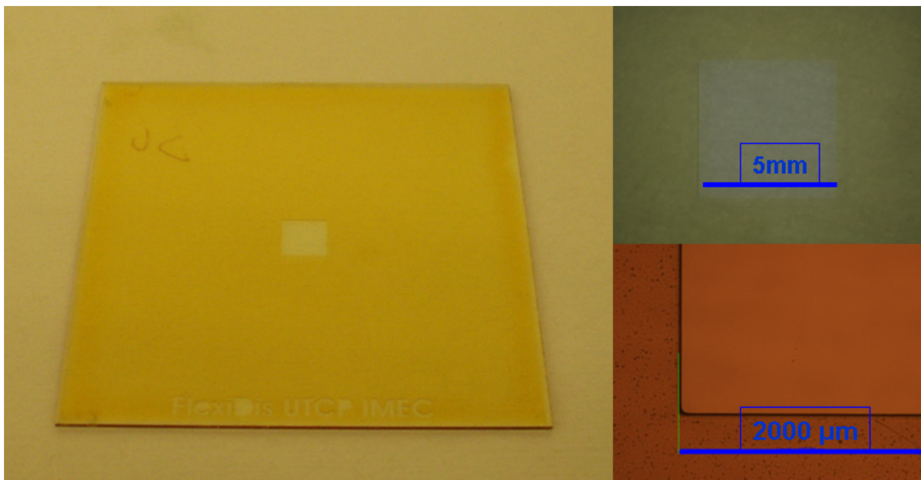


Figure 5.5: A cavity created in the photodefinable PI layer: two close-up top views of the cavity are shown on the right [5, 6]

Cure The HD-7012 is cured with following curing profile:

- heating from room temperature to 200°C, with a ramp rate of 4°C per minute
- 30 minutes at 200°C
- heating from 200 to 375°C, with a ramp rate of 2,5^{o}C per minute
- 60 minutes at 375°C
- gradual cooling down to room temperature

(Curing is done in a vacuum oven, adding a little N_2 flow (5 sccm) to ensure better solvent removal during curing.)

Results

After the curing of the HD-7012 polyimide layer, the chips will be placed in the cavities, see Figure 5.1. Finally a covering PI-2611 layer is applied and cured (again RIE treatment is applied first to ensure good adhesion of the top PI layer on the cured PDPI film).

First feasibility has been demonstrated and 5 μm PI-2611/30 μm HD-7012/5 μm PI-2611 sandwiches without integrated chips were processed and released from the carrier. This is shown in Figure 5.6.

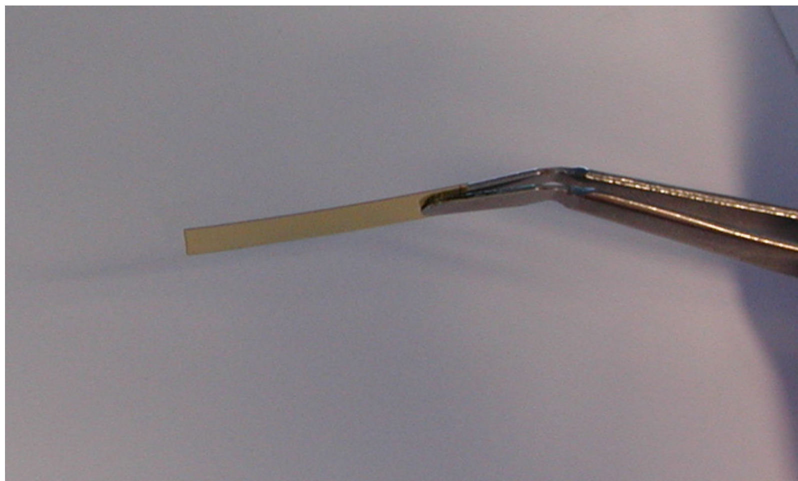


Figure 5.6: Flatness of sandwich of 5 μm PI-2611/30 μm HD-7012/5 μm PI-2611 after release from rigid carrier

Figure 5.7 shows the release of an asymmetric 5 μm PI-2611/30 μm HD-7012 stack. This indicates the importance for having a symmetric build-up. Stresses are introduced in the different polyimide layers during the curing because of the CTE mismatch between the PI-2611 (CTE = 3×10^{-6} K^{-1}) and the HD-7012 (CTE = 74×10^{-6} K^{-1}). These stresses can result in curling of the substrate after release. For the symmetric build-up with another PI-2611 layer on top, these stresses are compensated and the result will be a flat UTCP after release from the carrier.

Figure 5.8 shows a cavity, developed in the inner layer of the symmetric PI-2611/HD-7012/PI-2611 stack, after release.

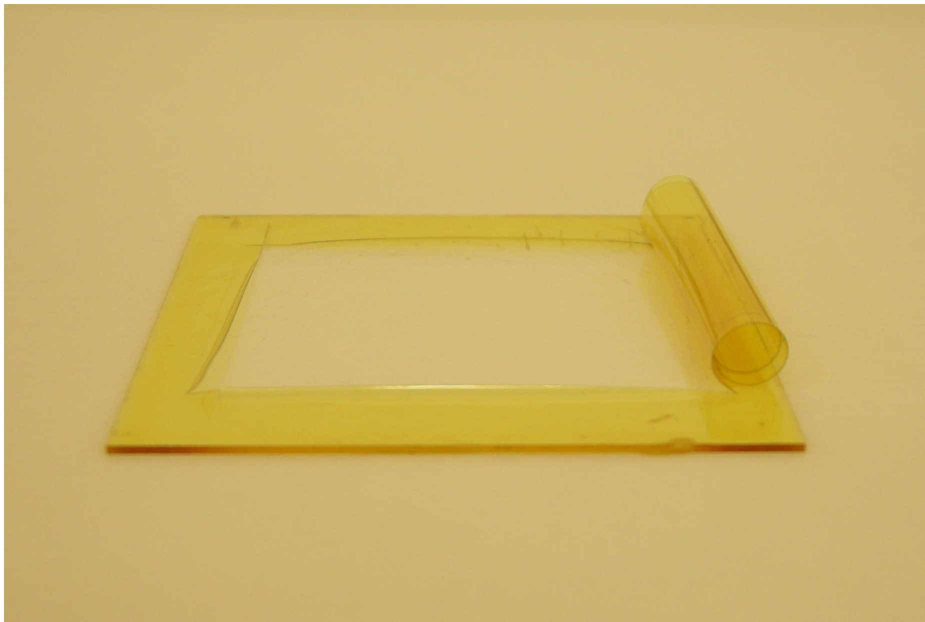


Figure 5.7: Stress induced in the asymmetric PI-2611/HD-7012 stack during processing results in curling of the substrate after release from its carrier

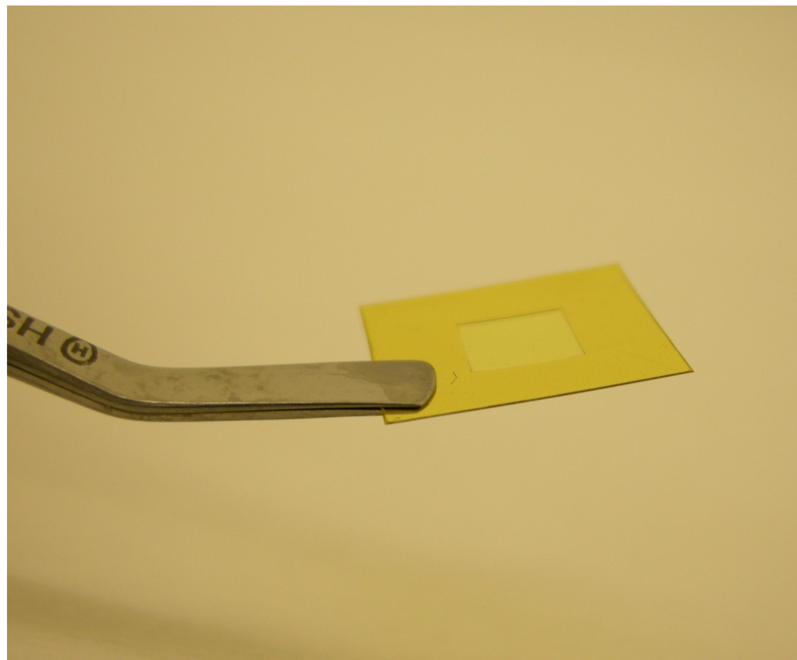


Figure 5.8: Cavity realized in the HD7012 inner layer of a PI-2611/HD-7012/PI-2611 stack

Further optimization and results

A lot of the process optimization, realizing the symmetric polyimide stack and demonstration of the principle was done in the framework of this PhD [1]. Further optimization of this processing, including the mounting of the die in the cavities and the via laser drilling to the contacts of the embedded chips, was continued in the framework of the European FP6-IP-FlexiDis project [7]. Interconnection test chips are integrated successfully and characterized with this flat UTCP technology: these results will be published in the PhD thesis of Jonathan Govaerts.

The aim was to combine the UTCP technology with Philips' EPLAR (Electronics on Plastics by Laser Assisted Release) technology, where a thin-film active matrix for driving a flexible display is made on spin-on polyimide as the substrate. This results in a very flexible active matrix substrate. Integration of the display driver chips as UTCP in the same substrate would allow to maintain more or less this flexibility, in contradiction to the use of standard packaged drivers, which reduce greatly the flexibility of the entire display.

5.2 UTCP with photodefined vias

5.2.1 Concept

The introduction of a photodefinable polyimide in the UTCP technology could also be a valuable alternative for the via production: if the covering PI-2611 layer can be replaced by a photodefinable polyimide layer, via openings can then be photolithographically patterned in this layer. Photolithographic via development can be a cost-effective alternative technology for the laser ablation or RIE based via technologies discussed in Chapter 2.

A suitable process flow for the production of UTCP packages with photodefined vias is given in Figure 5.9. The basic process involves the substrate preparation (application of the base polyimide layer on rigid glass carrier) and the placement of the ultra-thin devices on top of these substrates using BCB as adhesive material. The covering photosensitive polyimide film is spin coated on top of the fixed die. This photodefinable polyimide will be patterned before curing: the polyimide is first illuminated through a suitable via contact mask and the vias are opened by solving the non-illuminated material in a dedicated polyimide developer. Finally this patterned top polyimide is cured and the top metallization is deposited using sputtering.

It is clear that this technology, needing only a photolithographic process step for opening the vias, can be a very cost-effective alternative for the laser drilling or RIE processes. This PDPI based UTCP technology has been demonstrated in the framework of this PhD study: a suitable polyimide was selected first and the different processing steps introducing this polyimide in the UTCP technology were optimized. Test samples were produced and characterized.

5.2.2 Material selecton: PI-2731

A suitable polyimide for the application as photo imageable top layer for the UTCP technology was first selected, based on following requirements:

- target polyimide film thickness around 15 μm: this is the typical layer thickness for the top polyimide in the 'standard' UTCP technology.
- low CTE: in order to limit possible stresses introduced in the ultra-thin silicon chips (CTE = $2.6 \times 10^{-6}\,K^{-1}$) during the processing of the packages.

The polyimide PI-2731 from the Pyralin PI-2730 series (HD Microsystems) was selected. Pyralin PI-2730 series has been specially developed for use as a passivation layer for semiconductors. The Pyralin PI-2730 series polyamic esters contain a negative-working photopackage making them sensitive to broadband exposure from a mercury lamp in the range of 350 to 435 nm. The material is supplied as

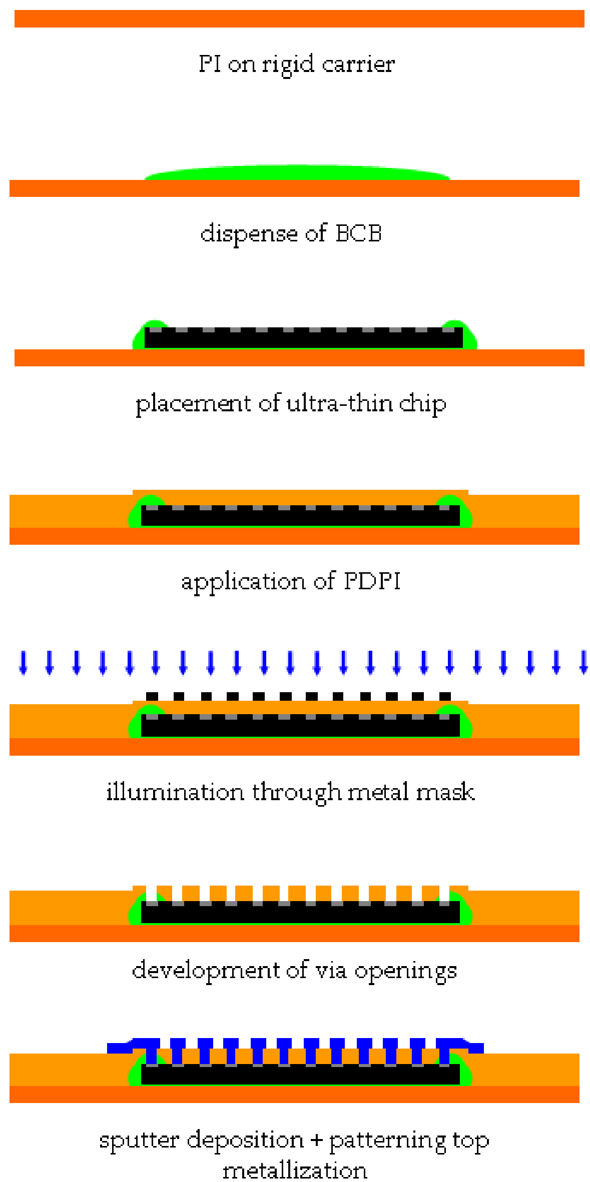


Figure 5.9: Process flow of UTCP with photodefined vias

viscous solution suitable for spincoating; cured film thickness between 2,5 and 15 μm can be achieved. This material is also self-priming thus eliminating the need for an additional adhesion promoter. The cured polyimde film offers good mechanical properties and has a low coefficient of thermal expansion of 13 ppm [8].

5.2.3 Process optimization

The different process steps for the application of a PI-2731 film are shown in Table 5.3. The optimization of these different process steps is discussed below in more detail.

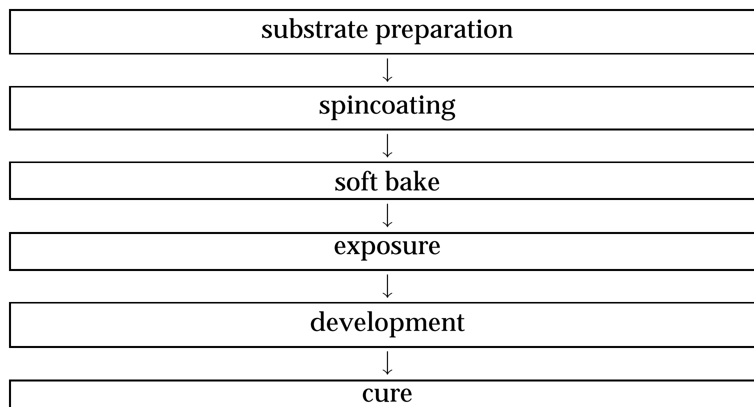


Table 5.3: Process flow for the application of a photodefinable PI2731 polyimide layer

Substrate Preparation

The base substrates consist of a polyimide layer spincoated on rigid glass carrier. As for the standard UTCP technology the base polyimide film is a 20 μm PI-2611 film: the PI-2731 is not suitable for the release method of selective adhesion on the glass substrates since this polyimide is self-priming and would have a good adhesion on the substrates. Chips are placed face-up on this first polyimide layer using BCB as adhesive. Once this BCB is cured, the top polyimide will be applied. The samples are plasma treated first before the application of this photodefinable polyimide. An RIE treatment enhances the adhesion of the PI-2731 on the cured PI-2611 and on the BCB. (Parameters RIE: first 2 minutes with a 5 sccm-CHF_3/20 sccm-O_2 gas mixture, followed by a 2 minutes 25 sccm oxygen plasma; both applied with a power of 150 W and a pressure of 100 mTorr.) To ensure good adhesion of the PDPI on the chip also an adhesion promoter VM652 is applied: spincoated at 3000 rpm for 30 s and dried on a hot plate at 120 for 1 minute.

Spincoating

PI-2731 is applied by spincoating. The liquid polyimide should be first dispensed in the centre on static substrate. (Never trap air into the highly viscous solution. If bubbles are trapped in, give time to dissipate otherwise coating 'comets' will result.) Next the substrate is first rotated at 500 rpm for 5 seconds, in order to allow the polyimide to gradually cover most of the surface, before accelerating to final spin speed. Spin time is 45 sec at final speed. Cured film thicknesses are defined for different spin speeds, the result is shown in Figure 5.10. Test samples are spincoated at 2000 rpm with a resulting cured layer thickness of +/- 17 μm.

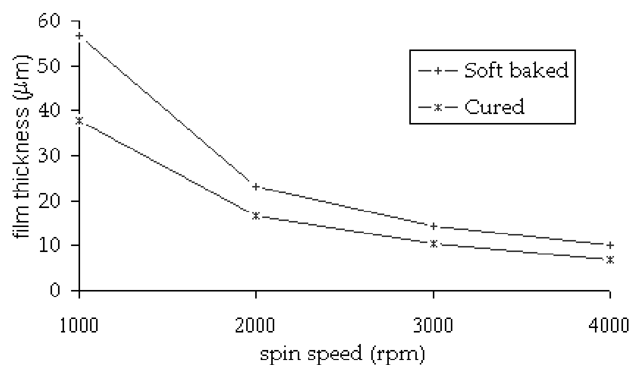


Figure 5.10: Spin speed cure of polyimide PI-2731 (first 5 s spin at 500 rpm, next 45 s at final speed)

Soft Bake

After application of the polyimide, a bake process is required in order to partially cure the polyimide prior to patterning. Part of the solvents are driven off, leaving the polyimide coating dry, yet soluble in the developer solution. Bonding of the polyimide is also achieved during this softbake cycle as the priming chemistry is activated by temperature.

This bake stage provides sufficient chemical resistance and adhesion so that the exposed areas of the coating will not be attacked or delaminated by the developer.

Soft bake is done on a hot plate:

- 60°C for 180 s
- 95°C for 180 s

Exposure

PI-2731 is a negative acting PDPI. The areas exposed to the UV light harden with exposure, the soft areas can be developed away afterwards. Datasheets indicate required exposure dose of 50 to 200 mJ/cm^2. Good results are achieved using 100 mJ/cm^2 (i.e. 10 s illumation time). As the polyimide is negative acting: a dedicated negative metal via etch mask is designed, covering only the via openings during illumination (size: 50 x 50 μm^2). This enhances the alignment before illumination: the pattern of squares can easily be aligned directly on the contact pads of the chip.

Development

The non-exposed areas of the PI-2731 film can be developed in PA400D. Development is done by agitation in a beaker. The surface is rinsed afterwards with Pyralin RI9180. Optimal results are achieved with following parameters:

- development: 2 min in PA400D
- rinse: 1 min in RI9180

Cure

Curing conditions for the PI-2731 are:

- heating from room temperature to 200°C, with a ramp rate of 4°C per minute
- 30 minutes at 200°C
- heating from 200 to 350°C, with a ramp rate of 2,5^{o}C per minute
- 60 minutes at 350°C
- gradual cooling down to room temperature

(Curing is done in a vacuum oven, adding a little N_2 flow (5 sccm) to ensure better solvent removal during curing.)

5.2.4 UTCP test sample production

UTCP test samples with photodefined vias are realized using the above discussed, optimized parameters. Figure 5.11 shows a picture of the photodefined vias after development. Figures 5.12, 5.13 and 5.14 give a detailed view of the top and the bottom of the vias: after development, after cure and after RIE. The RIE treatment done after the full cure of the photodefinable polyimide ensures a good adhesion of the sputtered metal layer on the cured polyimide. (Same as for the UTCP technology, see Chapter 2) This RIE treatment removes also all possible residues at the bottom of the vias.

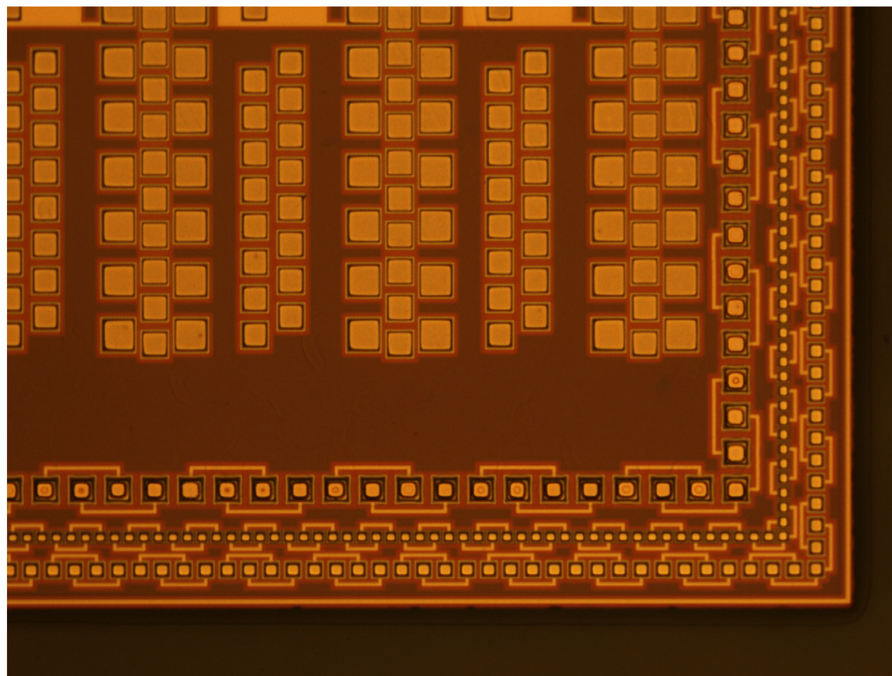
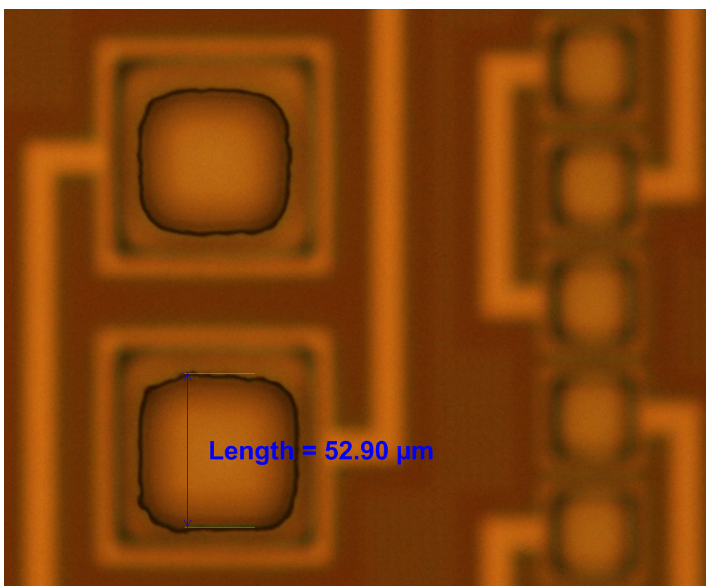
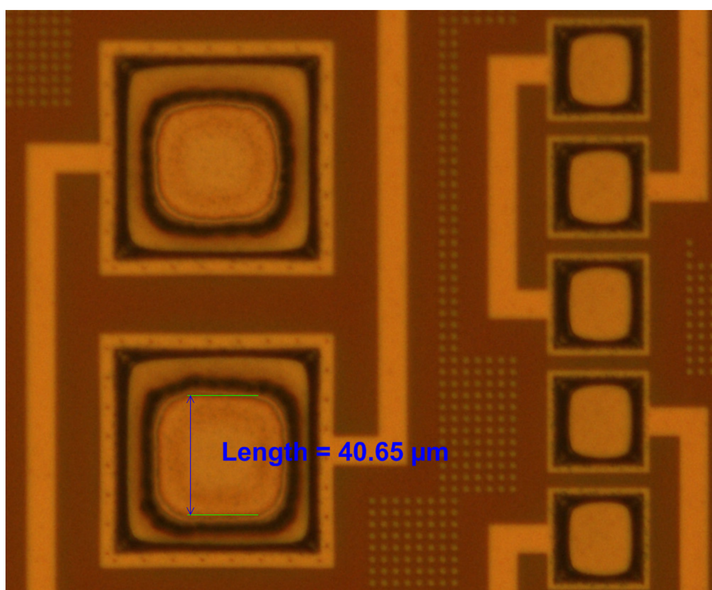


Figure 5.11: Photodefined vias

Figure 5.12 gives a detailed view of two photodefined vias after development, with a top diameter of 52 μm and a bottom diameter of 40.5 μm. The top diameter of the same via is 60 μm after cure, see Figure 5.13.



(a) Top



(b) Bottom

Figure 5.12: Top and bottom of photodefined via after development

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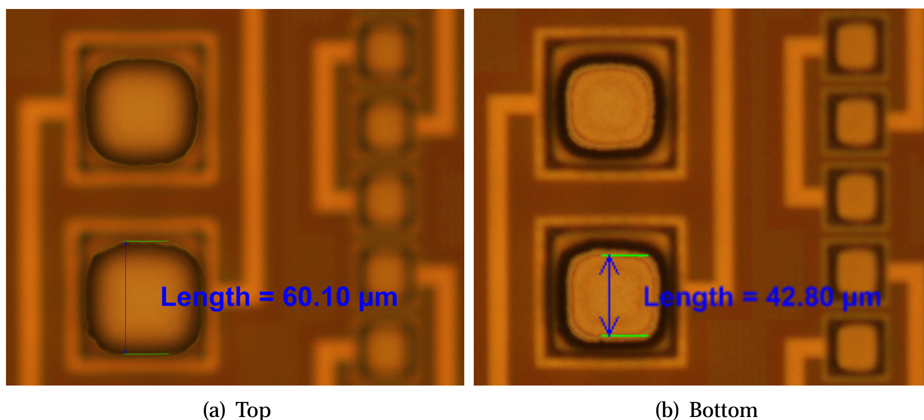
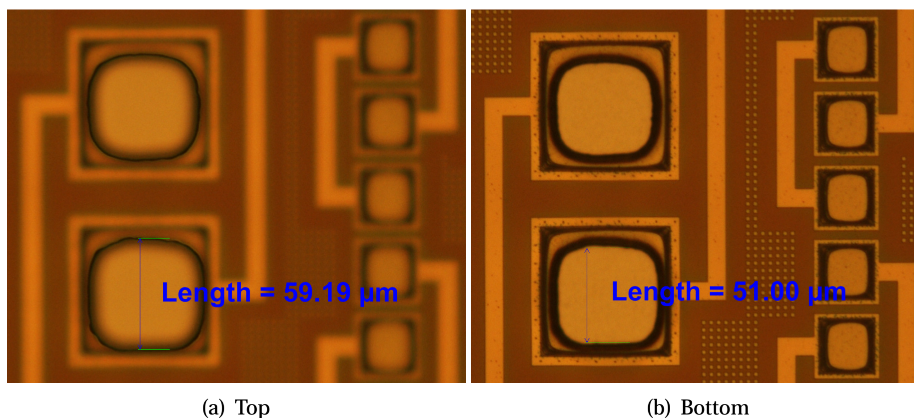


(a) Top (b) Bottom

Figure 5.13: Top and bottom of photodefined via after cure



(a) Top (b) Bottom

Figure 5.14: Top and bottom of photodefined via after RIE treatment

The same test chips and test design were used as described in Chapter 3. A realized test sample is shown in Figure 5.15: after via development, a 50 nm TiW and 1 μm Cu layer is sputtered and photolithographically patterned. Table 5.4 gives the results of the four-point-measurements of the via resistances and the daisy chain resistance DC 2 - DC 4. The average value for the via resistance is 0.0495 Ω.

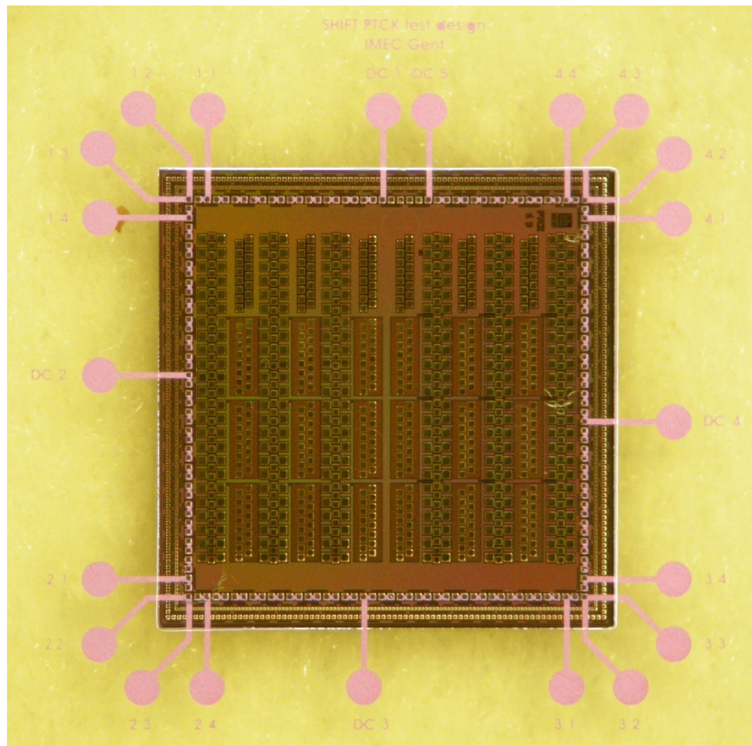
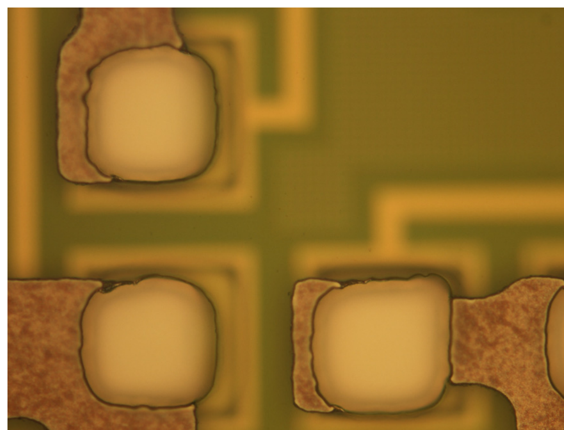


Figure 5.15: Test sample for photodefinable via technology

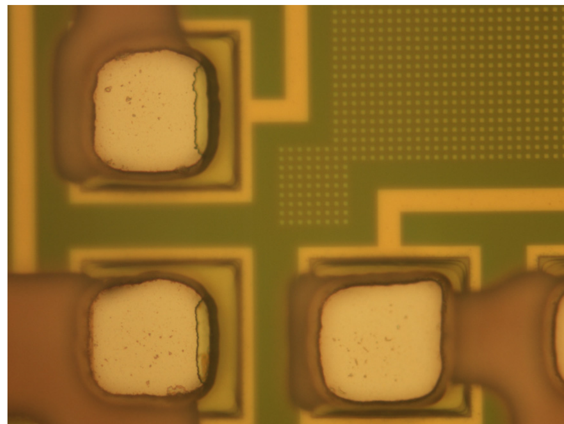
	resistance [Ω]
4PT1	0.044
4PT2	0.050
4PT3	0.053
4PT4	0.051
DC 2-4	38.07

Table 5.4: Measurement UTCP with photodefined vias

Figure 5.16 shows a detail of the metallization of the test sample with the photodefined vias. The sample was heavily overetched. This explains the higher via resistance values in Table 5.4, compared with the typical values presented in Chapter 3. It is clear that via resistance values will be lower if etch results are improved.



(a) Top of metallized via



(b) Bottom of metallized via

Figure 5.16: Overetched metal pattern of the photodefined vias, resistance value of the bottom left via: 0.051 Ω

5.3 Conclusions

Two alternative UTCP technologies are presented in this chapter. First, a concept for producing flat ultra-thin chip packages has been introduced. This technology introduces an extra HD-7012 photodefinable polyimide inner layer, in which cavities are defined. The chips can be placed in these cavities, realizing more flat packages. Process optimization, realizing the symmetric polyimide stack and demonstrating the principle, is presented. This technology has been further opti-

mized and used for display driver integration in flexible substrate in the framework of the European Flexidis project.

The second technology describes a UTCP package with photodefined vias. The PI-2611 top layer of the conventional UTCP is replaced by a photodefinable PI-2731 polyimide layer. $60\,\mu$m vias to integrated interconnection test chips were realized, and characterized after metallization. A possible problem for this technology can be the higher stresses, introduced in the ultra-thin device during processing, due to the higher CTE of most available photodefinable polyimides. This has to be investigated.

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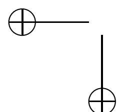
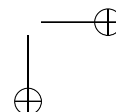



Chapter 6

Silicon thinning

In this chapter Si thinning processes are discussed. The first part of this chapter gives a very short overview of the different wafer thinning processes. In the second part special attention is given to the development of an individual Si die thinning process. Process optimization is presented and also some thinning results are included.

6.1 Introduction

As electronic applications shrink in size, integrated circuit (IC) packaged devices must not only be reduced in footprint but also in thickness. Die thickness is one of many crucial aspects in developing thinner and smaller packages; just like for the development of the UTCP. Thin chips allow more functionality per unit volume in a stacked die package, reduce the weight, and even become flexible. In this way chip thinning can also improve the flexibility in applications like smart cards. Thin chips are necessary for the next generation of ICs. The current chip thickness of about 100 μm for volume production is expected to decrease to about 50 μm in the near future and 20 μm within the next decade [1]. At the same time, wafer diameters will increase, which consequently leads to increased wafer thickness to withstand wafer manufacturing. Typical wafer thicknesses are shown in Table 6.1.

The requirement of an increasing thickness of the wafers during processing and the contrasting interest of thinner dies makes thinning techniques more and more important. The most effective way is the thinning of the whole wafer: suitable processes have been developed, and efficient thinning equipment is available [4]. But in some cases also thinning down of individual dies can be very useful. An optimized thinning process for thinning down individual dies is presented in this chapter.

wafer diameter (mm)	typical thickness (μm)
50	250–300
75	350–400
100	500–550
125	600–650
150	650–700
200	700–750
300	750–800

Table 6.1: Typical Si wafer thicknesses in function of the wafer diameter [2, 3]

6.2 Wafer thinning processes

Thinning silicon wafers down to thicknesses below 20–25 μm is still not common but a number of manufacturers have already presented equipment for this technology, and there are first services which offer such extreme wafer thinning and dicing. This section gives a very short overview of how most wafer thinning processes look like.

Most grinding systems start with a mechanical grinding (coarse and fine grinding). The coarse grinding removes rapidly most of the material, but introduces a lot of damages at the backside surface of the silicon wafer. A fine grinding process is much slower, but can already remove part of this damage. But after the mechanical back grinding steps there is a lot of subsurface damage introduced in the silicon material. Typical values for this subsurface damage are 10-25 μm [5]. Therefore there is a need for a stress relief process after mechanical grinding, which is increasingly important with decreasing final wafer thickness, because the damage layer becomes higher in relation to the total thickness. The stress relief process is most typically a back-etching process. Most common are chemical etching, chemical mechanical polishing (CMP) or plasma etching [6].

Another important topic is the dividing of the wafer into dies: the dicing process. Especially for thin dies, the edge quality of the chips after dicing plays an important role. Normally the wafers are diced with standard wafer saws. But a typical phenomena introduced by sawing of the wafer is the chipping: these are the mechanical defects on the sides of the cut, the little pieces of silicon breaking off the edge of the chip especially at the backside of the chip. These damages, also called 'shell cracks', are caused during this mechanical sawing process. These shell cracks can be insignificant for thick chips but gain influence with the chips getting thinner, because the mechanical damage introduced by the mechanical saw at the chip edge reveals high risk for chip breakage during back-end chip processing. To reduce this risk separation-by-thinning processes have been developed.

Figure 6.1 shows a typical wafer separation-by-thinning process: the IZM Dicing-by-Thinning process [7, 8]. Instead of sawing the thin wafers after back thinning, front side dicing grooves are opened before grinding, this increases the fracture strength of the thin dies significantly [9, 10].

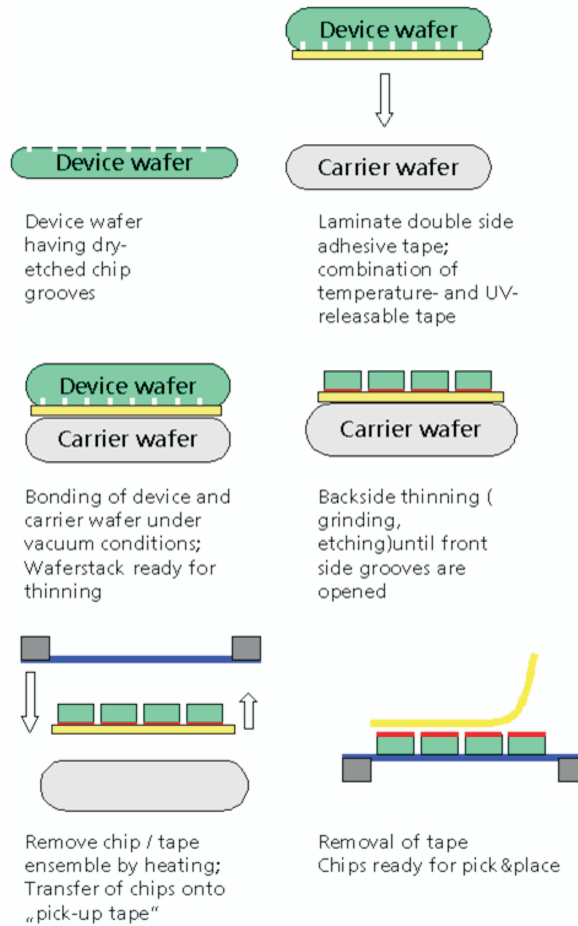


Figure 6.1: Schematic view of the Dicing-by-Thinning process and chip transfer to pick and place tape (source: IZM [8])

Preparation of the chip grooves can be accomplished by means of a standard wafer saw or by silicon dry etching. Etching increases the breaking force considerably, and reduces also the width of the scribe line by a large extent. A reduction of the sawing groove width enlarges, especially for small die sizes, the

number of chips per wafer enormously. If the trenches are opened by dry etching, the groove geometry is also no longer restricted to rectangular shapes. This way chips with other shapes can be manufactured.

After opening the grooves, the trenched wafer is mounted on a carrier wafer using a temperature releasable tape and thinned from its backside until the chip grooves are opened. If chip separation takes place during backside spin-etching, the grooves are rounded by the etchant and possible residual microcracks are removed. After thinning the chips can be transferred onto a pick-up tape, and are ready for pick & place.

6.3 Individual chip thinning technology

For a lot of research purposes it can be very useful to have also a thinning process for thinning down individual chips. Very often one needs only a limited amount of thinned dies, and not a full wafer. Purchasing whole functional wafers and thinning these wafers down would then be very costly since fully processed wafers can represent a value of some thousands of US Dollars. One example: for studying the impact of thinning on functional devices, it would be very cost intensive if one would have to thin down the full functional wafers to all different final thicknesses.

In a lot of cases it is also not so common to have access to whole functional wafers. Very often bare dies are only available as single (unthinned) dies. In this thesis also the embedding of ultra-thin functional dies was studied, see Chapter 3. These chips were only available a single, unthinned, bare dies. Therefore a thinning process for individual chips was optimized, in order to be able to thin functional, individual, silicon devices down to thicknesses below 20 μm. Such an individual die thinning process is very interesting if only limited numbers of thin dies are needed or if the silicon devices are only accessible as bare single dies and not as full wafers.

6.3.1 Set-up

The chip thinning technology is optimized on a PM5 Precision Lapping and Polishing Machine (Logitech, [11]), which is shown in Figure 6.2. The PM5 has one workstation for small scale operation. The principle is as follows: during thinning the single devices are mounted on rigid glass carriers by means of a mounting wax. These carriers are then fixed on the vacuum chuck of the JIG and during the thinning process this JIG is placed face down on the lapping or polishing plate. The lift-off lapping or polishing plate is mounted on a drive plate and the samples are backgrinded by rotating the plate and adding an abrasive material. This abrasive material is supplied from a dedicated abrasive cylinder.

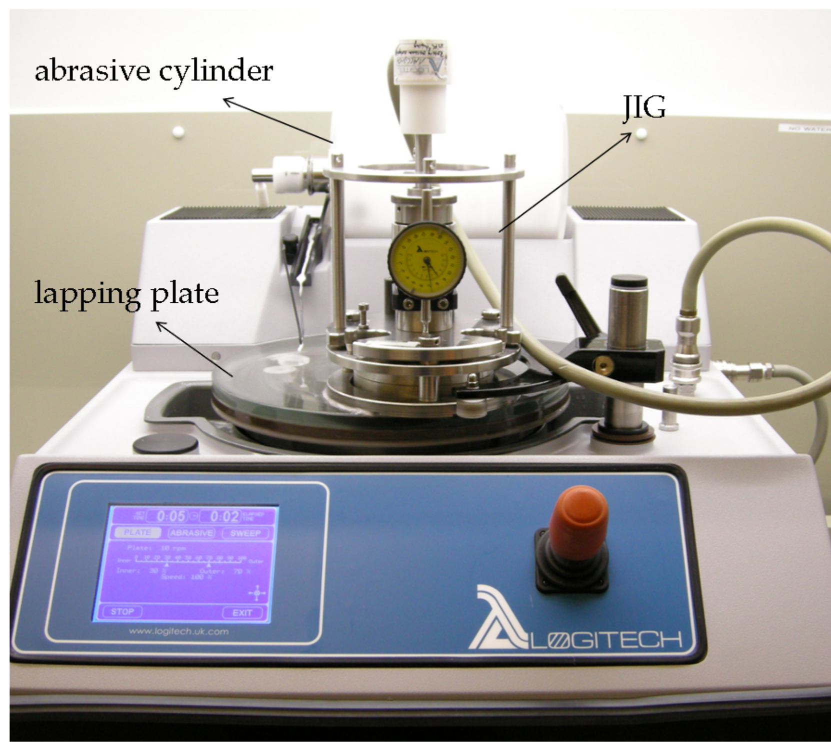


Figure 6.2: Logitech PM5 Precision Lapping and Polishing Machine as installed in the cleanroom

A general overview of different parts and their settings are given below. Details of the silicon thinning process optimization are given in the next section of this chapter.

First of all a lift-off lapping/polishing plate is mounted on a drive plate. During operation this drive plate can rotate with speed up to 70 rpm. Typical materials for the lapping plate are cast-iron or glass and for polishing plate polyurethane or a wide range of soft polishing cloths.

During the thinning process an abrasive material is added. The abrasive is supplied by the autofeed cylinder placed on rotating rollers. The cylinder is rotating and the agitated abrasive flows via the slurry chute and drip wire to the lapping or polishing plate. A constant rotation on the rollers ensures the abrasive to remain in suspension. Typical drip rate is 1–2 drips per second. Typical abrasive materials are diamond suspensions or Al_2O_3 solutions.

The specimens to be thinned are mounted on a glass carrier, using a dedicated mounting wax. Silicon devices with variable dimensions, or even parts of wafers,

can be mounted on this carrier. (Maximum total bonding surface on the carrier is 4 inch in diameter.)

Once the devices are mounted on the glass carrier, the carrier is fixed on the JIG on a vacuum chuck. During operation this JIG is placed face down in the roller arm on the lapping/polishing plate. The JIG creates and maintains a parallel material removal as the vacuum chuck is parallel to the lapping face. During lapping a good indication of the total material removal is monitored by the analogue dial gauge. Pressure on the samples during operation is maintained by a weight, and can be set from 100 g up to 2.5 kg. Increasing the load on the samples will increase the material removal rate.

6.3.2 Thinning process

The individual chip thinning process is a combination of a lapping and a polishing process. The first stage is a lapping process which has a much higher material removal rate, while the second stage is the polishing process which has a lower material removal rate but ensures a much smoother surface finish.

Lapping is actually the wearing away of material by abrasion from a free flowing slurry or fixed abrasive pad. This process produces a non reflective matt surface.

Polishing is the removal of surface damage usually created during lapping to produce a higher surface quality. It produces a reflective surface.

The surface roughness produced in the lapping stage is dependent on the abrasive particle size and the hardness of the material. The surface roughness produced in the polishing stage is dependent on the polishing method. Details and optimization for the different process steps are discussed below.

Chip mounting

Before starting the thinning process the die(s) have to be prepared and fixed, face down, on the 4 inch glass plates. For this temporary bonding on the glass carriers, wax can be used. Three different waxes were compared: quartz wax, thin film bonding wax, glycol phtalate (all supplied by Logitech). Quartz wax can be applied on hot plate at 90°C, the thin film wax at 120°C and the glycol phtalate at 130-140°C.

The higher the wax melting point, the higher the viscosity and the better the edges of the silicon dies will be protected by the wax during the thinning process. The lower the wax melting point, the lower its viscosity and the easier to control the final thickness of the wax film between the chip and the glass carrier.

Best results were achieved using the thin film wax with melting point at 120°C. All processing is optimized using this mounting wax. This thin film wax is available as a stick. The rigid glass carrier is heated on a hotplate at 120°C and a

small amount of wax is melted on this glass substrate. Next, the dies are placed manually on the carrier. After mounting, the wax has to cool down to harden. Finally thickness of chip + wax, and thickness variation over the chip surface or between different chips (if more chips are mounted) is measured with a digital measurement unit Millitast 1082, as shown in Figure 6.3.

Figure 6.3: Thickness measurement of die with thickness of 495 μm, mounted on a rigid glass carrier, by means of a digital measurement unit

During the whole thinning process, the devices stay on the glass carrier. To release the thinned devices after processing, the wax can easily be solved in a dedicated wax solving solution, Ecoclear (Logitech), heated at 70°C. Possible remaining wax residues can be removed form the Si surface by rinsing the thinned dies in acetone.

Lapping

The first phase of the chip thinning process is a lapping process. Most of the material is removed during this process step: the material removal rate is higher than during the polishing process, but the lapping introduces a lot of surface damage at the backside of the devices.

For lapping the silicon devices a glass lapping plate is used in combination with aluminum oxide as abrasive material. The aluminum oxide solution is supplied by the autofeed cylinder. This cylinder is rotating during operation, keeping the aluminum oxide in suspension, and adds the slurry to the plate (see also Figure 6.2).

The aluminum oxide abrasive is a mixture of 15 percent by volume of Al_2O_3 powder in water. This Al_2O_3 powder for lapping is available in different particle sizes, ranging from 3 up to 20 microns. The large particle size is suitable for rough lapping, while the smaller particles ensure a finer lapping operation. The larger the particles, the higher the material removal rate, but the more damage will be introduced in the silicon wafer surface. So the thicker the layer which will have to be removed during the slower polishing process step. Using e.g. the 20 micron Al_2O_3 grain size the lapping time will be quite short, but the polishing time would be much longer. Our chip thinning lapping process parameters were optimized using 9 micron aluminum oxide solution.

Rotation speed of the drive plate can range from 0–70 rpm. The higher the rotation speed, the higher the material removal rate.

Before operation also the pressure the JIG applies on the samples has to be set. Pressure is applied by a weight and can be ranged from 100 g up to 2.5 kg. Increasing the load, increases also the material removal rate. Applying too much load at too high speed on the silicon devices can cause severe damage at the edges of the dies. Figure 6.4 shows an example of damage on the samples by the application of too much weight on the chips: the edges of the outer chips are destroyed. (A weight of 1200 g was applied with a speed of 15 rpm.) Optimal settings are found to be 350–500 g at a rotation speed of 10 rpm.

Of course the silicon removal rate is also dependent on the total silicon surface to be thinned: both die size as the number of dies mounted on the same glass carrier are variable.

The process was initially optimized for a silicon display driver die of 6.4 x 6.4 mm^2 (more information on this specific die can be found in [12]). Optimized parameters for the lapping process for 1 individual die are: rotation speed of 10 rpm, load 350 g. These settings result in a removal rate of 20–25 μm per minute.

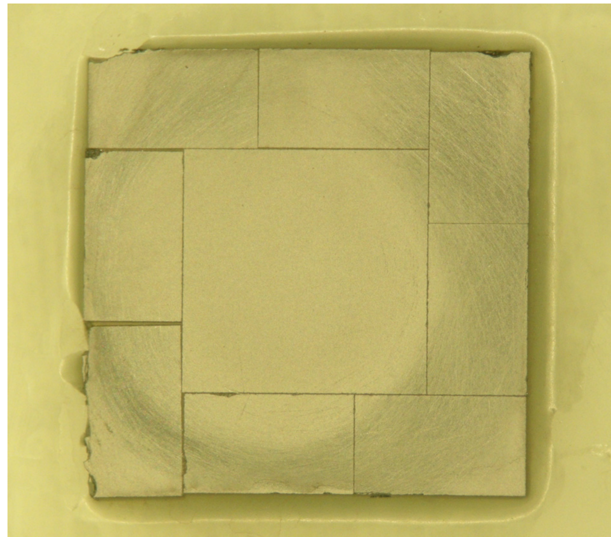


Figure 6.4: Edges of chips damaged during the lapping process

Figure 6.5 shows the very flat profile of a die after lapping (silicon was thinned from 500 μm down to 90 μm), measured with a non-contact profiler (Wyko NT 3300, Veeco Instruments). This illustrates the planarization properties of the lapping process: maximum total thickness variation (TTV) in X direction is only about 1 μm over a total length of 6 mm.

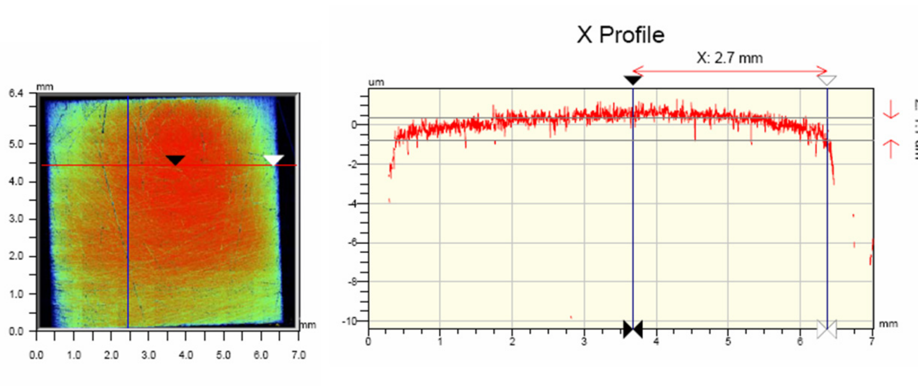


Figure 6.5: Profile of display driver chip lapped from 500 μm down to 90 μm

Surface roughness is also measured after lapping with the profiler, scan area 90 x 120 μm^2: R_a surface roughness is about 181-182 nm (Figure 6.6).

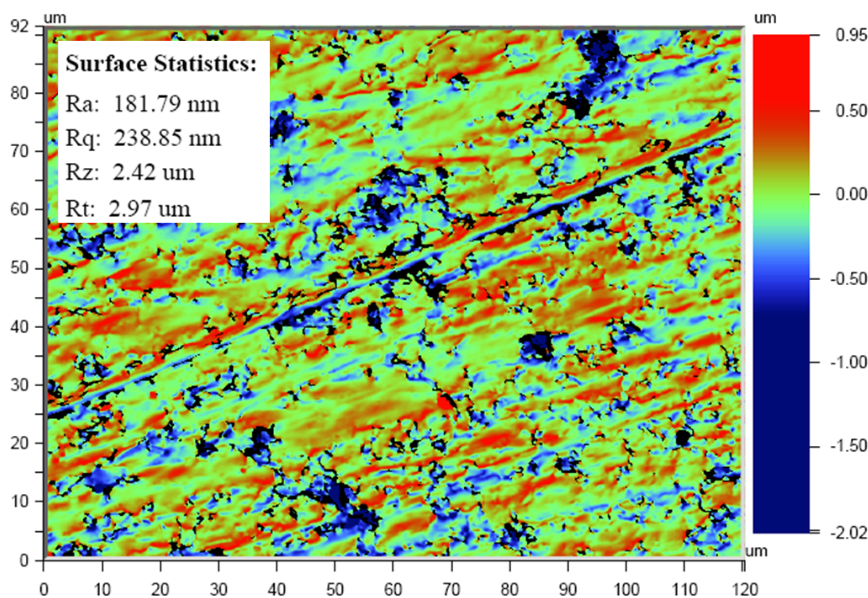


Figure 6.6: Surface roughness of a lapped silicon device

More thinning results and parameters are given in a dedicated section below.

Polishing

The second part of the chip thinning process is a polishing process. The polishing process removes the damage introduced during lapping and ensures a smooth back surface finish. The polishing has a much lower material removal rate, but ensures a nice surface finish without any damage. This is important to increase the fracture strength, especially for the very thin silicon devices [6].

The silicon chip polishing is not done mechanically but is a chemo-mechanical process. It is a combination of a chemical etching and mechanical material removal. A soft polyurethane plate is used in combination with Syton SF1 polishing solution (Logitech), with grain size of only $0.032\,\mu$m. During polishing the SF1 slurry fluid is added and ensures a chemical modification of the silicon surface. This results in a softer or more brittle silicon top layer, which is less abrasion resistant and which can be removed by the soft polyurethane polishing plate.

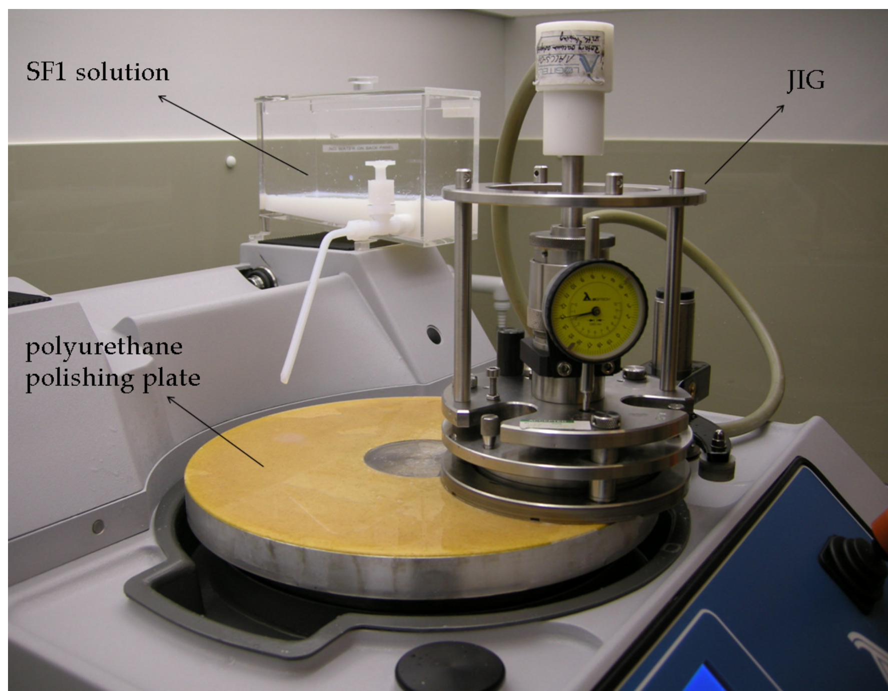


Figure 6.7: Polishing set-up on the Logitech PM5 Precision Lapping and Polishing Machine

Parameters for the polishing process are: the drive plate rotation speed (between 0–70 rpm) and the JIG load (between 100 g and 2.5 kg). The roller arm is used dynamically so that the JIG sweeps over the polishing plate.

Parameters were optimized to remove a 30 μm thick Si layer, to ensure all (sub)surface damage is removed during polishing. A critical point is the thickness difference between the middle of the die and the edges of the chip, introduced during polishing. Figure 6.8 shows a thickness profile of a driver chip after polishing (same chip as shown in Figure 6.5). Near the edges, the final thickness is about 10 to even 15 μm less then in the middle of the die. (The parameter set during polishing: load = 1500 g, 50 rpm, and no sweep.) This rounded edge phenomenem can be explained by the fact that the dies are pushed in the soft polyurethane cloth: this way, more material will be removed at the edges of the chips so the edges are rounded. The influence of load or speed on this rounding was also studied: a reduction in load or speed, or both, did not result in a reduction of the rounding of the edges.

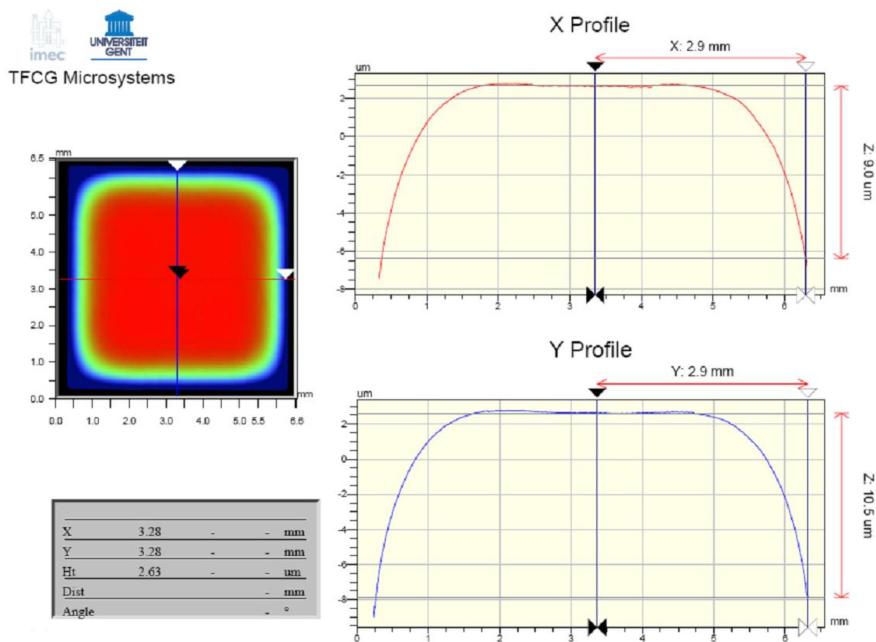


Figure 6.8: Rounded edges of thinned die after polishing

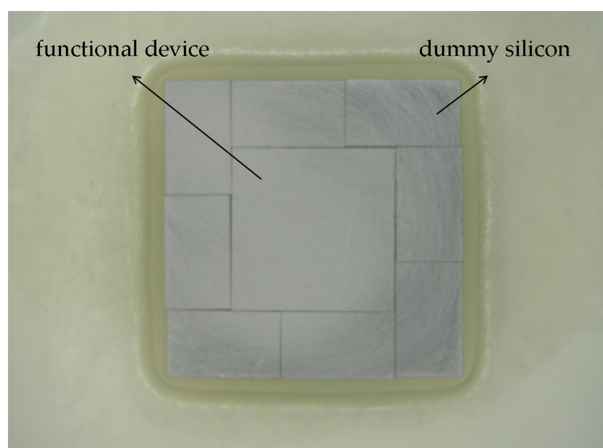


Figure 6.9: Dummies are mounted around the functional devices to protect the edges during the polishing process

This problem can be solved by mounting dummy silicon pieces around the functional devices (Figure 6.9). During polishing only the edges of the outer (dummy) silicon will be rounded and the edges of the functional, inner dies are protected. The profile of this chip after polishing is shown in Figure 6.10.

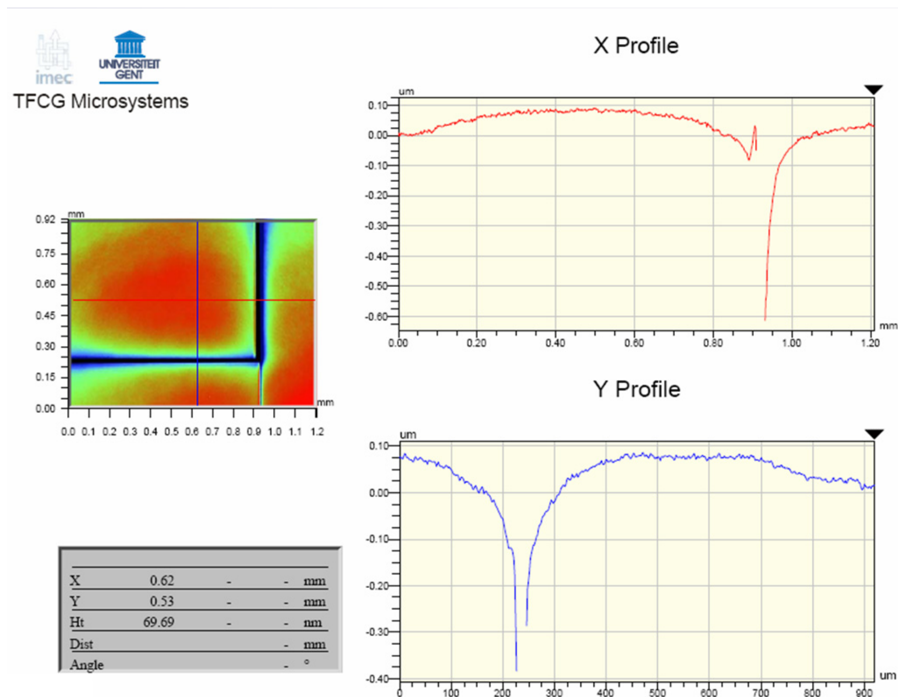


Figure 6.10: Edges of functional devices are protected during the polishing process by the surrounding dummies

As already mentioned before, the polishing process ensures a much smoother back surface finish than the lapping process. Surface roughness is measured after polishing with the Wyko NT 3300 profiler, scan area 90 x 120 μm^2: the back surface damage is removed, resulting in a R$_a$ surface roughness of about 4–5 nm (Figure 6.11).

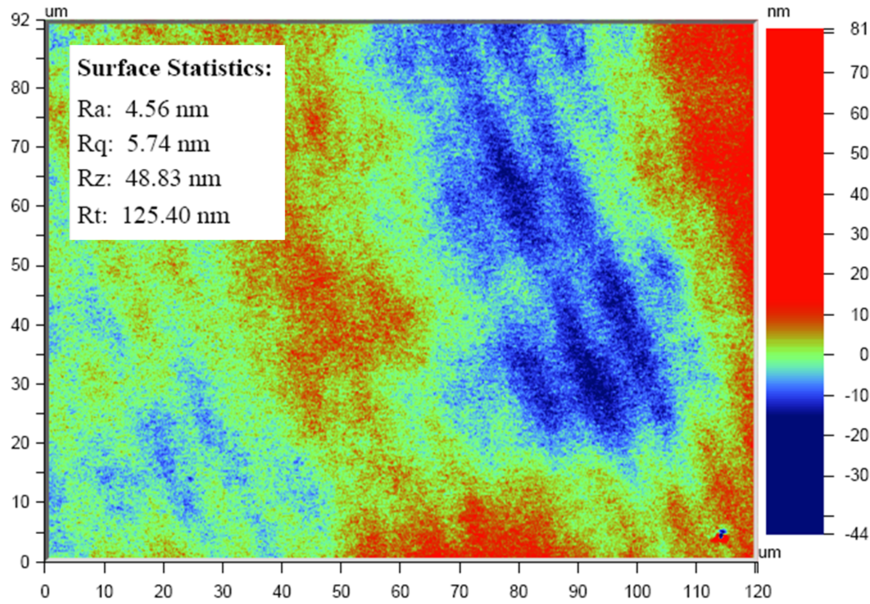


Figure 6.11: Surface roughness of a polished silicon device

6.3.3 Some thinning results

Different silicon display driver die types were available as test vehicle for optimizing the parameters for the individual die thinning process. Some results were already shown above. Figure 6.12 shows the result of the thinning down of another display driver ship: the DILA chip, for more info on this device see [13]. An unthinned chip is compared with a thinned one, the silicon is thinned from 500 μm down to 20 μm.

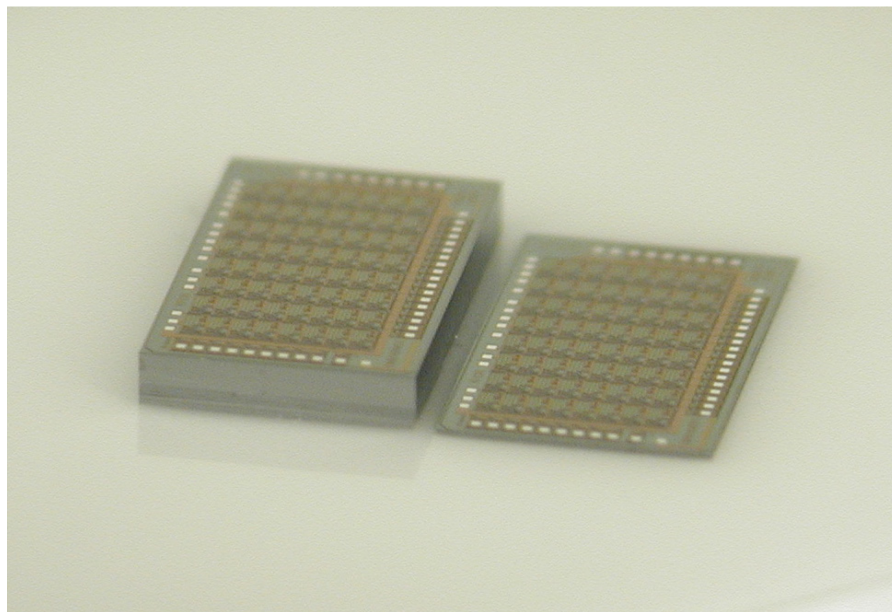


Figure 6.12: Unthinned and thinned DILA display driver chip, chip is thinned down from 500 μm down to 20 μm

These 2 types of display driver chips were used as mechanical test vehicles for optimizing the different thinning parameters and for demonstrating the feasibility of the combined lap- and polishing process. Thinned devices were only tested on visual defects.

Functional testing of thinned single dies were performed on several other types of functional dies.

Single silicon microcontroller devices of the low-power MSP430 family by Texas Instruments [14], more specifically the MSP430F149. These 3.6 x 3.8 mm^2 microcontrollers are thinned from +/- 260 μm (original dies) thickness down to 20–25 μm. The parameters for this thinning process are found in Table 6.2.

die type	MSP430F149
mounted die thickness	260 μm
die size	3.6 x 3.8 mm^2
number of dies	4
total Si surface (including dummy Si)	123.4 mm^2

lapping parameters

total time	final thickness	load	rpm	removal rate
14 min	56 μm	500 g	10	14.6 μm/minute

polishing parameters

total time	final thickness	load	rpm	removal rate
23 min	28 μm	1000 g	50	1.2 μm/minute

Table 6.2: Parameters for the individual die thinning process for thinning down the TI microcontroller, the MSP430F149

Basic electrical functional tests were performed part-time during the assembly process, see also Chapter 3, to study the influence of the thinning down of the Si for this functional microcontroller. Measurement was done with a manual needle probing setup, and verified the following items:

- power consumption is correct
- microcontroller can be programmed and retains its program (flash memory OK)
- microcontroller properly executes its program (control logic and oscillator functionality OK)

Out of 10 tested thinned samples from the first run, only 2 failed (80% yield):

- 1 sample had a large visible crack in the die (failure in the thinning process); this microcontroller draws excessive power and was not functional
- 1 sample does not retain its program (failed flash memory); possibly non-visible (subsurface) damage from thinning in some parts of the die.

These ultra thin microcontrollers were also integrated as UTCP package, and full functionality has been demonstrated.

More extensive tests were also performed on the characterization of the analog-to-digital converter on these thinned microcontrollers, for monitoring possible effects of the silicon back thinning. These measurements did not indicate any

measurable degradation after thinning. All differences are within measurement error, see also Section 3.4.3.

Also silicon radio chips have been thinned down using this individual die thinning process: the Nordic radio chip nRF2401A [15]. The 2089 x 2314 μm^2 chips are thinned from about 250 μm to 25 μm. Typical parameters for this thinning process are found in Table 6.3.

die type	nRF2401A
mounted die thickness	260 μm
die size	2089 x 2314 μm^2
number of dies	4
total Si surface (including dummy Si)	115.3 mm^2

lapping parameters

total time	final thickness	load	rpm	removal rate
17 min	48 μm	500 g	10	12.5 μm/minute

polishing parameters

total time	final thickness	load	rpm	removal rate
10 min	28 μm	1000 g	50	2 μm/minute

Table 6.3: Parameters for the individual die thinning process for thinning down the Nordic radio chip nRF2401A

These thinned chips were first UTCP embedded before testing. Functionality has been demonstrated to be similar to the behavior of an unthinned die. For more details see also Section 3.5.4.

The thinning process has also been used for thinning 1.6 x 55 mm^2 STeDrive026 driver chips. The dies are thinned from original die thickness (+/- 620 μm), down to 24 μm. (Functionality of the drivers was not tested after thinning.) The parameters for this thinning process are given in Table 6.4. Note that in this experiment the removal rates dropped significantly because of the increased total Si surface.

die type	STeDrive026
mounted die thickness	620 μm
die size	1.6 x 22 mm^2
number of dies	8
total Si surface	281.6 mm^2

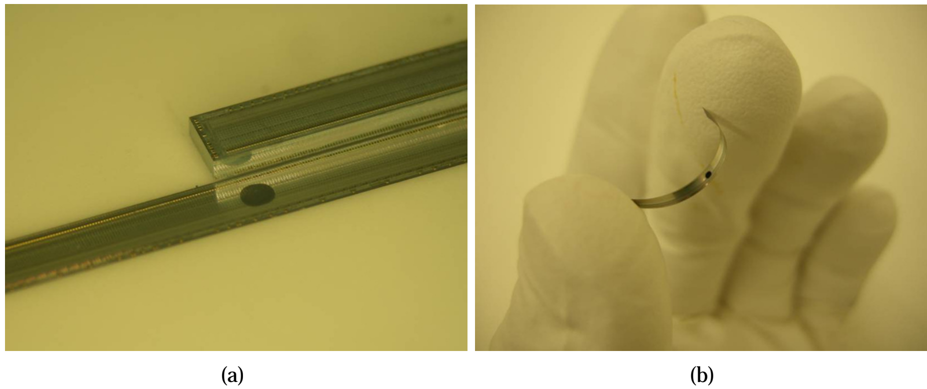
lapping parameters

total time	final thickness	load	rpm	removal rate
90 min	45 μm	500 g	10	6.4 μm/minute

polishing parameters

total time	final thickness	load	rpm	removal rate
60 min	24 μm	1000 g	50	0.35 μm/minute

Table 6.4: Parameters for the individual die thinning process for thinning down the STeDrive026 driver chip



(a) (b)

Figure 6.13: Thinning result of 1.6 x 55 mm^2 silicon chip

Also extremely small silicon Micro Electro Mechanical Systems (MEMS) devices are thinned using this individual die thinning process. SiTime SiT0100 resonators [16] (dimensions: 640 x 810 μm^2) were thinned successfully from the initial thickness of 140 μm down to thickness of 40 μm, with only minimal damage and no change in operational characteristics [17]. The parameters for this thinning process are given in Table 6.5.

die type	SiT0100
mounted die thickness	140 μm
die size	640 x 810 μm^2
number of dies	7
total Si surface	45.6 mm^2

lapping parameters

total time	final thickness	load	rpm	removal rate
5 min	71 μm	300 g	10	13.8 μm/minute

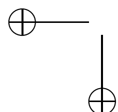
polishing parameters

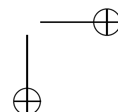
total time	final thickness	load	rpm	removal rate
17 min	45 μm	1000 g	50	1.53 μm/minute

Table 6.5: Parameters for the individual die thinning process for thinning down the SiTime SiT0100 MEMS resonators

6.4 Conclusions

Most of the silicon thinning processes available at the moment are based on wafer thinning. For research purposes it can be very interesting to be able to thin down individual dies, as full wafers with functional dies are not always accessible and full functional wafer can be extremely costly. A lap- and polishing machine was installed and the silicon backthinning processing was optimized successfully. A lapping process ensures a fast back grinding step, while the polishing process removes the back surface damage and ensure a smooth back surface finish of the die. This thinning process was demonstrated with several functional dies. Microcontrollers, display drivers, radio chips and MEMs can be thinned from original silicon thickness up to 700 μm down to thicknesses even below 20 μm, without any loss in functionality.





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Chapter 7

Thin film on flex

This chapter presents a ’thin film on flex’ technology. This technology is based on the thin film technologies, introduced for the UTCP production. A suitable process flow is established for building multilayer RF structures by repetitive application of polyimide layers by a spin-on process and metal layers by sputtering. All technology development and process optimization work of the different process steps for this build-up are discussed in detail.

7.1 Concept

The thin film technologies, used for the production of the UTCP package, can also be used for the production of ultra-thin, extremely flexible polyimide substrates. Multilayer structures will be built-up on temporary rigid carrier substrates by repetitive application of polyimide layers by a spin-on process and metal layers by sputtering. After processing and testing the structures can easily be released from the carrier.

The same spin-on polyimide used for the UTCP package has also been used to develop this ’thin film on flex’ process. Structures, with up to three metal layers, can be realized onto these ultra thin, extremely flexible polyimide substrates.

These very thin substrates have several advantages over traditional flex. Among these are: it allows for dense routing (thin film technologies), very fine features, very high performance and a perfect flat surface for component assembly (the thin flex is spun onto a glass carrier for later release). But this performance has also a cost penalty when compared to technologies used by the FCB or PCB industry. Techniques developed for PCB processing such as electroplating and wet etching, use much less costly equipment and remain much cheaper. Furthermore they are performed on much larger areas, resulting in lower cost per fabricated

unit area.

The idea is to realize only the high resolution parts of a given substrate with the presented thin film on flex technologies, and limit the high precision flex only to the area where needed. Next, these high-precision parts could be e.g. laminated inside larger, conventional flex substrates, with a 3D integration technology as presented for the UTCP chip packages in Chapter 4, Figure 4.1.

Although they are quite cost intensive, they offer the possibility to limit the need for high density parts of the total substrate only to a small area, realized with the thin film flex, e.g. for fine pitch flip chip or for having a high performance RF part, and they can exclude the need for a complete high density wiring board. In this sense they can become rather cost effective. This was also calculated within the European SHIFT project by the project end-user partner Oticon [1]. They will consider combining these expensive thin film flex with conventional, cheaper flex substrates for hearing aid production.

The technology will be demonstrated in this chapter for realizing RF test structures, using up to 3 metalization layers, but can be easily applied for other applications like: fine pitch interconnections, fine-pitch flip chips, resistor foils, RF parts, microstrip interconnects, etc.

In the next sections of this chapter the technological development and optimization progress will be discussed in more detail. Examples will be given based on the RF test design. This work focuses only on the technology optimization. The design and characterization work of these structures are used to demonstrate the feasibility of the presented technology but were not part of this PhD work.

7.2 Passive component integration in polyimide substrates

The thin film on flex technology will be demonstrated for the production of integrated passive devices (IPD) for RF applications. Actually, thin film technology is a known technology for IPD on wafer level, see ITRS Roadmap 2007 Edition [2].

Integrated passive devices can contain all three types of passives (R, L, and C) as well as only two or one type, or any combination. The elements can be connected to each other in order to realize a certain network, matching or filter functions or stand for their own to realize only single resistive, inductive, or capacitive functions. It is also possible to realize ground planes and transmission lines to create impedance controlled RF-signal transmission.

The use of thin film processes (spin-on polyimide - sputtered metal) technology will offer the possibility to manufacture, application specific, integrated passive devices in the following value ranges [2]:

- resistors: 10 Ω-150 kΩ (NiCr: 100 Ohm/sq)
- inductors: 1 nH–80 nH
- capacitors: +/- 25.7 pF/mm^2 (polyimide PI-2610, ϵ_r = 2.9, layer thickness: 1 μm [3]).

If these passive are interconnected by striplines, even complete RF structures can be produced with this 'thin film on flex' technology.

7.3 Process flow

The 'thin film on flex' technology is a polyimide based technology for producing flexible, ultra thin, multilayer (RF) circuits, using conventional thin film techniques. Multilayer structures can be built-up on temporary rigid carrier substrates by repetitive application of polyimide layers by a spin-on process, and metal layers by sputtering. After processing and testing, the structures can easily be released from the carrier.

The number of metal layers can vary and will be dependent on the application. The technology presented in this chapter contains three different metal layers.

Based on this 3-metal layer build-up, a suitable process flow has been established first. An overview of the different process steps is shown in Figure 7.1. The different process steps include:

A PI spincoated on rigid glass carrier

B Metal 1: sputtered NiCr/Cu

C Cu etch

D NiCr etch

E PI 2: thin capacitor dielectric

F Metal 2: sputtered TiW/Cu (+ TiW and Cu etch)

G PI 3: thick (10 m) spincoated PI layer

H Drilling of the vias to the contacts of the passives

I Metal 3: sputtered TiW/Cu, top metallization + filling vias

J Release from rigid carrier

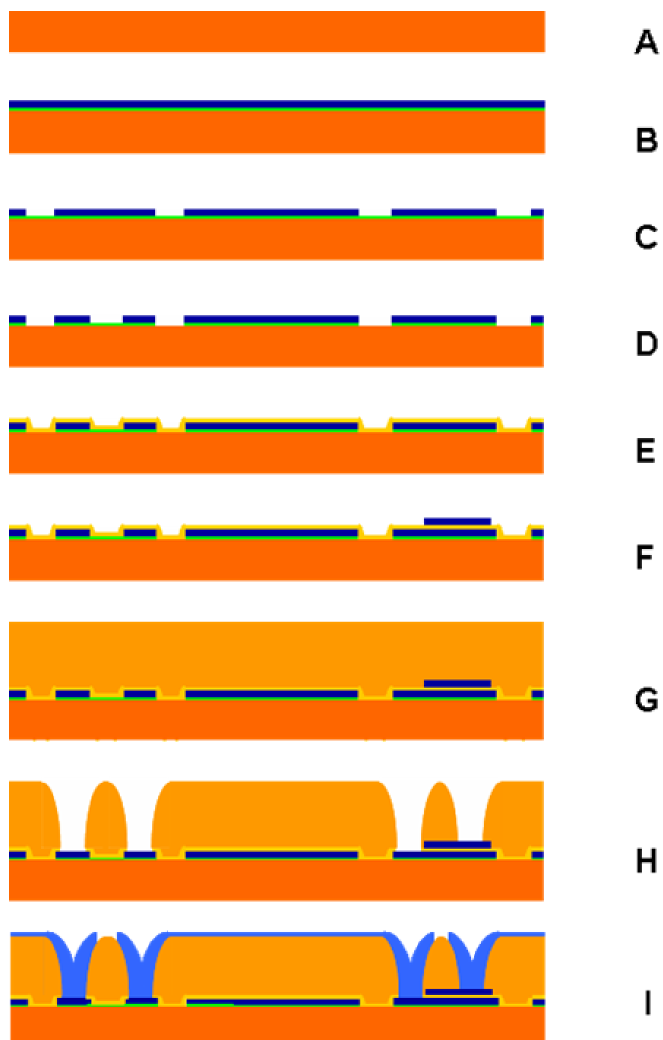


Figure 7.1: Process flow for polyimide based RF structures

The layer build-up of this thin film on flex technology consists of three polyimide layers and three metallization layers. The base substrates are polyimide spin-coated on rigid glass carrier. The first metal layer can be a NiCr Cu layer, in which resistors, inductors and bottom electrodes of the capacitors can be defined. PI 2 is a very thin polyimide layer, which is used as dielectric for the capacitors. Metal 2 is a TiW Cu layer for top electrode definition. Metal 3 is a next TiW Cu layer which provides the contacts to the test structures, but also inductors and striplines are defined here.

The different process steps will be discussed more in detail below. This technology has been developed in the framework of the European SHIFT project [4]. The application within the SHIFT project is the realization of ultra-thin bendable RF structures. All design and the characterization work for these RF structures was done by Steven Brebels from IMEC Leuven, but were not part of this PhD dissertation.

In the next section you find first some information on the different designs for this technology. These designs are also used during the technology development work, which is discussed in the next sections more in detail.

7.4 Design

As presented in the section above, a suitable process flow has been established to be able to produce ultra-thin, high precision flex substrates using conventional thin film technologies.

The number of metal layers can vary; the proposed process flow will be developed for having up to three different metal layers. The first metal layer will also have sputtered NiCr as resistive material, so also resistors can be produced with the thin-film on flex technology.

Based on this proposed layer build-up different test designs were made by the colleagues of IMEC Leuven. The first test design was used during most of the technology optimization work, and is presented in this section.

7.4.1 First test design

The first RF passive test cells for the thin-film on flex technology, designed by IMEC Leuven, are shown in Figure 7.2. Red lines are added on the picture to show the different component types. Also the direction of numbering is indicated.

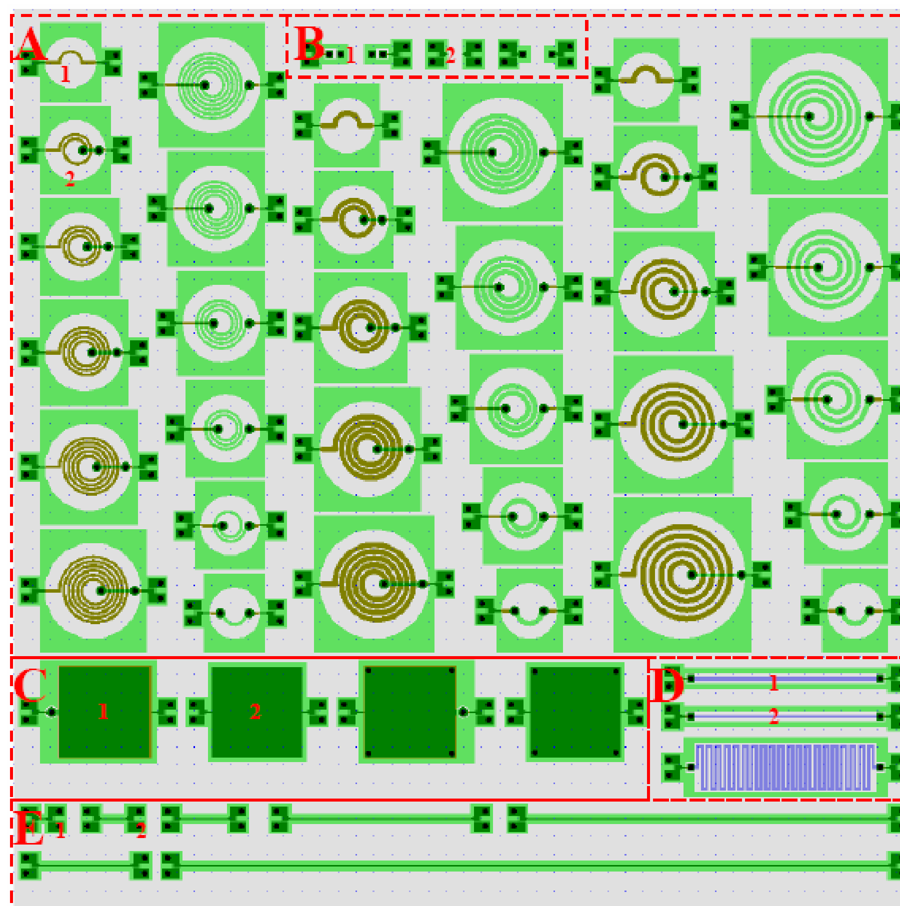


Figure 7.2: Layout of test cell with different RF test structures

This design is subdivided in 5 different test structures:

A spiral inductors with variable width, spacing and number of turns

B SOLT calibration structure

C series and shunt capacitors on Metal2 and Metal3

D straight and meandered resistors

E 24 μm wide microstrip transmission lines

These different test structures will be presented more in detail below. For each structure ground-signal-ground (GSG) contact pads are foreseen for use with coplanar waveguide launching (CPW) wafer probes. The design of these GSG pads is depicted in Figure 7.3. Probes with pitches between 100 and 250 μm can be used. The contact pad will give a low loss transition from the coplanar probe to the microstrip interconnect lines. Short-Open-Load-Thru (SOLT) structures are also available on the test cell. These structures will allow the full characterization of the parasitics of the contact pad such that they can be subtracted from the measurements.

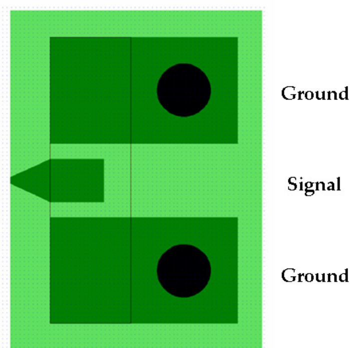


Figure 7.3: Ground-signal-ground contact pad layout

Spiral inductors

The spiral inductors are numbered from top left to bottom right, as indicated on Figure 7.2. All inductors have a spacing of 300 μm between spiral inductor and ground plane and an inner diameter of 450 μm. Table 7.1 gives an overview of the width and spacing for the different spiral inductors. The inductors are defined in Metal 1 and Metal 3, see Table 7.2. The number of turns of the different inductors is given in Table 7.3.

Width [μm]	Spacing [μm]	Component numbers
50	50	1–12
100	50	13–22
100	100	23–32

Table 7.1: Width and spacing for the different spiral inductors

Layer	Component numbers
Metal 3	1–6, 13–17, 23–27
Metal 1	7–12, 18–22, 28–32

Table 7.2: Spiral inductor: layer position

Number of turns	Component numbers
0.5	1, 12, 13, 22, 23, 32
1.5	2, 11, 14, 21, 24, 31
2.5	3, 10, 15, 20, 25, 30
3.5	4, 9, 16, 19, 26, 29
4.5	5, 8, 17, 18, 27, 28
5.5	6, 7

Table 7.3: Spiral inductor: number of turns

SOLT calibration structure

The component numbers for the Short-Open-Load-Thru calibration structure are given in Table 7.4. These structures allow the full characterization of the parasitics of the contact pad, such that they can be subtracted from the measurements.

Description	Component number
Short	B3
Open	B2
Load	B1
100 μm Thru	E1

Table 7.4: Short-Open-Load-Thru calibration structure numbering

Series and shunt capacitors

The capacitors are square shaped, with 2000 μm width and length. The bottom plate is on layer Metal 1. The top plate can be on layer Metal 2 or Metal 3, the type of capacitor can either be shunt or series, see Table 7.5.

Component number	Layer of top plate	Capacitor type
1	Metal 3	Series
2	Metal 3	Shunt
3	Metal 2	Series
4	Metal 2	Shunt

Table 7.5: Capacitors

Resistors

Resistors can be straight or meandered, line width 50 or 100 μm, see Table 7.6.

Component number	Description
1	Straight, width: 100 μm, length: 4050 μm
2	Straight, width: 50 μm, length: 4050 μm
3	Meandered, width: 50 μm, pitch: 150 μm, meander width: 950 μm, 19.5 meanders

Table 7.6: Resistor test structure design

Microstrip transmission lines

All microstrip transmission lines have a line width of 24 μm. The length of the different transmission lines are given in Table 7.7.

Component number	Length [μm]
1	100
2	500
3	1000
4	4000
5	8000
6	2000
7	15700

Table 7.7: Length of microstrip transmission lines

A cross sectional view of an integrated resistor, series capacitor and inductor is depicted in Figure 7.4.

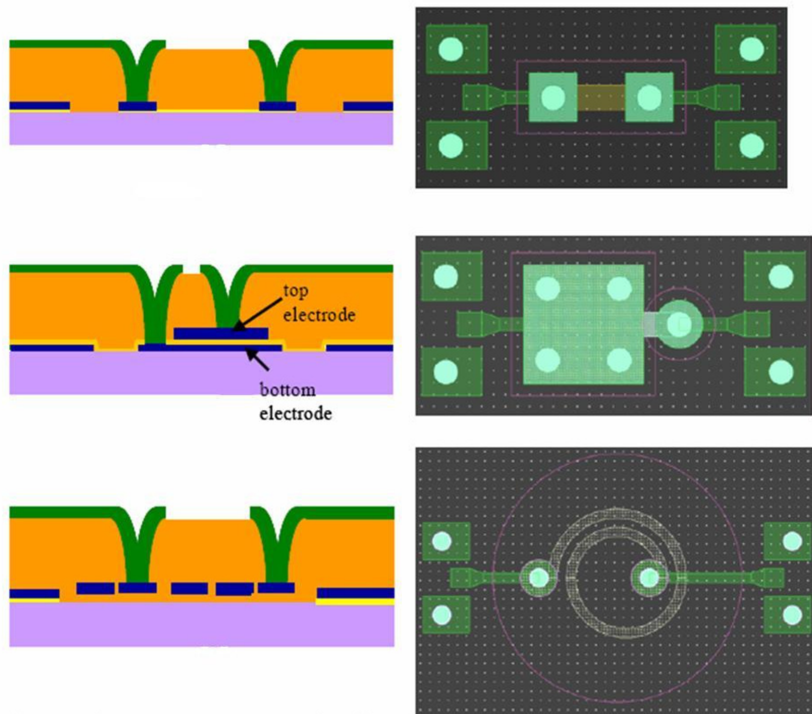


Figure 7.4: Integrated passives on flex cross section (left) and top view (right), from top to bottom: resistor, series capacitor and inductor

7.5 Process optimisation

This section discusses the individual process steps for realizing ultra thin, flexible, high resolution, RF structures (including 3 polyimide layers and 3 metal layers).

7.5.1 Base substrates - PI 1

The substrate preparation is similar to the substrate preparation for the UTCP technology as described in Chapter 2.

The base substrate is a 10 μm PI layer (PI-2611), deposited on a 5 cm x 5 cm rigid

glass carrier. After processing, the RF structure will be released from the rigid carrier. An easy release of the package from the rigid substrate is obtained in a special way: before spinning the first polyimide layer, the 4 edges of the square glass substrate are coated with an adhesion promoter (the VM652 from HD Microsystems). The consequence of this is that the first layer of polyimide adheres well to the edges of the substrates, and has marginal adhesion strength to the centre of the substrate. However, the adhesion to the edges is sufficient to allow for the whole process cycle. After processing, the multilayer structures can easily be cut out from the rigid carrier. With this release technology, the RF structure can be carried on this rigid substrate during the whole processing cycle. This makes it possible to make use of very fine pitch thin-film techniques during processing, and also to test the structures on the rigid carrier before release, using standard (rigid) test equipment.

All described processing is done on Selected White Float glass (from Praezisions Glas and Optik GmbH [5]).

The 5 cm x 5 cm glass substrates are first cleaned thoroughly before the application of the adhesion promoter. An RBS 25 cleaning agent based cleaning procedure is followed in order to remove all greases and other dirt:

- put substrates in 5% RBS solution for 12 hours
- ultrasonic agitation (USA) during 5 min in RBS
- rinse two times in DI water
- USA during 5 min in DI water
- rinse two times in isopropanol
- rinse in DI water
- dry with N_2 gun.

This extensive cleaning of the glass substrates is required to avoid hydrophobic problems during the application of the adhesion promoter.

As described above, an adhesion promoter, VM652, is applied at the edges of the glass substrates: only a border of 1–2 mm of the substrates is coated with the adhesion promoter. Application is done manually by means of a very fine syringe. (Alternatives for this deposition include dispensing or dipcoating.) The adhesion promoter is dried on a hotplate for 1 minute at 120°C.

In the next step, the polyimide is applied on the selectively coated glass substrates. The desired total thickness of the base polyimide layer is 10 μm. This layer will be built up from two, 5 μm thick, polyimide PI-2611 layers, spincoated at 3000 rpm for 45 s after a short spread at 500 rpm for 5 s. The reason for spinning the polyimide always at 3000 rpm is to limit the edge bead, i.e. a local thicker

layer of PI at the edge of the substrate after spincoating. Too large edge bead could limit the achievable resolution, during the fine pitch lithography steps.

The first polyimide film is spincoated and cured first, before the next polyimde layer can be applied. The PI-2611 is cured up to 350°C in vacuum oven, following the standard curing cycle:

- heating from room temperature to 200°C, with a ramp rate of 4°C per minute
- 30 minutes at 200°C
- heating from 200 to 350°C, with a ramp rate of 2,5°C per minute
- 60 minutes at 350°C
- gradual cooling down to room temperature

During the cure of the polyimides a small N_2 flow rate (5 sccm) is added to enhance the evaporating water and solvents removal.

In order to ensure good adhesion of the second polyimide layer on the first, cured, polyimide layer a RIE (Reactive Ion Etching) treatment is applied: see Chapter 2. Parameters for this RIE are: first 2 minutes with a 5 sccm CHF_3/20 sccm O_2 gas mixture, followed by a 2 minutes 25 sccm oxygen plasma; both applied with a power of 150 W and a pressure of 100 mTorr. After this RIE, the second polyimide layer is spincoated and cured, using the same parameters as the first polyimide layer.

7.5.2 Metal 1

The first metal layer is a sputtered NiCr/Cu/TiW stack. This layer will be used for defining resistors, inductors and bottom electrodes for the capacitors. NiCr (80% Ni, 20% Cr) is used as resistive material, with a target layer thickness of 20 nm, in order to have a sheet resistance of 50 Ω per square. A 1 μm Cu will be used for the contacting of the RF components and for the interconnections between the different components. (Cu has a low resistivity, see Table 2.15.) On top of this an thin additional 50 nm TiW (10% Ti, 90% W) is sputtered. This TiW top layer can protect the Cu layer against oxidation during processing and PI curing, and will ensure better contacting to Metal 3 layer.

This metal stack can be sputtered during the same sputter cycle, by DC magnetron sputtering in an Alcatel SCM600 system. Parameters for the NiCr sputtering are given in Table 7.8, parameters for the Cu and the TiW are found in Table 2.16.

	Pressure Argon	Power	Thickness	Sputter Time
NiCr	1×10^{-2} mbar	1500 W	20 nm	33 s

Table 7.8: Sputter parameters for NiCr deposition (for the Alcatel SCM600)

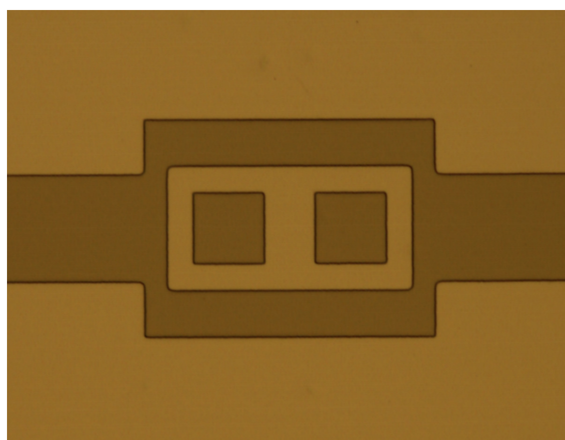
Before sputtering, the polyimide is first plasma treated during RIE to ensure increased adhesion, using the same parameters as discussed in Chapter 2 (2 minutes with a 5 sccm-CHF_3/20 sccm-O_2 gas mixture, followed by 2 minutes 25 sccm oxygen plasma; both applied with a power of 150 W of and a pressure of 100 mTorr).

After sputtering, the NiCr/Cu/TiW metal stack is photolithographically patterned. Lithography is done using a positive photoresist S1818 (Rohm and Haas Electronic Materials) with following parameters:

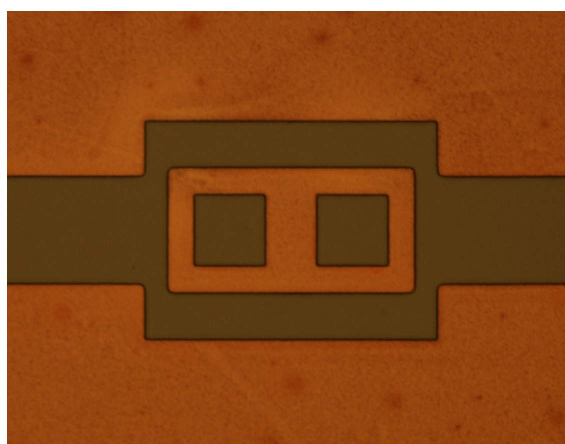
- spincoating: 4000 rpm / 60 s (typical layer thickness: 1.8 μm)
- pre-exposure bake: 90°C / 30 min in oven
- illumination: mJ/cm^2 (7.5 s)
- development: 25–30 s
- postbake: 120°C / 30 min oven.

The TiW is etched for about 10 seconds in 30% H_2O_2 (50°C) and next for 10 seconds in a cold 30% H_2O_2 solution. The Cu layer is etched in a $FeCl_3$ solution (25 g of $FeCl_3$ in 1.5 l DI water). This etching is done dynamically, in a beaker, for about 3–4 minutes.

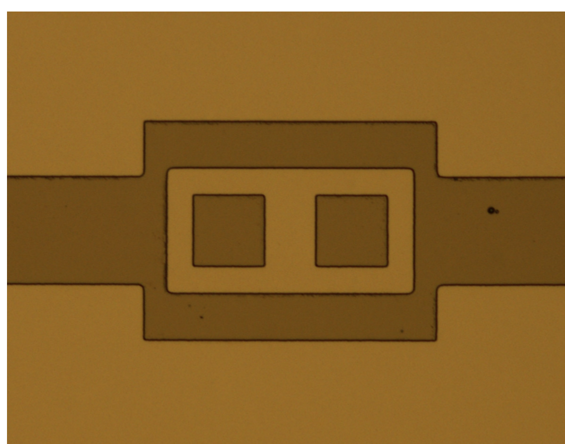
In the next step, the NiCr will be etched. Problem is that most of the suitable etchants for NiCr also contain Cu etching chemicals. Different etchants were compared by Lernout [6]. In this study, best results were achieved using a $Ce(SO_4)_2.2(NH_4)2SO_4.2H_2O$ + $HClO_4$ saturated solution. During the NiCr etch step, the remaining Cu will also be protected, since the Cu would be attacked by this NiCr etchant. Protection of the Cu is achieved during the second lithographic step after Cu etching (using the same photoresist and parameters as for the first lithographic step): the second mask oversizes the dimensions of the Cu contact pads, so that the photoresist is covering the edges of the Cu pattern.



(a) Lithography on sputtered Metal 1



(b) Result after TiW etch



(c) Result after Cu etch

Figure 7.5: Lithography and TiW + Cu etch of resistor structure

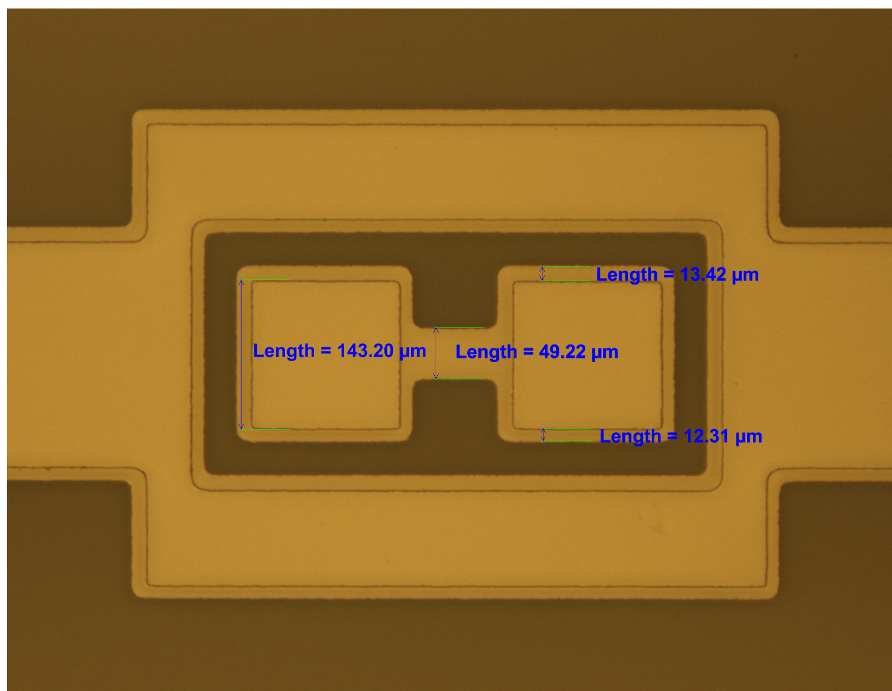


Figure 7.6: Straight resistor structure after NiCr etch, Cu was protected during NiCr etch by photoresist

Figure 7.5 shows the first process steps of a resistor structure in Metal 1: (a) lithography, (b) after TiW etch and (c) after Cu etch. Figure 7.6 shows the same resistor structure after NiCr etch. The Cu contacts were protected during this NiCr etch by photeresist. This explains the +/- 12 μm NiCr border around the contacts of the resistor.

7.5.3 PI 2

PI 2 is the second polyimide layer, which will be used as dielectric for the capacitors. A thin polyimide PI-2610 is used for this: the thinner the layer thickness, the higher the capacitance value will be. This PI-2610 is a diluted version of PI-2611 and has cured layer thicknesses between 1-3 μm: see Figure 2.2 for the spin speed curve of this polyimide.

The PI 2 for the RF test samples was always applied at 3000 rpm (5" at 500 rpm, 45" at 3000 rpm), targetting a PI-2610 layer thickness around 2 μm. Lower layer thicknesses can be achieved by further increase of the final spin speed or by using a diluted version of the PI-2610: Pyralin T9039 (HD Microsystems) is a thinner

suitable for reducing the viscosity and solids contents of the PI-2610 polyimide solution.

In order to have good adhesion of the PI 2 on PI 1, the cured PI 1 is first RIE plasma treated before the application of PI 2. Parameters for the RIE treatment are: 2 minutes with a 5 sccm-CHF_3/20 sccm-O_2 gas mixture, followed by 2 minutes 25 sccm oxygen plasma; both applied with a power of 150 W of and a pressure of 100 mTorr. Also adhesion promoter VM652 is first spincoated before the polyimide application, in order to improve the adhesion of the PI film on the Metal 1 layer. VM652 is dispensed on the sample and spin dried for 30 seconds at 3000 rpm. Next, the sample has a hotplate bake for 60 seconds at 120°C.

7.5.4 Metal 2

In this second metal layer, the top electrodes of the capacitors will be defined, using the thin PI 2 layer as dielectric. Metal 2 is a sputtered 50 nm TiW + 1 μm Cu + 50 nm TiW stack. The lower TiW ensures a good adhesion to the PI, the upper TiW protects the underlying Cu from oxidation during processing and polyimide curing. This ensures better contacting to Metal 3.

For optimum adhesion strength of the metal on this cured polyimde film, the PI 2 layer is first plasma treated before Metal 2 is sputtered.

Lithography is done using the same, 1.8 μm thick, photoresist S1818 (Rohm and Haas Electronic Materials), as for Metal 1.

After lithography, first the TiW and Cu layers are etched. The upper and lower TiW are etched for about 10 seconds in 30% H_2O_2 (50°C) and next for 10 seconds in a cold 30% H_2O_2 solution. The Cu layer is etched in a $FeCl_3$ solution (25 g of $FeCl_3$ in 1.5 l DI water). The Cu is etched dynamically in a beaker for about 3–4 minutes.

7.5.5 PI 3

The next polyimide layer is a 15 μm thick PI-2611 layer. This PI 3 layer will serve as dielectric layer for the microstrip interconnects defined in Metal 3.

Again, the RIE treatment is applied first, to have good adhesion of this polyimide layer on the previous, cured, polyimide layer. To ensure better adhesion to the metals, also the VM652 adhesion promoter is applied.

PI 3 is built-up of three 5 μm thick polyimide layers. After the RIE treatment of PI 2 and the application of adhesion promoter, the three polyimide layers are deposited by repetitive spincoating and drying. The polyimides are spincoated using the same parameters as for the PI 1 layer: 5 s at 500 rpm for spreading and 45 s at 3000 rpm for achieving the final 5 μm layer thickness. In between the spincoating of the previous layer and the application of the next polyimide layer the

samples are dried on a hotplate, with following drying profile:

- start temperature hotplate: 100°C
- heating from 100 to 200°C, with a ramp rate of 3°C per minute
- 15 minutes at 200°C
- cooling down to 100°C.

After spincoating the third polyimide layer, the polyimide PI 3 is full cured up to 350°C, following the dedicated curing cycle.

7.5.6 Via technology

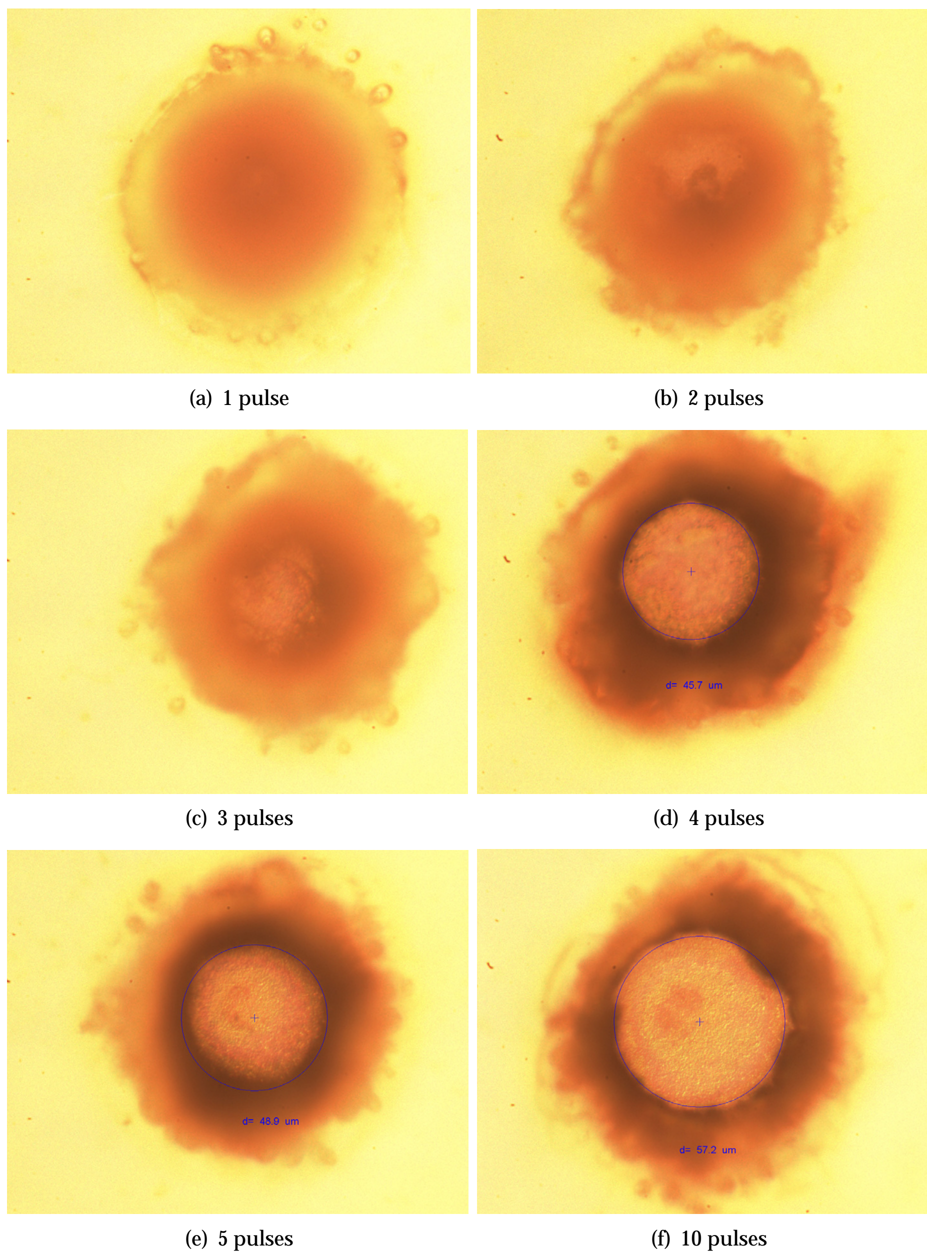
Openings to the contacts of the RF passives are opened by CO_2 laser ablation (infrared, working at 10.6 μm; see also Section 2.6). Most of the metal layers reflect the incident IR light of the CO_2 laser beam and are not ablated, this way the thin Metal 1 and Metal 2 layers will act as a laser stop.

This is clearly illustrated in Figure 7.7. It shows the CO_2 laser ablation through a 10 μm polyimide film for an increasing amount of pulses. The Metal 1 acts clearly as laser stop, Figure 7.8 shows a via after even 100 pulses: the Metal 1 layer at the bottom of this via is still not damaged.

The first test samples were produced with following laser parameters: 25 pulses. The result is shown in Figure 7.9: the vias have a bottom diameter of about 85 μm and a top diameter of 125 μm. Finally these vias were metallized for further testing and characterization. But these first samples could not be characterized because of two main problems:

- during laser drilling a lot of debris is deposited on the top surface, making litho and etching very difficult and causing shorts between the contacts of the RF components
- contacting problem at the bottom of the vias.

The first problem was caused by debris: during CO_2 laser ablation the polyimide material is removed accross the vias, but part of this ablated material can be deposited on the surface of the samples. If these impurities on the polyimide surface are not removed before sputtering the top metal, this can cause problems during the Metal 3 etching afterwords. This is illustrated in Figure 7.10: the debris caused bad etching of the metal layer, resulting in shorts between the contacts of the RF structures. This debris is difficult to remove: a rinse with acetone is not sufficient. A solution is found in the application of a thin photoresist layer (Microposit S1818) on the polyimide surface, before laser drilling. After laser drilling



(a) 1 pulse (b) 2 pulses (c) 3 pulses (d) 4 pulses (e) 5 pulses (f) 10 pulses

Figure 7.7: CO_2 laser ablation of a 10 μm polyimide film, spincoated on top of a 1 μm Cu layer, for an increasing number of pulses

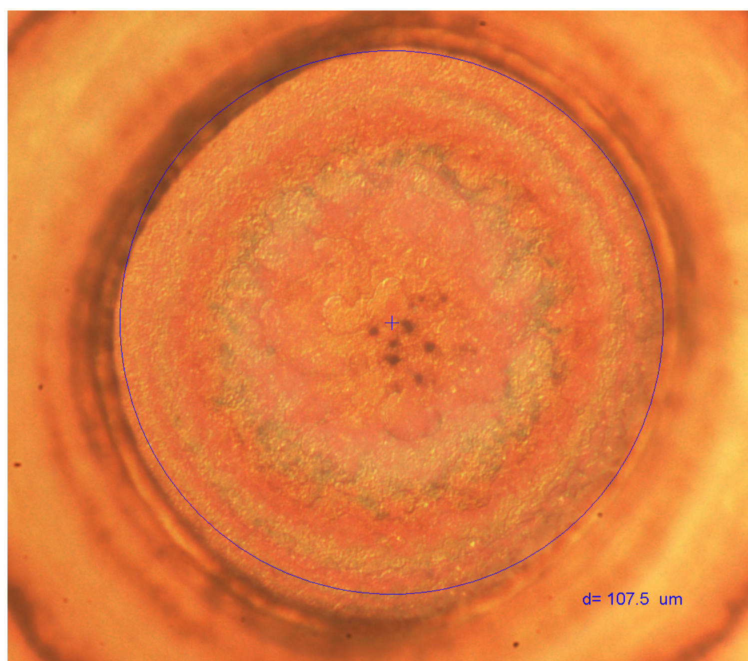


Figure 7.8: Impact of 100 pulses with CO_2 laser on Metal 1

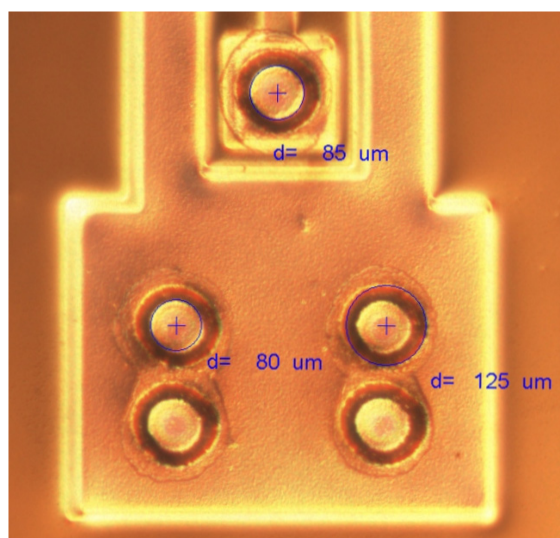


Figure 7.9: Laser drilled vias of first RF test samples

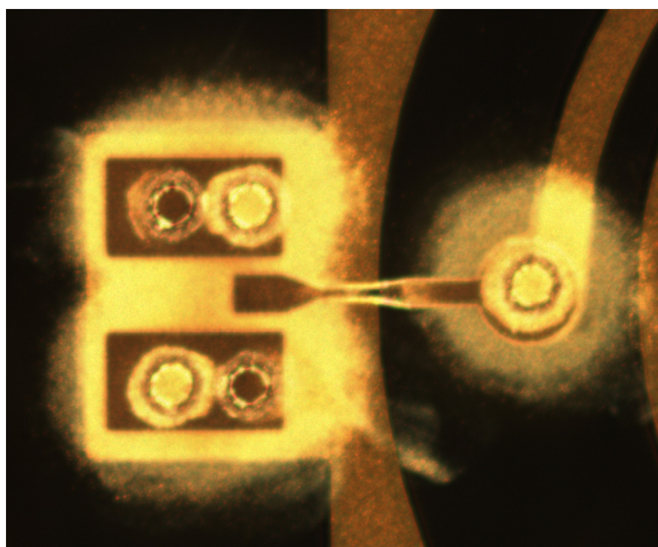


Figure 7.10: Debris deposited during ablation around the vias causing shorts at the contacts of the test structures

this photoresist can be easily stripped in acetone, removing also the debris this way. Figure 7.11 shows the result before and after photoresist strip: all the debris deposited during laser ablation has been removed from the surface by stripping the photoresist.

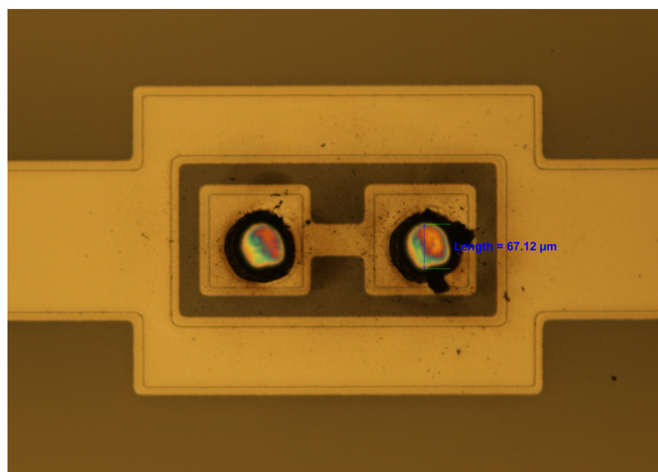
Another problem was the bad contacting to the first RF test structures. The reason for this was also discussed in Chapter 2, Section 2.6: after CO_2 laser drilling there is still a very thin, residual polyimide film at the bottom of the vias. This residual layer, at the bottom of the via, prevents later contacting to the contact pads of the chip.

A solution for this problem is found by the introduction of a 10 min RIE treatment after CO_2 laser via drilling. Parameters for this RIE are shown in Table 7.9.

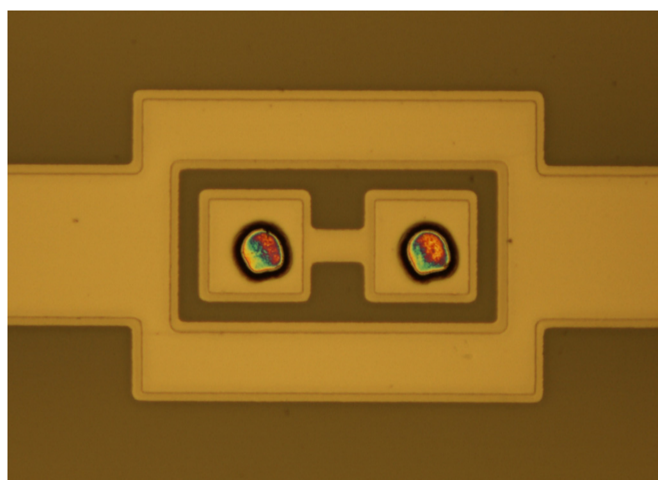
CHF_3	O_2	Power	Pressure	Time
5.0 sccm	20.0 sccm	150 W	100 mTorr	10 min

Table 7.9: RIE parameters for residual polyimide layer removal

The result, before and after the RIE etching step, is shown in Figure 7.12. This 10 min RIE treatment removes approximately 5 μm of polyimide. This means that PI 2 will be 5 μm thinner after this RIE, so original PI 2 thickness has to be



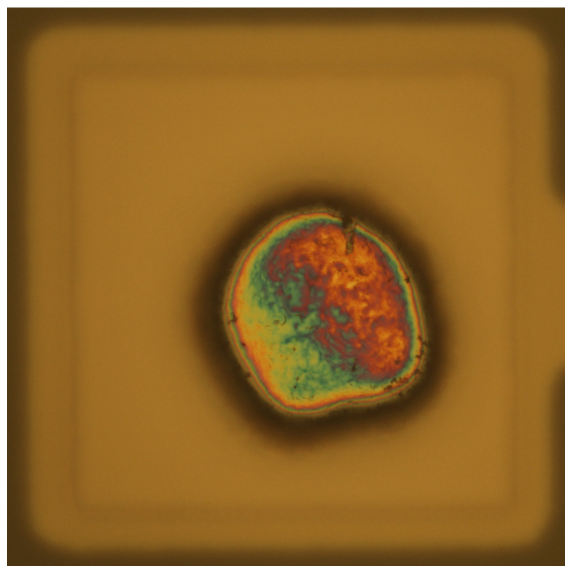
(a) Debris on photoresist



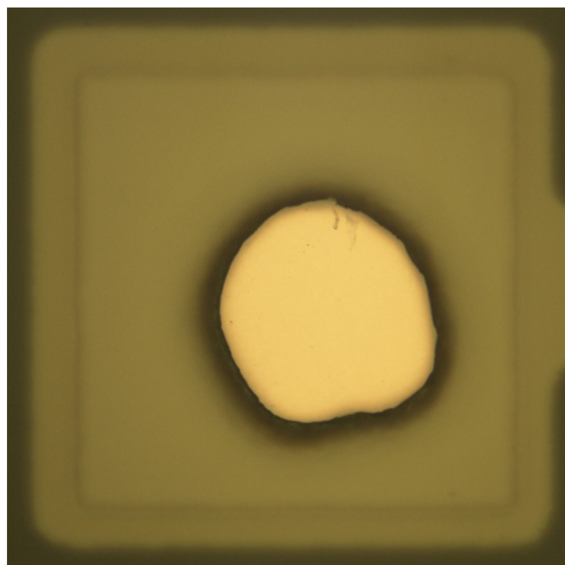
(b) Photoresist stripped

Figure 7.11: Debris is removed by stripping the photoresist after CO_2 laser drilling

5 μm more than the desired dielectric thickness.



(a) Thin residual PI film at the bottom of the via



(b) RIE cleaned via

Figure 7.12: A thin residual polyimide at the bottom of the via (a) is removed after laser drilling by 10 min RIE clean step (b) (via bottom diameter = 72 μm, top diameter = 84 μm)

As desired final thickness for PI 2 is 10 μm, a 15 μm polyimide layer is applied. Parameters for CO_2 laser drilling through this 15 μm polyimide layer are given in Table 7.10.

freq.	mask	number of pulses	demagn.	fluence
100 Hz	circular diam.: 1000 μm	50	11.41	0.928 mJ/cm^2

Table 7.10: Parameters for CO_2 laser drilling of the vias to the contacts of the RF structures

An overview of the optimised process flow for the via production for the passive embedding technology is given in Table 7.11. The different process steps are shown in Figure 7.13 for a RF test structure.

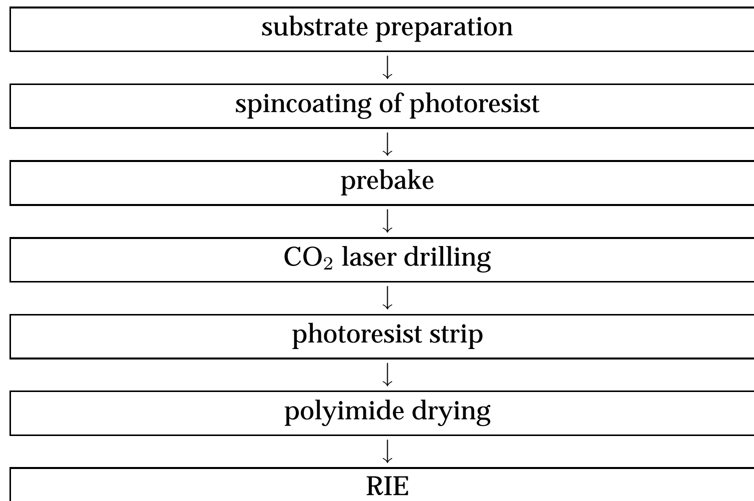
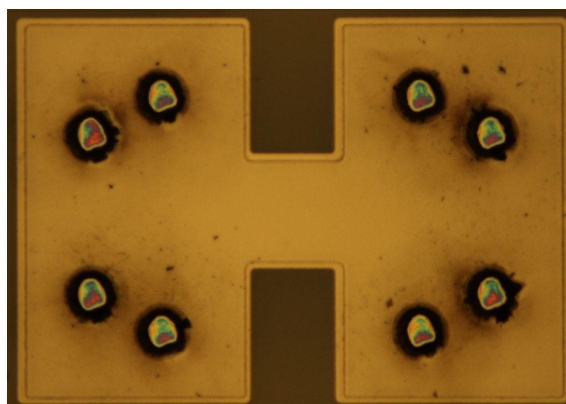
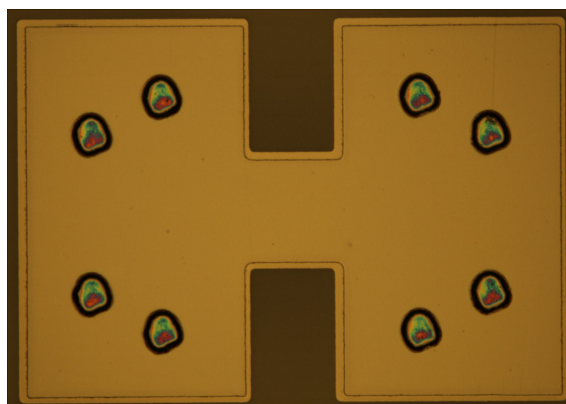


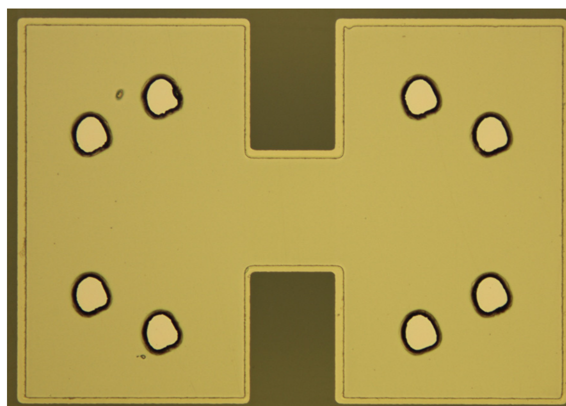
Table 7.11: Optimized process flow for via production by CO_2 laser ablation



(a) Debris on photoresist



(b) Photoresist stripped



(c) RIE residual PI film removal

Figure 7.13: Via drilling by CO_2 laser ablation to the contacts of RF test structure

7.5.7 Metal 3

After the plasma treatment, removing the residual polyimide at the bottom of the via, Metal 3 is sputtered: 50 nm TiW + 1 μm Cu.

This top metal layer provides not only the contacts to the test structures, but also inductors and striplines are defined here.

Lithography is done with the S1818 photoresist, the Cu is etched in $FeCl_3$ solution and the TiW in H_2O_2 solution.

7.5.8 Release from carrier

After processing and testing, the RF structures are easily cut out from their rigid carrier. This can be done either manually or, if more precision is desired, by laser cutting. The polyimide film releases easily from the glass substrate. Figure 7.14 shows a released RF test sample, containing resistors, inductors, capacitors and microstrip test structures (using the design shown in Figure 7.2).

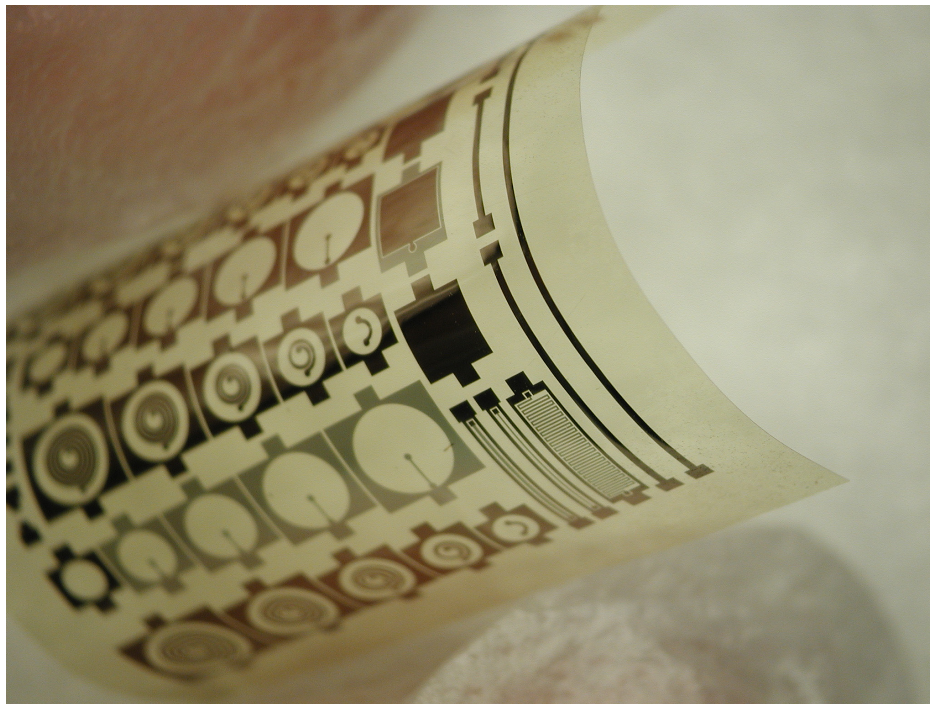
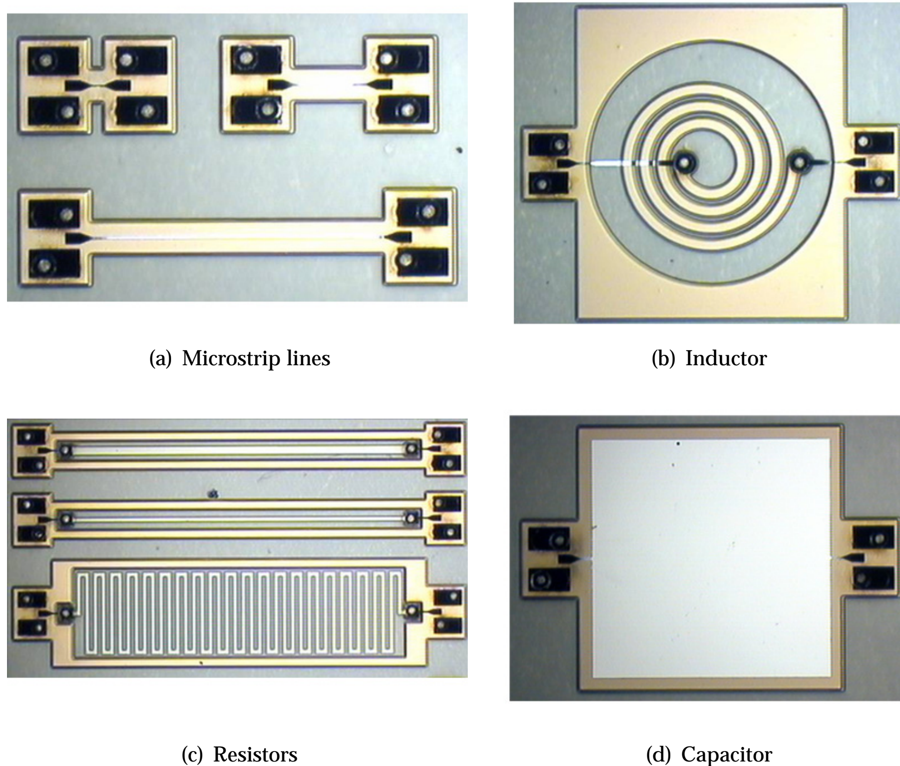


Figure 7.14: RF structure released from its carrier

7.5.9 Some realized structures

This section illustrates some examples of several realized test structures, using the, above presented, 3 metal layer thin film on flex technologies.

Figure 7.15 shows some realized microstrip lines, an inductor, resistors and a capacitor, based on the design shown in Figure 7.2.



(a) Microstrip lines (b) Inductor

(c) Resistors (d) Capacitor

Figure 7.15: Some realized RF test structures

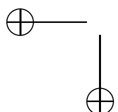
Characterization work of these test results are not covered in this PhD study, this part was done by IMEC Leuven. Characterizations are not completed yet and could, unfortunately, not be included in this chapter.

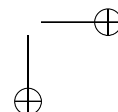
7.6 Conclusions

A 'thin film on flex' technology has been successfully developed, based on the thin film technologies used for the UTCP package production. Ultra-thin, polyimide multilayer substrates are built-up on temporary rigid carrier substrates by repetitive application of polyimide layers by a spin-on process and metal layers by sputtering. All processing and testing can be done on the rigid carrier and afterwords the structures are easily released resulting in extremely flexible, high resolution flex substrates.

A suitable process flow had been established, and a design for RF structures, based on three metal layers, have been realized with this technology. Sputtered NiCr can be used as resistor material, thin spincoated polyimide layers as dielectric for capacitors and microstrips. Metal interconnects are defined in a 1 μm sputtered Cu layer.

Design and the characterization of these test results are not covered in this PhD study, this part was done by IMEC Leuven. Characterizations are not completed yet and could, unfortunately, not be included in this chapter.





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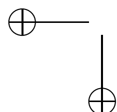
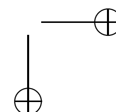

Chapter 8

Conclusions and outlook

8.1 Main achievements

In the framework of this PhD study a unique concept has been developed for integrating ultra-thin silicon devices inside multilayer substrates: the Ultra-Thin Chip Package (UTCP) technology.

Silicon devices, with thickness below 30 μm, can be packaged in between 2 spin-on polyimide layers as UTCP package. The result is a very thin, even flexible, chip package, with a total package thickness of only 50–60 μm.

The base substrate is a uniform polyimide layer, applied (spin coated and cured) on a rigid carrier. Then the ultrathin chip is placed face-up and fixed, using BCB as die attach material. Next, the second spin-on polyimide layer is applied and cured. Vias to the contacts of the chip are laser drilled and the contact metal layer is sputtered and photolithographically patterned. This metal layer is providing a fan out to the contacts of the chips. After processing and testing, the whole package is easily released from the rigid substrate.

Interconnection samples were characterized, having via resistances around 20 mΩ, and monitored during extensive reliability testing. Test samples passed 1000 h hot/humidity storage at 85°C/85 r.h., 1000 temperature cycles between -40°C/+125°C and 1000 h high temperature storage at 125°C.

Also feasibility of integrating ultra-thin functional devices has been successfully demonstrated: a TI microcontroller, MSP430F149, and a Nordic radio device, nRF2401A, did not show any decrease in functionality after UTCP packaging.

The UTCP package also enables the 3D integration of silicon devices inside conventional flex boards. The UTCP interposers have been laminated inside large commercial flex panels, and interconnected to the wiring of the board by plated through hole interconnects. Dummy package integration indicated that a 3.5 μm

metal thickness on the UTCP package is already sufficient to ensure good interconnects and that an ENIG metal finish on the UTCP samples does not affect the through hole plating quality. Daisy chain interconnects between integrated dummy packages and the FCB were characterized, and monitored during reliability investigations. High temperature storage at 150°C (up to 1000 h), hot humidity storage at 85°C/85 r.H. (up to 1000 h) and thermal cycling between -40°C and +125°C (up to 1000 cycles) did not introduce any failure to the interconnects.

This 3D technology was also used for the integration of a functional microcontroller device for a wireless ECG application. A TI microcontroller, MSP430F149, was removed from the surface of the substrate and successfully integrated inside a standard double-layer flex PCB, with even smaller SMD components mounted above and below the embedded chip, realizing a fully functional wireless biopotential system.

Also two alternative UTCP technologies were presented, both making use of photodefinable polyimide. A first technology places the chip in a cavity, photodefined in an extra polyimide inner layer, enabling for the production of flat UTCP packages. The second technology uses a photodefinable top polyimide layer for the photodefinition of 60 μm vias to the integrated chip contact pads.

A silicon thinning process was developed, for thinning down individual devices. A lap- and polishing machine was installed and the silicon backthinning processing was optimized. The lapping process ensures a fast back grinding step, while the polishing process removes the back surface damage and ensures a smooth back surface finish of the thinned die. This thinning process was demonstrated with several functional dies: microcontrollers, display drivers, radio chips and MEMs devices have been thinned from original die thickness, up to 700 μm, down to thicknesses even below 20 μm, without any loss in functionality.

A 'thin film on flex' technology, based on the thin film technologies already used for UTCP package production, was developed for the production of ultra-thin, extremely flexible, polyimide substrates. High resolution multilayer flex structures were built-up on temporary carrier substrates by repetitive application of polyimide layers by a spin-on process and metal layers by sputtering. This technology has been demonstrated with three metalization layers and has been used for realizing high resolution, high precision RF structures.

8.2 Future work

The technology described in this PhD study has been introduced in other (parallel running) projects and will be further developed.

In the first place in FP6-IP-FlexiDis, UTCP technology as flexible display driver has been explored. The aim was to combine the UTCP technology with Philips' EPLAR (Electronics on Plastics by Laser Assisted Release) technology, where a

thin-film active matrix for driving a flexible display is made on spin-on polyimide as the substrate. This results in a very flexible active matrix substrate. Integration of the display driver chips as (flat) UTCP in the same substrate would allow to maintain more or less this flexibility. In this context the flat UTCP package concept was further developed: these results will be published in the PhD thesis of Jonathan Govaerts, Ghent University.

Within the framework of the Flemish funded IWT-SBO-BioFlex project, a more advanced version of the IMEC ExG wireless sensor node demonstrator will be further developed by the 3D integration, not only of the TI microcontroller, but also of the Nordic radio device and a biopotential device, even combined with stretchable interconnects.

A logical further step for the UTCP technology is also to try to stack UTCP packages. This will create 3D chip stacks, which are as compact as TSV (through silicon via) technology stacks, and have at the same time the advantage of the less compact PoP (Package on Package) technology: the packaged chips can easily be tested and selected before stacking. 3D stacking of the thin modules will be done within the framework of the European FP7-STRP-TIPS project (Thin Interconnected Package Stacks) and is the subject of the ongoing PhD study of Enkhbold Sodov, Ghent University.

The UTCP technology can also be combined with the presented thin film on flex technology. The thin-film RF structures like striplines, microstriplines, RF passives are compatible with the UTCP technology and could be integrated on the UTCP package, very close to the integrated chip. The RF behavior of such UTCP packages and the applicability of UTCP packages for RF applications will the subject of another PhD study, starting at the beginning of 2009 (4 year PhD-grant paid by IMEC to the University of Ghent).