

# **Ontwerp van een geschakelde xDSL versterker in een submicron hoogspanningstechnologie**

**Design of a Switching xDSL Line Driver  
in a Submicron High Voltage Technology**

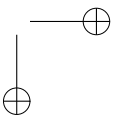
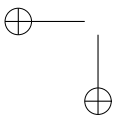
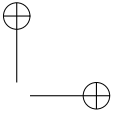
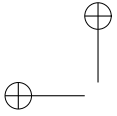
Vincent De Gezelle

Promotor: prof. dr. ir. J. Doutreloigne

Proefschrift ingediend tot het behalen van de graad van  
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Electronica en Informatiesystemen  
Voorzitter: prof. dr. ir. J. Van Campenhout  
Faculteit Ingenieurswetenschappen  
Academiejaar 2008–2009





# **Ontwerp van een geschakelde xDSL versterker in een submicron hoogspanningstechnologie**

**Design of a Switching xDSL Line Driver  
in a Submicron High Voltage Technology**

Vincent De Gezelle

Promotor: prof. dr. ir. J. Doutreloigne

Proefschrift ingediend tot het behalen van de graad van  
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Electronica en Informatiesystemen  
Voorzitter: prof. dr. ir. J. Van Campenhout  
Faculteit Ingenieurswetenschappen  
Academiejaar 2008–2009



ISBN 978-90-8578-300-8

NUR 959

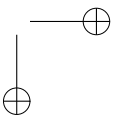
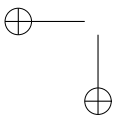
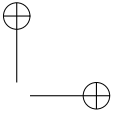
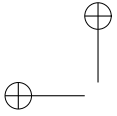
Wettelijk depot: D/2009/10.500/58



Promotor:

Prof. dr. ir. J. Doutrelaigne

Onderzoeksgroep CMST  
Vakgroep Electronica en Informatiesystemen  
Technologiepark 914A  
B-9052 Zwijnaarde



## Dankwoord

Plots zit ik daar dan, verstand op nul, blik op oneindig en een nog warme stapel vers afgedrukt papier voor mijn neus. De vaststelling dat de georganiseerde chaos die ik "bureau" noem toch eens wat opgeruimd moet worden, onmiddellijk gevolgd door de gedachte dat ik dan impulsief en met grenzeloos enthousiasme dingen weg zal smijten die ik achteraf toch nog nodig blijk te hebben. De reden voor dit alles? Na acht jaar ligt hier eindelijk een schriftelijke samenvatting van een belangrijk deel van het onderzoek en projectwerk dat ik in die periode verricht heb. Dit zou echter nooit mogelijk geweest zijn zonder de steun van een heleboel mensen.

Als eerste zou ik prof. André Van Calster willen bedanken om mij als pas afgestudeerd ingenieur op te nemen in de TFCG/CMST familie en ons van tijd tot tijd te verwennen met een diner of een BBQ. Daarnaast heeft natuurlijk ook mijn promotor, prof. Jan Doutreloigne, een belangrijke rol gespeeld, door regelmatig eens wat licht te doen schijnen in de tunnel, dit proefschrift te lezen en de nodige kritische opmerkingen te formuleren.

Dank ook aan alle collega's en ex-collega's, zonder hen was het hier maar saai geweest. Een aantal van hen zou ik toch extra willen bedanken. Jean, om de settings voor mijn designomgeving op punt te helpen zetten en mij te introduceren in een wondere wereld genaamd "Cadence". Ronny en Michiel om mij te assisteren bij de meest waanzinnige Unix-problemen en Wim om Cadence draaiende te houden. Dieter, om mij af en toe binnen te smokkelen in de cleanroom als ik weer eens microscoopfoto's nodig had van deze of gene chip. Björn voor al het wirebonden en het fijnere soldeerwerk en Lieven voor de Mentor-support.

Mijn bureaugenoten mogen natuurlijk ook niet ontbreken. Benoit voor de eerste hulp bij speciale devices en Ann om altijd opgewekt te zijn. Zangvogel Stefaan, omdat er toch iemand wat leven in de designerbrouwerij moet brengen en Pieter en Dominique om te allen tijde de kalmte te bewaren. Jodie, bedankt om af en toe eens een lastige vraag te stellen. Hopelijk heb je iets aan dit boek.

Verder wens ik ook enkele mensen van Alcatel-Lucent te bedanken. Marnix, zonder jou zou het financiële plaatje er ongetwijfeld anders uitgezien hebben. Eddy, bedankt voor de technische support, het ter beschikking stellen van een pak interessante documenten en de verhelderende uitleg over alles wat met telefonie te maken heeft.

Also a special thanks to the people of ETCA Charleroi to allow me to confiscate several power supplies, a signal generator and their spectrum analyzer for my final measurements. Philippe, Karim, Pierre-Gilles and Stephanie, thank you very much.

Naast het professionele gedeelte, zijn er natuurlijk nog mensen die mij, elk op hun manier, tijdens mijn vrije tijd gesteund hebben. De muzikanten van het ter ziele gegane Tempi Misti en opvolger Guso, door wie ik verplicht ben af en toe mijn cello nog eens af te stoffen. De “Insiders”, om te bewijzen dat er behalve whine-surfers ook nog windsurfers zijn die effectief gaan varen. Daarnaast zijn er ook nog “de mannen van Brugge” die mij af en toe meetweefelden om een ander stukje België onveilig te gaan maken.

Als laatste, maar daarom zeker niet minder belangrijk, zijn er nog mijn ouders en zus. Bedankt voor alle kansen die ik gekregen heb, voor de financiële ondersteuning, de goede raad, om mij overal naartoe te voeren of de auto te lenen, ook al wordt die dan steevast mishandeld door tientallen kilo’s aan plastic en carbon op het dak te stouwen, voor al die dingen die evident lijken maar het niet zijn. Charlotte, bedankt om te bewijzen dat een viool best wel mooi kan klinken en om mij te verblijden met weetjes zoals het aantal verschillende noten dat koolmezen en pimpelmezen kunnen produceren.

Bedankt voor alles!

Vincent De Gezelle

Gent, 12 augustus 2009

# Contents

<b>1</b>	<b>Introduction</b>	<b>1</b>
1.1	Wire line communication . . . . .	1
1.1.1	Rise of the network . . . . .	1
1.1.2	Extending the applications . . . . .	2
1.1.3	Some properties of xDSL . . . . .	2
1.2	Context and goal of this work . . . . .	4
1.3	Outline . . . . .	7
<b>2</b>	<b>Concept and verification</b>	<b>11</b>
2.1	Preliminary considerations . . . . .	11
2.2	Technology overview . . . . .	14
	DMOS transistors . . . . .	14
	MOS transistors . . . . .	14
	Capacitors . . . . .	15
	Resistors . . . . .	15
2.3	Zeroth order . . . . .	16
2.3.1	Schematics and simulations . . . . .	16
	Output stage . . . . .	16
	Comparator . . . . .	20
	Full simulation . . . . .	25
2.3.2	Layout and measurement results . . . . .	30
2.4	First order . . . . .	34
2.4.1	Schematics and simulations . . . . .	34
	Opamp and integrator . . . . .	34
	Comparator . . . . .	38
	Biasing circuit . . . . .	41
	Output stage . . . . .	45
	Full simulation . . . . .	46
2.4.2	Layout and measurement results . . . . .	55
	Reference circuit . . . . .	55
	Amplifiers . . . . .	55
2.5	Conclusion . . . . .	61

<b>3</b>	<b>Theory of operation</b>	<b>65</b>
3.1	Introduction . . . . .	65
3.2	Describing functions linearization . . . . .	66
3.2.1	Small and large signals . . . . .	66
3.2.2	Large signal approximation . . . . .	67
3.2.3	An example . . . . .	70
	Offset . . . . .	70
	Sinewave . . . . .	70
	Full response . . . . .	72
3.2.4	Sinusoidal input signals . . . . .	72
	A single sinusoid . . . . .	72
	A sinusoid with other signals . . . . .	74
	Exponential transfer revisited . . . . .	74
3.2.5	Limit cycle calculation . . . . .	75
3.3	Distortion calculation . . . . .	76
3.3.1	Zeroth and first order loop . . . . .	77
3.3.2	Second order loop . . . . .	80
3.3.3	Third order loop . . . . .	81
3.4	Numerical verification . . . . .	82
3.4.1	First order loop . . . . .	82
	Oscillating frequency . . . . .	82
	Third order harmonic distortion . . . . .	83
	Simulation . . . . .	83
3.4.2	10MHz second order loop . . . . .	86
	Oscillating frequency . . . . .	86
	Third order harmonic distortion . . . . .	87
	Simulation . . . . .	88
3.4.3	30MHz second order loop . . . . .	91
3.4.4	Third order loop . . . . .	94
	Oscillating frequency . . . . .	94
	Third order harmonic distortion . . . . .	94
	Simulation . . . . .	95
3.4.5	Discussion . . . . .	98
	Limit cycle frequency . . . . .	98
	Third order harmonic distortion . . . . .	98
	What about MTPR? . . . . .	101
3.5	Conclusion . . . . .	101
<b>4</b>	<b>Designing the loop</b>	<b>105</b>
4.1	Introduction . . . . .	105
4.2	Technology overview . . . . .	106
4.2.1	DMOS transistors . . . . .	106
4.2.2	MOS transistors . . . . .	106

**CONTENTS**

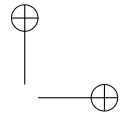
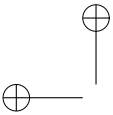
**v**

4.2.3	Capacitors . . . . .	107
4.2.4	Resistors . . . . .	107
4.3	Building blocks . . . . .	108
4.3.1	Opamps . . . . .	108
	Integrator . . . . .	108
	Voltage follower . . . . .	115
	Biasing circuit . . . . .	118
4.3.2	Comparator . . . . .	120
4.3.3	Output stage . . . . .	121
4.3.4	Time delay, level shifter and buffers . . . . .	127
4.3.5	Passive filter-divider . . . . .	130
	First order loop . . . . .	131
	10MHz second order loop . . . . .	132
	30MHz second order loop . . . . .	132
	Third order loop . . . . .	133
4.4	First order system . . . . .	133
4.5	10MHz second order system . . . . .	135
4.6	30MHz second order system . . . . .	139
4.7	Third order system . . . . .	139
4.8	Second order system with independent loops . . . . .	139
4.9	Layout considerations . . . . .	146
4.9.1	Interconnection . . . . .	146
4.9.2	Components . . . . .	147
4.10	Conclusion . . . . .	147
<b>5</b>	<b>Measurements</b> . . . . .	<b>151</b>
5.1	Introduction . . . . .	151
5.2	Initial measurements . . . . .	154
5.2.1	First order system . . . . .	154
	DC response . . . . .	154
	AC response . . . . .	154
	MTPR response . . . . .	157
5.2.2	10MHz second order system . . . . .	157
	DC response . . . . .	157
	AC response . . . . .	157
	MTPR response . . . . .	157
5.2.3	30MHz second order system . . . . .	159
	DC response . . . . .	159
	AC response . . . . .	164
	MTPR response . . . . .	164
5.2.4	Third order system . . . . .	164
	DC response . . . . .	164
	AC response . . . . .	164

---

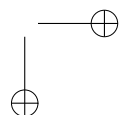
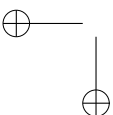
	MTPR response . . . . .	164
5.2.5	Second order system with independent loops . . . . .	170
	DC response . . . . .	170
	AC response . . . . .	170
	MTPR response . . . . .	170
5.3	Troubleshooting . . . . .	173
5.4	Final measurements . . . . .	180
5.4.1	First order system . . . . .	181
	DC response . . . . .	181
	AC response . . . . .	181
	MTPR response . . . . .	181
5.4.2	10MHz second order system . . . . .	184
	DC response . . . . .	184
	AC response . . . . .	185
	MTPR response . . . . .	185
5.4.3	30MHz second order system . . . . .	185
	DC response . . . . .	185
	AC response . . . . .	185
	MTPR response . . . . .	185
5.4.4	Third order system . . . . .	191
	DC response . . . . .	191
	AC response . . . . .	192
	MTPR response . . . . .	192
5.4.5	Second order system with independent loops . . . . .	192
	DC response . . . . .	192
	AC response . . . . .	192
	MTPR response . . . . .	198
5.5	Conclusion . . . . .	199
<b>6</b>	<b>Conclusions and outlook</b> . . . . .	<b>203</b>
6.1	Main achievements . . . . .	203
6.2	Future work . . . . .	204
6.3	Feasibility and extensibility . . . . .	204





## List of Tables

2.1	Key characteristics of I <sup>2</sup> T100 DMOS devices . . . . .	14
2.2	Key characteristics of I <sup>2</sup> T100 MOS devices . . . . .	15
2.3	Key characteristics of I <sup>2</sup> T100 capacitors . . . . .	15
2.4	Key characteristics of I <sup>2</sup> T100 resistors . . . . .	16
2.5	Transistor dimensions of level shifter and buffer . . . . .	18
2.6	Transistor dimensions of the delay circuit . . . . .	22
2.7	Transistor dimensions of the comparator . . . . .	23
2.8	Delay times of the comparator . . . . .	25
2.9	Summary of simulation results . . . . .	28
2.10	Power dissipation of the single ended amplifier . . . . .	28
2.11	Maximum dV/dt capability of the DMOS switches used . . . . .	29
2.12	Calculated dimensions of the opamp transistors . . . . .	37
2.13	Optimized component dimensions of the opamp . . . . .	38
2.14	Simulation results of the opamp . . . . .	39
2.15	Transistor dimensions of the comparator . . . . .	41
2.16	Delay times of the comparator . . . . .	41
2.17	Transistor dimensions of the reference circuit . . . . .	45
2.18	Voltages and currents from the reference circuit . . . . .	46
2.19	Transistor dimensions of level shifter and buffer . . . . .	47
2.20	Transistor dimensions of the delay circuit . . . . .	48
2.21	Summary of the simulation results . . . . .	52
2.22	Summary of the calculated results . . . . .	54
2.23	Measured voltages from the reference circuit . . . . .	56
2.24	Comparison of measurement results . . . . .	61
3.1	Bernoulli numbers . . . . .	79
3.2	Calculated and simulated limit cycle frequencies . . . . .	98
3.3	Simulated MTPR . . . . .	101
4.1	Key characteristics of I <sup>3</sup> T80 DMOS devices . . . . .	106
4.2	Key characteristics of I <sup>3</sup> T80 MOS devices . . . . .	107
4.3	Key characteristics of I <sup>3</sup> T80 capacitors . . . . .	107
4.4	Key characteristics of I <sup>3</sup> T80 resistors . . . . .	108



4.5	Final dimensions of the opamp . . . . .	111
4.6	Final dimensions of the opamp . . . . .	115
4.7	Transistor dimensions of the biasing circuit . . . . .	118
4.8	Transistor dimensions of the basic comparator . . . . .	121
4.9	Transistor dimensions of the comparator . . . . .	123
4.10	Normalized values for a third order Chebychev low pass filter with 1dB ripple . . . . .	124
4.11	Dimensions of the output transistors . . . . .	125
4.12	Transistor dimensions of the delay circuit . . . . .	127
4.13	Transistor dimensions of the low to high level shifter . . . . .	129
4.14	Transistor dimensions of the high to low level shifter . . . . .	129
4.15	Dimensions of the first order loop filter components . . . . .	132
4.16	Dimensions of the 10MHz second order loop filter components . . . . .	132
4.17	Dimensions of the 30MHz second order loop filter components . . . . .	133
4.18	Dimensions of the third order loop filter components . . . . .	133
4.19	Summary of the calculated efficiencies . . . . .	148
5.1	Maximum saturation voltage at process corners . . . . .	174
5.2	Summary of both sets of measurements on all five circuits . . . . .	200

## List of Figures

1.1	Simplified diagram of telephone interconnection . . . . .	3
1.2	Principle of DMT encoding . . . . .	3
1.3	Frequency and time domain representation of a DMT encoded signal . . . . .	4
1.4	Simplified diagram of a class G amplifier using multiple supply voltages . . . . .	5
1.5	Simplified diagram of a class G amplifier using a variable supply voltage . . . . .	6
1.6	Block diagram and corresponding waveforms of a basic PWM amplifier . . . . .	6
1.7	Example of an asynchronous mixed class AB and D amplifier . . . . .	7
1.8	Block diagram of an asynchronous class D amplifier . . . . .	8
2.1	Block diagram of an asynchronous class D amplifier . . . . .	12
2.2	Π versus T output filter topology . . . . .	13
2.3	More detailed diagram of the asynchronous class D amplifier . . . . .	13
2.4	Schematic of the high voltage output stage . . . . .	17
2.5	Simulation of the high voltage output stage . . . . .	17
2.6	Schematic of the level shifter with buffer . . . . .	18
2.7	Simulation of the level shifter with buffer . . . . .	19
2.8	Illustration of turn-on in DMOS transistors . . . . .	19
2.9	Schematic of the delay circuit . . . . .	20
2.10	Schematic of the comparator . . . . .	21
2.11	Simulation of the comparator . . . . .	24
2.12	Schematic of the loop filter . . . . .	25
2.13	Simulated output of single ended amplifier @ 200kHz reference signal . . . . .	26
2.14	Simulated spectrum of single ended amplifier @ 200kHz reference signal . . . . .	26
2.15	Simulated output of balanced amplifier @ 200kHz reference signal . . . . .	27
2.16	Simulated spectrum of balanced amplifier @ 200kHz reference signal . . . . .	27
2.17	Simulated gate and output signals of the output stage . . . . .	29

2.18	Die photograph of the amplifier processed . . . . .	31
2.19	Measured and ideal output of the asynchronous switching amplifier . . . . .	32
2.20	Efficiency of the asynchronous switching amplifier . . . . .	32
2.21	THD of the asynchronous switching amplifier . . . . .	33
2.22	Efficiency of the asynchronous switching amplifier versus amplitude . . . . .	33
2.23	Block diagram of the modified balanced asynchronous class D amplifier . . . . .	34
2.24	Integrator circuit . . . . .	35
2.25	Schematic of the opamp . . . . .	36
2.26	Simulated amplitude and phase of the opamp . . . . .	38
2.27	Schematic of the comparator . . . . .	39
2.28	Simulation of the comparator . . . . .	40
2.29	Diagram of the basic voltage reference . . . . .	42
2.30	Schematic of the biasing circuit . . . . .	43
2.31	Diagram of the cascode output stage . . . . .	47
2.32	Schematic of the divider . . . . .	48
2.33	Simulation of DMOS in and outputs, basic version . . . . .	49
2.34	Simulation of DMOS in and outputs, cascode version . . . . .	49
2.35	Simulated output of the basic amplifier @ 200kHz reference signal . . . . .	50
2.36	Simulated output of the cascode amplifier @ 200kHz reference signal . . . . .	50
2.37	Simulated spectrum of the basic amplifier @ 200kHz reference signal . . . . .	51
2.38	Simulated spectrum of the cascode amplifier @ 200kHz reference signal . . . . .	51
2.39	Simulated linearity of both amplifiers . . . . .	53
2.40	Simulated input power of both amplifiers . . . . .	54
2.41	Die photograph of the amplifier processed, basic output stage . . . . .	55
2.42	Die photograph of the amplifier processed, cascode output stage . . . . .	56
2.43	Simulated and measured linearity of the basic amplifier . . . . .	57
2.44	Simulated and measured linearity of the cascode amplifier . . . . .	57
2.45	Measured linearity of both amplifiers . . . . .	58
2.46	Simulated and measured input power of the basic amplifier . . . . .	59
2.47	Simulated and measured input power of the cascode amplifier . . . . .	59
2.48	Measured input power of both amplifiers . . . . .	60
2.49	Full-rate ADSL output spectrum . . . . .	60
2.50	Detail of the MTPR output spectrum . . . . .	61
3.1	Exponential transfer function with small signal parameters . . . . .	66
3.2	Exact and small signal output response . . . . .	67
3.3	Block diagram of non-linearity and approximation . . . . .	68

**LIST OF FIGURES**

3.4	Exact, small and large signal output response . . . . .	72
3.5	Block diagram of a closed loop system . . . . .	75
3.6	Generalized block diagram of a closed loop system . . . . .	76
3.7	HD <sub>3</sub> as function of $v_m$ and $f$ , 6MHz first order loop, fixed $f_0$ . . .	84
3.8	HD <sub>3</sub> as function of $v_m$ and $f$ , 6MHz first order loop, $v_m$ compensated $f_0$ . . . . .	84
3.9	Comparison of calculated and simulated HD <sub>3</sub> , first order loop, 200kHz signal . . . . .	85
3.10	Comparison of calculated and simulated HD <sub>3</sub> , first order loop, 500kHz signal . . . . .	85
3.11	Comparison of calculated and simulated HD <sub>3</sub> , first order loop, 1MHz signal . . . . .	86
3.12	HD <sub>3</sub> as function of $v_m$ and $f$ , 10MHz second order loop, fixed $f_0$ .	88
3.13	HD <sub>3</sub> as function of $v_m$ and $f$ , 10MHz second order loop, $v_m$ compensated $f_0$ . . . . .	89
3.14	Comparison of calculated and simulated HD <sub>3</sub> , 10MHz second order loop, 200kHz signal . . . . .	89
3.15	Comparison of calculated and simulated HD <sub>3</sub> , 10MHz second order loop, 500kHz signal . . . . .	90
3.16	Comparison of calculated and simulated HD <sub>3</sub> , 10MHz second order loop, 1MHz signal . . . . .	90
3.17	HD <sub>3</sub> as function of $v_m$ and $f$ , 30MHz second order loop, fixed $f_0$ .	91
3.18	HD <sub>3</sub> as function of $v_m$ and $f$ , 30MHz second order loop, $v_m$ compensated $f_0$ . . . . .	92
3.19	Comparison of calculated and simulated HD <sub>3</sub> , 30MHz second order loop, 200kHz signal . . . . .	92
3.20	Comparison of calculated and simulated HD <sub>3</sub> , 30MHz second order loop, 500kHz signal . . . . .	93
3.21	Comparison of calculated and simulated HD <sub>3</sub> , 30MHz second order loop, 1MHz signal . . . . .	93
3.22	HD <sub>3</sub> as function of $v_m$ and $f$ , 10MHz third order loop, fixed $f_0$ . .	95
3.23	HD <sub>3</sub> as function of $v_m$ and $f$ , 10MHz third order loop, $v_m$ compensated $f_0$ . . . . .	96
3.24	Comparison of calculated and simulated HD <sub>3</sub> , third order loop, 200kHz signal . . . . .	96
3.25	Comparison of calculated and simulated HD <sub>3</sub> , third order loop, 500kHz signal . . . . .	97
3.26	Comparison of calculated and simulated HD <sub>3</sub> , third order loop, 1MHz signal . . . . .	97
3.27	Comparison of all calculated loops, rms input voltage $v_m = 0.126$	99
3.28	Comparison of all calculated loops, 200kHz input signal . . . . .	99
3.29	Comparison of all calculated loops, 500kHz input signal . . . . .	100
3.30	Comparison of all calculated loops, 1000kHz input signal . . . . .	100

4.1	Basic schematic of a two stage folded cascode opamp . . . . .	109
4.2	Schematic of the two stage folded cascode opamp with output common mode control . . . . .	112
4.3	Simulated Bode diagram of the opamp . . . . .	113
4.4	Realized integrator . . . . .	113
4.5	Bode plot of the 1.6MHz integrator . . . . .	114
4.6	Bode plot of the 3.2MHz integrator . . . . .	114
4.7	Schematic of the rail-to-rail voltage follower . . . . .	116
4.8	Bode diagram of the voltage follower, 1.65V input common mode	117
4.9	Phase margin of the opamp, depending on the common mode input voltage . . . . .	117
4.10	Gain bandwidth product of the opamp, depending on the com- mon mode input voltage . . . . .	118
4.11	Biasing circuit for the folded cascode stage . . . . .	119
4.12	Basic circuit of the comparator . . . . .	120
4.13	Final circuit of the comparator . . . . .	122
4.14	Simulation result of the comparator . . . . .	123
4.15	Schematic of the high voltage output stage . . . . .	124
4.16	Comparison of power dissipation between the VFNDM80 and VFNDM80a DMOS as a function of the time delay, for different widths . . . . .	125
4.17	Output voltage as a function of duty cycle . . . . .	126
4.18	Input power as a function of duty cycle . . . . .	126
4.19	Schematic of the level shifter . . . . .	128
4.20	Schematic of the high to low level shifter . . . . .	129
4.21	Simulation of the level shifter . . . . .	130
4.22	Simulation of the buffers . . . . .	131
4.23	Schematic of the filter-divider . . . . .	131
4.24	DC simulation of the first order system . . . . .	134
4.25	Third order harmonic distortion of the first order system . . . . .	136
4.26	DC simulation of the 10MHz second order system . . . . .	137
4.27	Third order harmonic distortion of the 10MHz second order system	138
4.28	DC simulation of the 30MHz second order system . . . . .	140
4.29	Third order harmonic distortion of the 30MHz second order system	141
4.30	DC simulation of the third order system . . . . .	142
4.31	Third order harmonic distortion of the third order system . . . . .	143
4.32	DC simulation of the second order system with independent loops	144
4.33	Third order harmonic distortion of the second order system with independent loops . . . . .	145
5.1	Die photograph of the amplifiers processed . . . . .	152
5.2	Photograph of the test board . . . . .	153
5.3	DC measurements on the first order system . . . . .	155

**LIST OF FIGURES**

**xiii**

5.4	Third order harmonic distortion of the first order system . . . . .	156
5.5	Noise measurements on the first order system . . . . .	158
5.6	MTPR measurements on the first order system . . . . .	159
5.7	DC measurements on the 10MHz second order system . . . . .	160
5.8	Third order harmonic distortion of the 10MHz second order system	161
5.9	Noise measurement on the 10MHz second order system . . . . .	162
5.10	MTPR measurements on the 10MHz second order system . . . . .	162
5.11	DC measurements on the 30MHz second order system . . . . .	163
5.12	Third order harmonic distortion of the 30MHz second order system	165
5.13	Noise measurement on the 30MHz second order system . . . . .	166
5.14	MTPR measurements on the 30MHz second order system . . . . .	166
5.15	DC measurements on the third order system . . . . .	167
5.16	Third order harmonic distortion of the third order system . . . . .	168
5.17	Noise measurements on the third order system . . . . .	169
5.18	MTPR measurements on the third order system . . . . .	170
5.19	DC measurements on the second order system with independent loops . . . . .	171
5.20	Third order harmonic distortion of the second order system with independent loops . . . . .	172
5.21	Noise measurement on the second order system with indepen- dent loops . . . . .	173
5.22	MTPR measurements on the second order system with indepen- dent loops . . . . .	173
5.23	Schematics for worst case simulations and PDMOS transistor mea- surements . . . . .	175
5.24	Resistance of the PDMOS, spice simulation, typical . . . . .	176
5.25	Resistance of the PDMOS, spice simulation, worst case 1 . . . . .	176
5.26	Resistance of the PDMOS, spice simulation, worst case 2 . . . . .	177
5.27	Resistance of the PDMOS, comparison of spice and TCAD simu- lations . . . . .	177
5.28	Measured resistance of a 80 $\mu$ m PDMOS . . . . .	178
5.29	Measured resistance of a 4818 $\mu$ m PDMOS . . . . .	178
5.30	Temperature of the 4818 $\mu$ m PDMOS package seal . . . . .	179
5.31	Oscillating frequency detail, 25 $\Omega$ load, 30MHz second order loop	180
5.32	Oscillating frequency detail, 50 $\Omega$ load, 30MHz second order loop	181
5.33	DC measurements on the first order system . . . . .	182
5.34	Third order harmonic distortion of the first order system . . . . .	183
5.35	Noise measurement on the first order system . . . . .	184
5.36	MTPR measurements on the first order system . . . . .	184
5.37	DC measurements on the 10MHz second order system . . . . .	186
5.38	Third order harmonic distortion of the 10MHz second order system	187
5.39	Noise measurement on the 10MHz second order system . . . . .	188
5.40	MTPR measurements on the 10MHz second order system . . . . .	188

5.41	DC measurements on the 30MHz second order system . . . . .	189
5.42	Third order harmonic distortion of the 30MHz second order system	190
5.43	Noise measurement on the 30MHz second order system . . . . .	191
5.44	MTPR measurements on the 30MHz second order system . . . . .	191
5.45	DC measurements on the third order system . . . . .	193
5.46	Third order harmonic distortion of the third order system . . . . .	194
5.47	Noise measurement on the third order system . . . . .	195
5.48	MTPR measurements on the third order system . . . . .	195
5.49	DC measurements on the second order system with independent loops . . . . .	196
5.50	Third order harmonic distortion of the second order system with independent loops . . . . .	197
5.51	Noise measurement on the second order system with indepen- dent loops . . . . .	198
5.52	MTPR measurements on the second order system with indepen- dent loops . . . . .	198



## Samenvatting

Tijdens de laatste decennia zijn telecommunicatie in het algemeen en digitale datacommunicatie in het bijzonder een steeds belangrijkere rol gaan spelen in het dagdagelijkse leven. Terwijl de interconnectie van de grote datacenters gerealiseerd kan worden door relatief dure oplossingen zoals optische vezel en satellietverbindingen, omwille van het grote datadebiet dat daar verwerkt wordt, blijft het grote probleem het overbruggen van de laatste kilometers naar de eindgebruiker. Door gebruik te maken van het bestaande telefoon-, kabeltelevisie- of zelfs het elektriciteitsnetwerk kan deze kost echter beperkt worden.

Dit werk zal zich verder concentreren op de overdracht van digitale data over het twisted pair telefoonnetwerk, meer in het bijzonder met behulp van de familie van digital subscriber line (xDSL) technologieën. Waar xDSL gekend is omwille van zijn hoge spectrale efficiëntie en immuniteit voor stoorinvloeden en vervorming, heeft deze het nadeel van een hoge crest factor, gedefinieerd als de verhouding van de piekwaarde tot de kwadratisch gemiddelde waarde van het signaal, en de nood aan sterk lineaire lijnversterkers, waardoor de gemiddelde vermogensefficiëntie beneden de 15% blijft. Dit houdt ook een beperking in van het aantal lijnen dat per wijkcentrale aangestuurd kan worden om te voldoen aan thermische- en vermogensisen.

Een mogelijk alternatief om de efficiëntie op te drijven, is de klasse van niet-lineaire versterkers, aangezien deze idealiter een efficiëntie van 100% hebben. Dit betekent natuurlijk ook dat een zorgvuldig ontwerp nodig is om aan de lineariteitseisen te voldoen.

Het soort versterker dat verder doorheen dit boek gebruikt zal worden, is een asynchrone versie van de klassieke pulswijdte modulator (PWM). In plaats van hetingangssignaal te vergelijken met een zaagtand referentiesignaal op vaste frequentie, wordt een laagdoorlaat gefilterde versie van de blokgolfuitgang gebruikt. Het eindresultaat is dus een oscillator, door het gebruik van positieve terugkoppeling in de lus, met het efficiëntievoordeel van PWM, maar waarbij het in principe mogelijk moet zijn om op lagere schakelfrequenties te werken, wat natuurlijk de schakelverliezen vermindert. Analoog aan de naamgeving bij synchrone  $\Sigma\Delta$  omvormers, die een gelijkaardig blokschema hebben, wordt de "orde" van de versterker bepaald door het aantal invertoren in het voorwaartse signaalpad om systematische identificatie van het blokdiagram te vereenvoudigen.

Het werkingsprincipe van deze asynchrone lijnversterker wordt getest in hoofdstuk 2 door de implementatie van een nulde en een eerste orde versterker in de AMIS  $0.7\mu\text{m}$  I<sup>2</sup>T100 100V technologie, die werkt op een voedingsspanning van 50V.

Het ongebalanceerde nulde orde systeem blijkt op een lagere oscillatiefrequentie te werken dan gesimuleerd door de toevoeging van verschillende meetpaden, met een hogere efficiëntie en distorsie tot gevolg. Voor een 200kHz, 10V referentie uitgangssignaal resulteert dit in een gesimuleerde distorsie van 6.07% en 27.91% efficiëntie en de gemeten waarden 7.49% voor de distorsie met 31% efficiëntie.

Het differentiële eerste orde systeem werkt ook op een lagere oscillatiefrequentie door onvoldoend gemodelleerde component parasitairen en extra parasitairen in de lay-out, wat opnieuw een positieve invloed heeft op de efficiëntie. De gemeten efficiëntie voor een typisch ADSL signaal is ongeveer 13% tegenover een 10% schatting gebaseerd op simulaties. Voor de eerste orde lus is de lineariteit bepaald door de multitone power ratio (MTPR) op te meten, aangezien het uiteindelijk deze waarde is die in de specificaties opgenomen is. Hiertoe wordt een DSL signaal versterkt, waarbij op sommige frequenties geen signaal uitgestuurd wordt. De MTPR is dan gedefinieerd als de verhouding van het vermogen, gemeten op de uitgestuurde frequenties, ten opzichte van het vermogen op deze ongebruikte frequenties. De gemeten waarde voor de MTPR is 40dB, wat hoger is dan de gesimuleerde 35dB, maar nog steeds te laag om te voldoen aan de vereiste voor ADSL lijnversterkers, die, afhankelijk van de bron, tussen 55dB en 65dB bedraagt.

Om het ontwerp van de lusorde en de filters van de asynchrone versterker op een systematischer manier aan te pakken, is een meer wiskundige beschrijving van het systeemgedrag vereist. Alhoewel er legio manieren zijn om het gedrag van lineaire systemen te beschrijven en het gedrag van PWM versterkers vereenvoudigd wordt door het gebruik van een synchrone klok, zijn deze methodes niet onmiddellijk toepasbaar op de asynchrone versterker.

De berekening van de oscillatiefrequentie is gebaseerd op een lineaire benadering van de niet-lineaire component in de lus, door gebruik te maken van de beschrijvendefunctietheorie en het Nyquist criterium voor stabiliteit van systemen in gesloten lus. De schatting van de derde orde harmonische component van zijn kant gebeurt door het verwachte uitgangssignaal gedurende een oscillatieperiode uit te schrijven als een Fourier reeks en die dan uit te breiden tot een volledige signaalperiode.

Dit leidt uiteindelijk tot een stel vergelijkingen die afhankelijk zijn van alle tijdconstanten van het systeem. Deze berekeningen zijn uitgevoerd in hoofdstuk 3, waar de systeemp parameters van een eerste en derde orde lus zijn bepaald, samen met deze van een tweede orde lus met hoge en een met een lagere oscillatiefrequentie.

De simulatieresultaten van de systemen met de berekende parameters komen goed overeen met de berekende voorspellingen en leiden tot het niet zo verrassende besluit dat een hogere lusorde of oscillatiefrequentie beiden een lagere distorsie en hogere MTPR waarde tot gevolg hebben.

De resultaten van deze berekeningen worden verder gebruikt als basis voor de simulaties in de AMIS  $0.35\mu\text{m}$  I<sup>3</sup>T80 80V technologie in hoofdstuk 4. In dit geval is de gekozen voedingsspanning 25V, wat een verdubbeling van de stroom tot gevolg heeft om nog steeds het vereiste vermogen te leveren aan de last.

Wegens de aanwezigheid van tijdvertragingen en parasitaire componenten in het circuit, moeten sommige tijdconstanten aangepast worden om de gewenste oscillatiefrequentie te behouden. Dit heeft natuurlijk tot gevolg dat de overeenkomst tussen de berekeningen van hoofdstuk 3 en de simulaties slechter zal worden naarmate de tijdvertraging toeneemt ten opzichte van de oscillatieperiode. Algemeen kan er besloten worden dat de simulaties behoorlijk goed overeenkomen met de berekeningen, rekening houdend met de ruwe benaderingen die bij de berekeningen gebruikt zijn.

De simulatieresultaten van alle verschillende circuits leiden tot vergelijkbare schattingen voor de efficiëntie rond de 20%, wat duidelijk hoger is dan de voorgaande resultaten en de efficiënties die in de literatuur vermeld staan.

Tot slot wordt in hoofdstuk 5 een overzicht gegeven van alle meetresultaten op de geïntegreerde circuits. Het eerste wat waargenomen kan worden, is de vermindering in oscillatiefrequentie met ongeveer 30% bij alle circuits, wat in principe een negatieve invloed heeft op de lineariteit.

Ten tweede blijkt het vermogensverbruik in ongebruikte toestand merkbaar hoger te zijn dan gesimuleerd, wat tot gevolg heeft dat de efficiëntie gereduceerd wordt tot minder dan 13%. De oorzaak hiervan is van velerlei aard, zoals de invloed van parasitaire in de lay-out, het verschil in weglengte van de differentiële signaalpaden, de werkt temperatuur en de variaties bij de productie. Daarenboven zal de lage waarde van de schakelvertraging van de uitgangstransistoren ook de aanvaardbare tolerantie verder verminderen, aangezien parasitaire tijdsvertragingen dan een relatief belangrijke invloed hebben op het schakeltijdstip en kortsluitstromen in de uitgangstrap mogelijk zijn.

De gemeten waarde voor de MTPR is beperkt tot 20 à 30dB, wat duidelijk minder is dan de gesimuleerde waarden. Het sterk verminderde bereik van de uitgangsspanning, ongeveer 9V in plaats van de gesimuleerde minimale waarde van 12.5V, vormt een belangrijke indicatie met betrekking tot de oorzaak van dit probleem. Uiteindelijk blijkt de zelfopwarming van de uitgangstransistoren, ten minste gedeeltelijk, verantwoordelijk te zijn voor dit verschil, omdat een gedeelte van de terminatieweerstand voor het filter in de uitgangstrap geïntegreerd is in de transistoren om op silicium oppervlakte te kunnen besparen. Bijkomende oorzaken voor de lagere lineariteit kunnen de niet-lineariteit van de geïntegreerde

passieve componenten en de opamps zijn, wat niet verder geverifieerd kon worden, aangezien deze signalen niet geconnecteerd zijn met een meetpad.

Verdere simulaties op de circuits, met toevoeging van bijkomende weerstand in serie met de uitgangstransistoren, vertonen een gelijkaardig gedrag als de metingen en wijzen op een toename van de derde orde harmonische met ongeveer 20dB. Bijkomende metingen, met verhoogde lastweerstand om de relatieve invloed van de impedantie van de uitgangstransistoren te beperken, leiden reeds tot een toename van de MTPR van ongeveer 10dB, wat de invloed van zelfopwarming op de performantie van de versterker bevestigt.

## Summary

During the last decades, telecommunication in general and digital data communication in particular played an increasingly prominent role in everyday life. While the interconnection of large data centres, based on their data flow, can be obtained by rather expensive solutions such as optical fibre and satellite communication the main problem remains bridging "the last mile" to the end user. However, the use of pre-existing infrastructure, such as the telephone and cable TV network or even the power grid, can alleviate this cost.

This work will further focus on the transmission of digital data over the twisted pair telephone network, more specifically on the digital subscriber line (xDSL) technology family. While xDSL is known to be highly spectral efficient and immune to distortion, it has the disadvantage of a high crest factor, defined as the peak to root mean square ratio of the signal, and to require highly linear line drivers, resulting in power efficiencies well below 15%. This limits the number of lines that can be served at the central office, due to thermal and power requirements.

A possible alternative to increase the efficiency would be to use non-linear amplifiers, based on their ideal efficiency of 100%. As a consequence, special care must be taken in order to obtain the linearity required.

The amplifier class implemented in this work is an asynchronous version of the classical pulse width modulated (PWM) amplifier. Instead of comparing the input signal with a sawtooth reference signal at fixed frequency, a low pass filtered version of the square wave output is used. The final result basically is an oscillator, due to positive feedback in the loop, having the efficiency advantage of PWM circuits, but supposedly at lower switching frequencies, thus reducing switching losses. In analogy with the nomenclature used with synchronous  $\Sigma\Delta$  converters, which also have a similar block diagram, the "order" of the amplifier is determined by the number of integrators in the forward signal path, to simplify systematic identification of the block diagram.

The basic concept of the asynchronous line driver is verified in chapter 2 by the implementation of a zeroth and first order amplifier in the AMIS  $0.7\mu\text{m}$   $I^2T100$  100V technology, operating at a 50V supply voltage.

The single ended zeroth order system was verified to operate at a slightly re-

duced oscillating frequency as compared to the simulations due to the insertion of several measurement pads, resulting in both higher efficiency and distortion. For the 200kHz, 10V reference output signal, this led to a simulated distortion of 6.07% at 27.91% efficiency and a measured 7.49% distortion at 31% efficiency.

The balanced first order system also operates at a lower oscillating frequency due to insufficient component parasitics modelling and additional layout parasitics, which again has a positive influence on the amplifier efficiency. Using a typical ADSL signal, the measured efficiency is about 13% instead of the 10% estimate resulting from the simulations. For the first order loop, the multitone power ratio (MTPR) is used as the measure for linearity, since the DSL specifications are based on this figure. For this test, a DSL like signal, composing of all but some DMT tones, is amplified by the line driver and the MTPR is determined as the difference between the nominal tone power and the power measured at the missing tone frequency. The measured 40dB MTPR also is slightly higher than the simulated 35dB, but this is still too low to fulfill the ADSL requirements, ranging from 55dB to 65dB depending on the source.

To allow for a more systematical design of loop order and the filters of the asynchronous amplifier, a mathematical description of the system behaviour is required. While there is a plethora of methods for describing linear circuits and the description of PWM amplifiers is simplified by the mere presence of a synchronous clock, these can not readily be applied on the asynchronous amplifier.

The calculation of the oscillating frequency is based on a linear approximation of the non-linear component in the loop, using the describing function theory and the Nyquist stability criterion for closed loop systems. The third order harmonic content on the other hand is approximated by writing the expected output signal during one oscillation period as its Fourier series, which can then be extended to the full input signal period.

This finally leads to a set of equations, depending on all time constants of the system. These calculations are performed in chapter 3, where the system parameters of a first and third order loop are determined, in addition to two second order loops, one with a low and one with a high oscillating frequency.

The results of simulations using the parameters as calculated correspond well with the calculated predictions and lead to the not so surprising conclusion that an increase in loop order or oscillating frequency both lead to a lower distortion and increased MTPR figure.

The results from these calculations are then used as a basis for the simulations in chapter 4, using the AMIS 0.35 $\mu$ m I<sup>3</sup>T80 80V technology. In this case, the supply voltage chosen is 25V, leading to a doubling of the current to deliver the required power to the load.

Due to the presence of time delays and parasitics in the circuit, some time constants needed adjustment in order to maintain the envisaged oscillating fre-

quency. As a consequence, the correspondence between the calculations from chapter 3 and the simulations will get worse with increasing time delay compared to the oscillating period. In general, it can be concluded that the system simulations still correspond rather well with the calculations, given the rough approximations made.

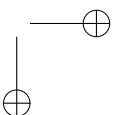
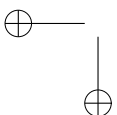
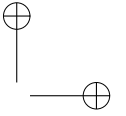
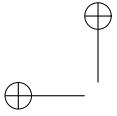
Simulations on all different circuits also lead to comparable efficiency figures of about 20%, which is significantly higher than the previous results and the efficiencies reported in the literature.

Chapter 5 finally gives an overview of all measurement results on the circuits implemented. A first observation is the reduction of the oscillating frequency by 30% for all circuits, which is expected to negatively impact the linearity.

Secondly, the idle power consumption of the amplifier is significantly higher than simulated, effectively limiting the estimated efficiency to under 13%. This is caused by a combination of several factors, such as layout parasitics, difference in length of the signal paths, operating temperature and process corners. In addition, the low value of the turn-on delay of the output transistors further reduces the acceptable tolerance, since additional time delays caused by parasitics will gain influence, possibly causing feed-through currents at the output stage.

The measured MTPR is limited to 20-30dB, well below the simulated values. An important indication as to which component might be the culprit, is the largely reduced output voltage swing, being about 9V instead of minimum 12.5V as simulated. As it turns out, self heating of the output transistors is, at least partially, to blame for this discrepancy, which is caused by the inclusion of part of the filter matching resistance in the output stage to reduce silicon area usage. Additional causes of distortion equally comprise the non-linearity of integrated passives and the opamp circuits, which could not be verified as those signals remain internal to the circuit.

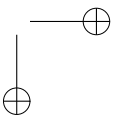
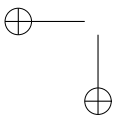
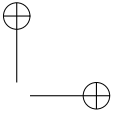
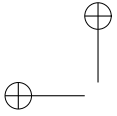
Simulations on the circuits processed, including additional resistance in series with the output transistors, already exhibit similar behaviour as the measurements, suggesting a deterioration of the third order harmonic content by 20dB. Additional measurements with increased output impedance, to reduce the relative importance of the output transistor impedance on the system, lead to an increase of MTPR by about 10dB, which confirms the influence of self heating on the amplifier performance.

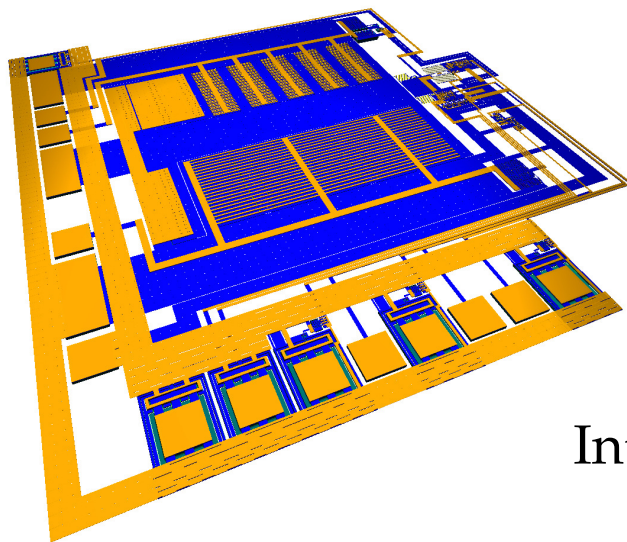




## List of Abbreviations

<b>Notation</b>	<b>Meaning</b>
ADC	Analogue to Digital Converter
ADSL	Asymmetric Digital Subscriber Line
CF	Crest Factor
CMOS	Complementary MOS
CO	Central Office
DAC	Digital to Analogue Converter
dBc	Decibels relative to the carrier
DMOS	Drain extended MOS
DMT	Discrete Multitone
DSP	Digital Signal Processor
GBW	Gain Bandwidth Product
HD <sub>3</sub>	Third order Harmonic Distortion
IFFT	Inverse Fast Fourier Transform
ISDN	Integrated Services Digital Network
LPF	Low Pass Filter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTPR	Multitone Power Ratio
NDMOS	N-type DMOS
OFDM	Orthogonal Frequency Division Multiplexing
PDMOS	P-type DMOS
PM	Phase Margin
POTS	Plain Old Telephone Service
PSU	Power Supply Unit
PWM	Pulse Width Modulation
QAM	Quadrature Amplitude Modulation
rms	Root Mean Square
TCAD	Technology Computer-Aided Design
THD	Total Harmonic Distortion
VDSL	Very high speed Digital Subscriber Line





# 1

## Introduction

### 1.1 Wire line communication

#### 1.1.1 Rise of the network

Since the invention of the electrical telegraph in the first half of the 19th century, private investors and government corporations start interconnecting these simple telecommunication devices. At first, wire length is rather limited, but at the beginning of the 20th century this network already interconnected major cities worldwide [1].

In parallel to these large scale interconnections, by the second half of the 19th century, the invention of the telephone caused a growing number of end users to show interest in the possibilities offered by this new technology. As with the telegraph, the first versions were standalone point to point connections using a single wire. Telegraph contractors however quickly realized they could extend the principle of the telegraph exchanges to this telephone, effectively creating a multi subscriber network. Since the bottleneck now shifted to the exchange operator, efforts were underway, first to simplify operation, but eventually to automate this process. Initially this also meant an increase in the number of wires needed — up to seven in the case of the Strowger automatic exchange [2]. Finally, only two wires were retained, this mainly for reasons of signal quality, leading to the classical twisted pair network.

### 1.1.2 Extending the applications

As technology evolved in the 20th century, new applications emerged for the now full-grown telephone network. The increasing performance of computers, and the development of the ARPANET research network yielded expertise that was soon to be adopted in the analogue telephone networks [1]. At first, the end-to-end networks were digitized, increasing capacity and data quality. Later on, modems were used to allow for communication between computers, and the integrated services digital network (ISDN, originally Integriertes Sprach- und Daten-netz) enabled a fully digitized path between end users. A further improvement of this digital communication is the xDSL family, of which asymmetric digital subscriber line (ADSL) and very high speed digital subscriber line (VDSL) are the best known members. A key difference between the classical modem and xDSL is the fact that xDSL uses its own frequency band, allowing for simultaneous use of telephone and xDSL communication.

A simplified diagram of the combination of plain old telephone service (POTS) and xDSL between end user and central office (CO) is given in Fig. 1.1.

### 1.1.3 Some properties of xDSL

The main advantage of xDSL over alternative forms of networking, such as optical fibre, is the use of the existing telephone wires, so the investments required usually are limited. However, the bandwidth of the wire pair will limit the bit rate and wire length. While this could be solved by increasing the power transmitted, cross-talk at both the transmitter and receiver end will further limit the quality of the signal, effectively putting an upper limit of about 5km on the wire length [3][4].

To reliably transmit the signal, xDSL uses a form of orthogonal frequency division multiplexing (OFDM) called discrete multitone (DMT), as depicted in Fig. 1.2. The digital data first is mapped onto the constellation of quadrature amplitude modulation (QAM), resulting in amplitude and phase information for each carrier frequency. This information then is transformed into analogue form for transmission by the use of an inverse fast Fourier transform (IFFT) and a digital to analogue converter (DAC) before being amplified by the line driver [5].

The result of this all is an encoding scheme, that can be implemented efficiently using a mainstream digital signal processor (DSP). The analogue output signal has a high spectral efficiency and low interference sensitivity. This explains the popularity of this modulation and its use in wireless networking, digital radio, digital TV etc.

However, this digital efficiency is not entirely translated into the analogue domain. Although the signal has a clean frequency domain representation as shown in Fig. 1.3a, the time domain can exhibit a high crest factor (CF), defined as the

1.1 Wire line communication

3

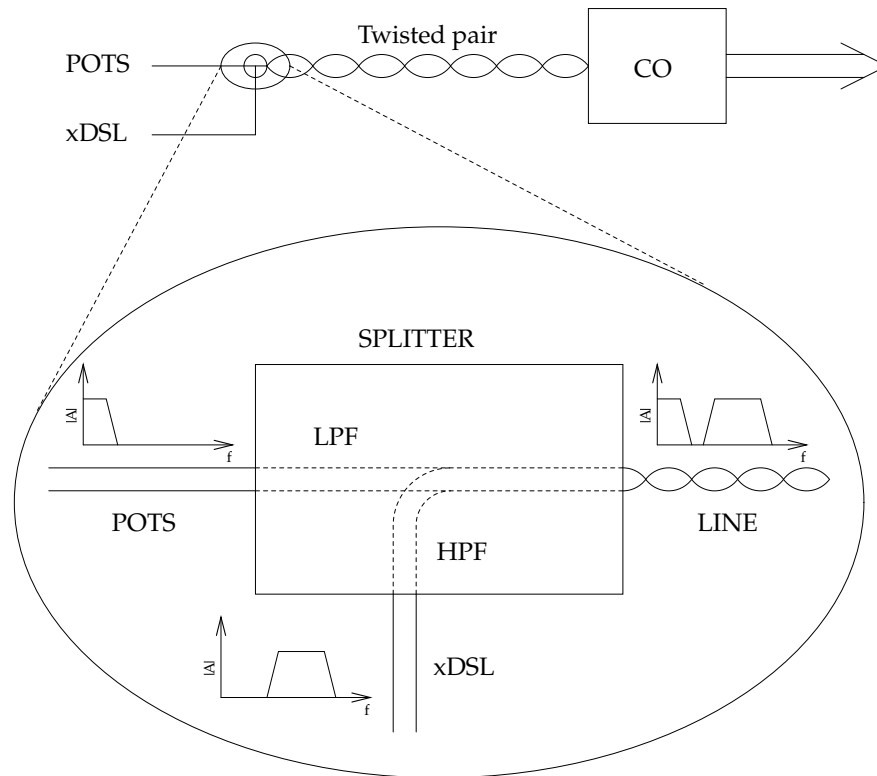


Figure 1.1: Simplified diagram of telephone interconnection

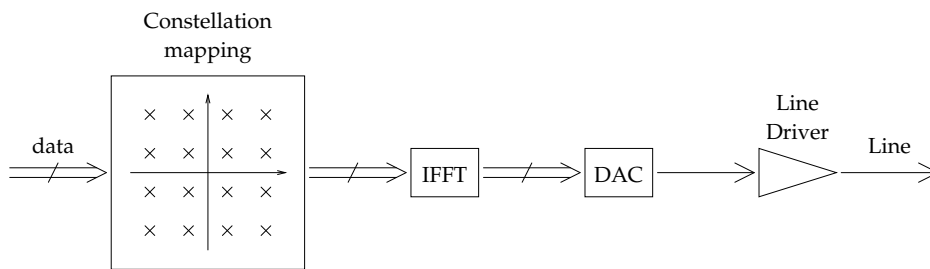


Figure 1.2: Principle of DMT encoding

peak to root mean square (rms) ratio of the signal. As a result, the analogue amplifier must be highly linear and might suffer low power efficiency [5][6]. Also note that all possible time domain representations will lead to Fig. 1.3a, regardless of CF, so Fig. 1.3c and Fig. 1.3d are only two possible results of the IFFT.

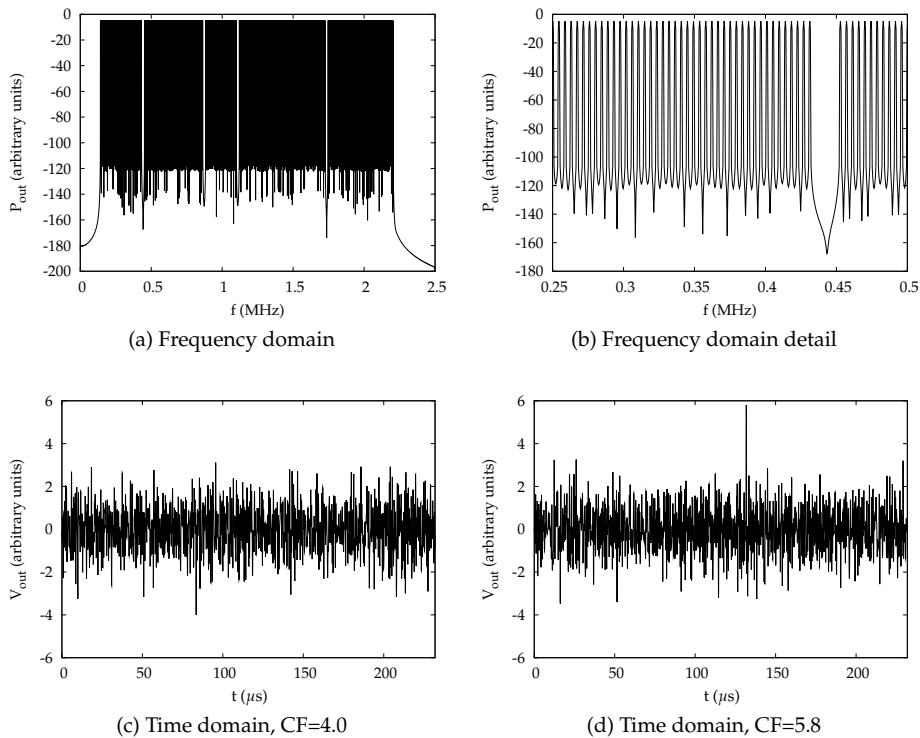


Figure 1.3: Frequency and time domain representation of a DMT encoded signal

## 1.2 Context and goal of this work

As already mentioned in Section 1.1.3, DMT suffers a high CF. To fulfill the high linearity demands, commercially available line drivers to date use some form of class AB amplifiers. However, using a CF of 5.8, the maximum achievable efficiency can be calculated as follows:

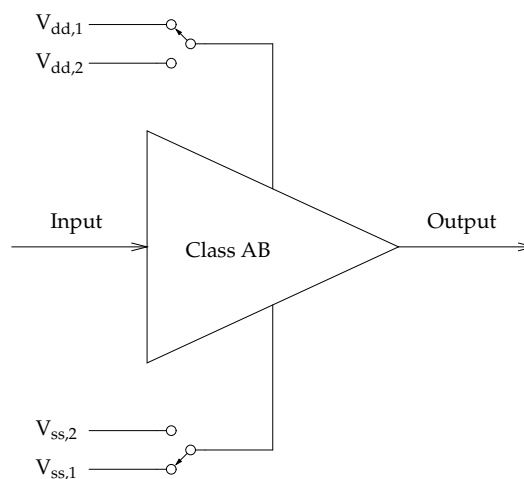
$$\eta = \frac{\pi}{4CF} = 13.5\%$$

## 1.2 Context and goal of this work

5

The result is a tremendous amount of power being dissipated at the CO, which limits the number of lines that can be served due to thermal and power requirements. As such, it might be interesting to investigate the applicability of less linear amplifiers. Although their frequency range is much lower, audio amplifiers form an excellent source of inspiration, because they have an even worse CF [7].

A first way to increase the efficiency, is to use a class G amplifier, as shown in Fig. 1.4 [8]. In this case, multiple supply voltages are fed into the amplifier, of which those yielding the highest efficiency are selected. An alternative is given in Fig. 1.5 [9], where the supply voltage is the output of a high efficiency switching amplifier, generating a voltage slightly higher than needed to ensure proper operation. In both cases this results in a higher average efficiency for the linear amplifiers.



**Figure 1.4:** Simplified diagram of a class G amplifier using multiple supply voltages

A different approach to the problem is to use highly efficient class D or pulse width modulation (PWM) amplifiers, as illustrated in Fig. 1.6. In its most simple form, the input signal is compared with a synchronous reference signal, often being a sawtooth. Depending on this comparison, the output will either be in the high or the low state. Since the output switches are ideally lossless, the efficiency of this amplifier is 100%. On the other hand, due to the hard non-linearity, the frequency of the synchronous reference signal must be sufficiently higher than the maximum input frequency to increase linearity.

Classical pulse width modulators (PWM) require a triangular or sawtooth reference input at a frequency of 10 to 100 times the highest signal frequency, which becomes impractical at xDSL frequencies. To lower the switching frequency while

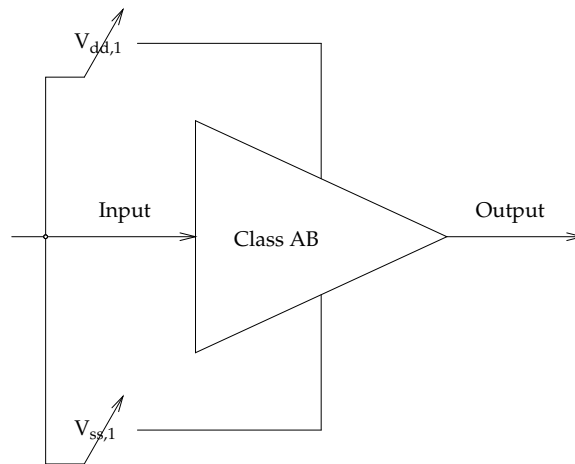


Figure 1.5: Simplified diagram of a class G amplifier using a variable supply voltage

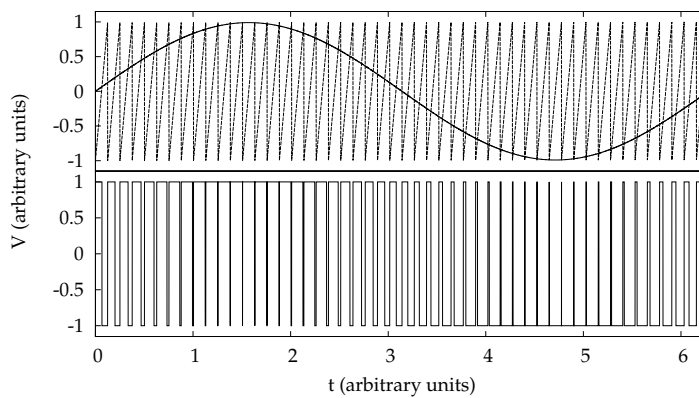
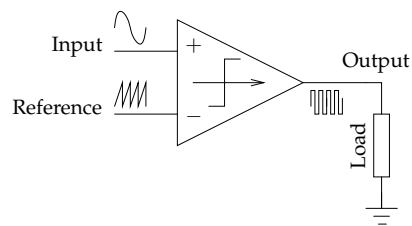


Figure 1.6: Block diagram and corresponding waveforms of a basic PWM amplifier



### 1.3 Outline

7

maintaining an acceptable level of distortion, a suitable feedback scheme has to be adopted, an example of which is given in Fig. 1.7 [10] for audio amplifiers. In this case, the main output power is delivered by a switching amplifier and switching is controlled by the error current delivered by a parallel class AB amplifier. When this current exceeds its threshold in any of both directions, the state of the class D output stage is changed accordingly. As a result, this amplifier is self-oscillating, at a frequency determined by the current threshold, with the output linearized by the class AB amplifier.

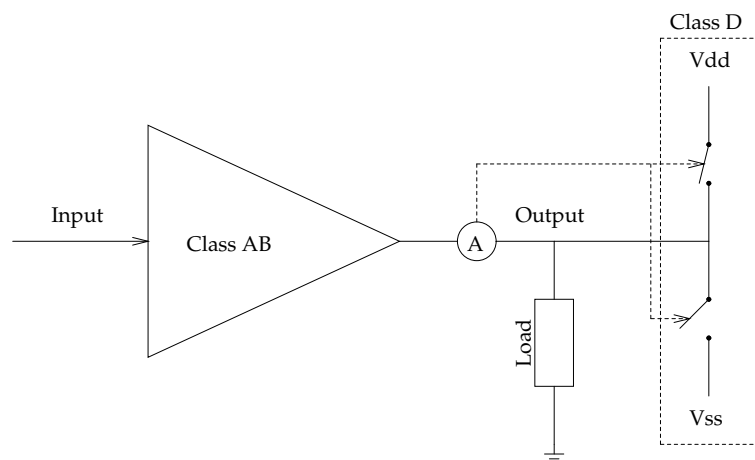


Figure 1.7: Example of an asynchronous mixed class AB and D amplifier

An alternative solution is to drop the external, synchronized reference input and use a filtered version of the output. By choosing an appropriate filter transfer function, the broad spectral content of the square wave output will be reduced, resulting in a more triangular signal that can be used as reference as depicted in Fig. 1.8 [11]. Basically, this amplifier is an oscillator, due to positive feedback, thus having the efficiency advantage of PWM circuits, but it should also be possible to achieve a comparable linearity at lower switching frequencies. On the other hand, the non-linearity and the asynchronous nature will complicate the mathematical description and performance prediction of the system.

### 1.3 Outline

This work is further organized as follows. In chapter 2, the concept from Fig. 1.8 is further developed and simulated, finally resulting in the demonstration of the feasibility of the basic idea and the presentation of measurement results on a silicon integration of the circuits studied.

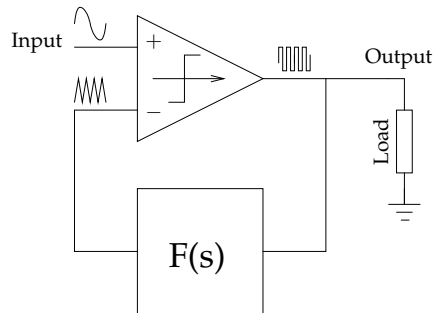


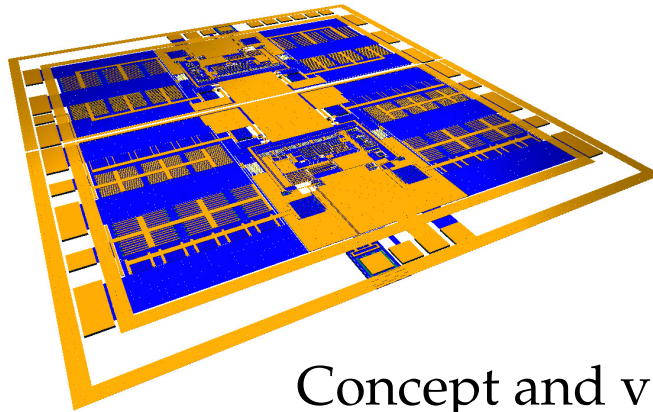
Figure 1.8: Block diagram of an asynchronous class D amplifier

Chapter 3 will then present a mathematical framework to predict the most important system parameters such as oscillating frequency and third order harmonic distortion. These calculations will result in values for the parameters of the building blocks, which will further be simulated on the transistor level in chapter 4. The measurements on the silicon implementations of these circuits and the corresponding remarks and conclusions are given in chapter 5. Finally, chapter 6 will give an overview of the most important conclusions of this work and possibilities for future research.

## References

- [1] Wikipedia. (2008, Jul.) Telegraphy. [Online]. Available: <http://en.wikipedia.org/wiki/Telegraph>
- [2] Wikipedia. (2008, Jul.) Telephone. [Online]. Available: <http://en.wikipedia.org/wiki/Telephone>
- [3] K. P. Ho, "Broadcast digital subscriber lines using discrete multitone for broadband access," *Microprocessors and Microsystems*, vol. 22, no. 10, pp. 605–610, May 1999.
- [4] F. Sjöberg, M. Isaksson, R. Nilsson, P. Ödling, S. K. Wilson, and R. O. Börjesson, "Zipper: a duplex method for VDSL based on DMT," *IEEE Trans. Commun.*, vol. 47, no. 8, pp. 1245–1252, Aug. 1999.
- [5] D. J. G. Mestdagh, P. M. P. Spruyt, and B. Biran, "Effect of amplitude clipping in DMT-ADSL transceivers," *Electronics Letters*, vol. 29, no. 15, pp. 1354–1355, July 22 1993.
- [6] Wikipedia. (2008, Jul.) Orthogonal frequency-division multiplexing. [Online]. Available: [http://en.wikipedia.org/wiki/Discrete\\_multitone\\_modulation](http://en.wikipedia.org/wiki/Discrete_multitone_modulation)
- [7] Wikipedia. (2009, Jan.) Crest factor. [Online]. Available: [http://en.wikipedia.org/wiki/Crest\\_factor](http://en.wikipedia.org/wiki/Crest_factor)
- [8] F. H. Raab, "Average efficiency of class-G power amplifiers," *IEEE Trans. Consum. Electron.*, vol. CE-32, no. 2, pp. 145–150, May 1986.
- [9] H. Nakagaki, N. Amada, and S. Inoue, "A high-efficiency audio power amplifier," *Journal of the Audio Engineering Society*, vol. 31, no. 6, pp. 430–436, Jun. 1983.
- [10] R. A. R. van der Zee and E. A. J. M. van Tuijl, "A power efficient audio amplifier combining switching and linear techniques," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 985–991, Jul. 1999.

- [11] J. Vanderkooy, "Comments on 'design parameters important for the optimization of very-high-fidelity PWM (class D) audio amplifiers'," *Journal of the Audio Engineering Society*, vol. 33, no. 10, pp. 809–811, Oct. 1985.



# 2

## Concept and verification

This chapter describes the preliminary verification of the functioning of the asynchronous amplifier. The first section will give a brief overview of design choices to be made, in the second section a brief overview of the technology used is given, while the third and fourth section discuss simulations and measurement results of two silicon implementations.

### 2.1 Preliminary considerations

A slightly more generalized block diagram of the asynchronous line driver, as proposed in section 1.2, is shown in Fig. 2.1. The first choice to be made, is the transfer functions  $F(s)$  and  $G(s)$ . For  $G(s)$ , this choice is quite obvious, since the fed back signal should be a low pass filtered version of the square wave output, so a passive low pass filter (LPF) is sufficient. For  $F(s)$  however, there is a broad range of suitable candidates. Due to the resemblance between this circuit and  $\Sigma\Delta$  analogue to digital converters (ADC), two functions stand out: a simple LPF and an integrator. As such, also the naming convention from  $\Sigma\Delta$  ADC's can be used, describing the converter by the number of integrators in the forward path, which results in a zeroth or first order system for the circuit in Fig. 2.1.

A second design choice is the supply voltage required to deliver the output power specified. As explained in section 1.1.3, for DMT encoded signals, this requires knowledge of the nominal power corresponding to the rms value of the signal

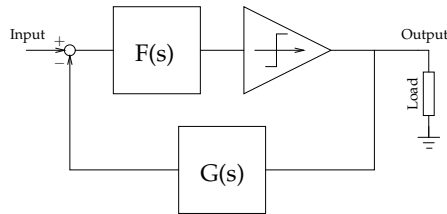


Figure 2.1: Block diagram of an asynchronous class D amplifier

and the maximal CF. These values were found in [1] as 20dBm power with CF 6.8. Furthermore, the output power is delivered to the  $100\Omega$  line impedance by means of a transformer. The winding ratio should be between 1:1 and 1:2 so as to not reduce the amplitude of the received signal excessively, since this is detected at resistors in series with the line driver output stage. For this first version, a winding ratio of 1:1 is chosen, thus the maximum output amplitude can be calculated as

$$V_{\text{out}} = \sqrt{P_{\text{out}} R_{\text{CF}}} = 21.5\text{V} \quad (2.1)$$

As such, the peak-to-peak voltage at the output is 43V.

For reasons of signal integrity, the output impedance of the amplifier should be matched, resulting in a doubling of the supply voltage required, but by opting for a bridge configuration, this can be halved again. To provide for some headroom, the supply voltage chosen is 50V. This also means that dedicated high voltage devices must be used. The technology chosen is the AMI Semiconductor I<sup>2</sup>T100 0.7 $\mu\text{m}$  technology, offering such high voltage extensions up to 100V to a mainstream low voltage CMOS technology.

Additionally, the oscillating frequency must be chosen, taking into account the envisaged signal bandwidth. The circuits described in this chapter should be capable of handling signals in the range of 138kHz to 1.108MHz, corresponding to ADSL [1]. As such, designing for a switching frequency of approximately 10MHz seems a reasonable trade-off between output linearity and switching losses.

Finally, it should also be noted that the output delivers a lot of excess power to the load, due to the high spectral content of a square wave. To clean this up, a LPF is placed between the matching impedance and the load, allowing only the frequency band of interest to pass through and suppressing the square wave output. Of the two possible topologies, namely the  $\Pi$  and T networks as shown in Fig. 2.2, only the T network can be used, since the  $\Pi$  variant allows for high frequency current to be dissipated in the matching impedance, effectively decreasing efficiency.

A more detailed diagram, showing the output configuration and the voltage supply, is given in Fig. 2.3.

2.1 Preliminary considerations

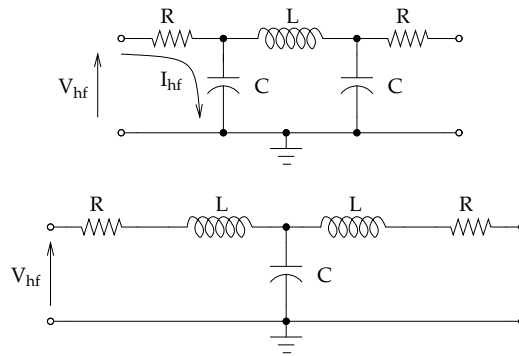


Figure 2.2:  $\Pi$  versus T output filter topology

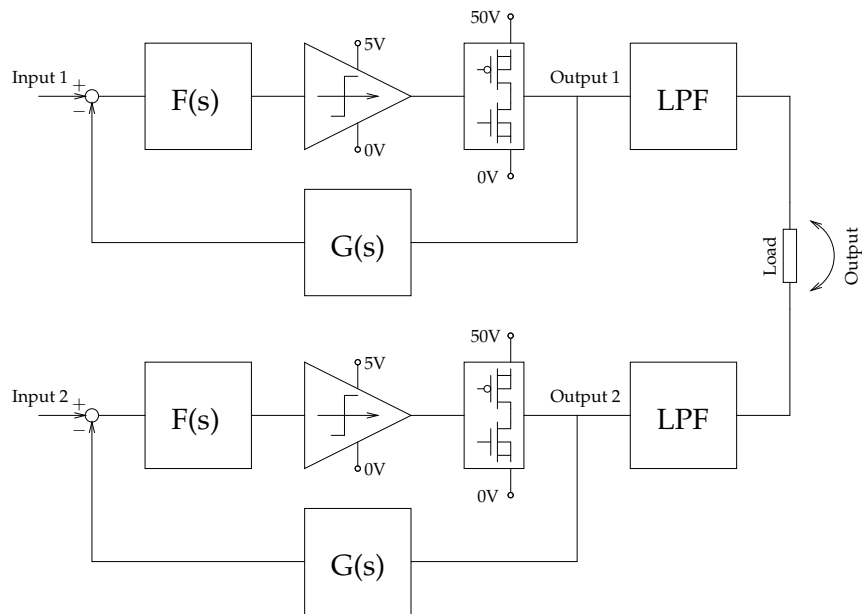


Figure 2.3: More detailed diagram of the asynchronous class D amplifier

Table 2.1: Key characteristics of I<sup>2</sup>T100 DMOS devices [2]

Device	Type	Floating bulk	Breakdown	R <sub>DS</sub> @  V <sub>DS</sub>   = 0.2V	Width per mm <sup>2</sup>
NDMOS	N	No	100V	70kΩ*μm	48309μm
FNDMOS	N	100V	100V	33.6kΩ*μm	67568μm
PDMOS	P	100V	-100V	176kΩ*μm	41322μm
FPDMOS	P	60V	-75V	55kΩ*μm	99010μm

This chapter is further organized as follows. Section 2.2 gives a brief overview of the AMIS I<sup>2</sup>T100 technology. In section 2.3, simulations on the sub blocks and the full circuit of the zeroth order system are discussed and compared with measurements on a silicon implementation of the circuit. Section 2.4 then describes simulation and measurement results of the first order system.

## 2.2 Technology overview

The AMI Semiconductor I<sup>2</sup>T100 technology is a high voltage extension to the standard 0.7μm CMOS technology, enabling special devices and structures to operate at voltages up to 100V, while the low voltage CMOS devices remain the same as in the 5V technology. Further on, this rather complex technology also provides high voltage DMOS devices, several types of bipolar transistors, in addition to the resistors and capacitors.

### DMOS transistors

As the amplifier has a switching output, only the DMOS devices are to be considered, since they show far superior switching behaviour compared with bipolar transistors. Opposed to the low voltage CMOS, the DMOS devices are not symmetrical. They also have a different gate oxide thickness, allowing for gate-source voltages of up to 12V. The targeted supply voltage of 50V puts a lower limit on the breakdown voltage, so only four devices are withheld, of which the key characteristics are summarized in table 2.1. From this table it is clear that the FNDMOS and FPDMOS are the best choice, since they both have a lower on resistance *and* a higher area efficiency.

### MOS transistors

Table 2.2 gives an overview of the available MOS transistors. Since the processing starts from a P-doped substrate, the bulk of the PMOS transistors is floating up



## 2.2 Technology overview

15

**Table 2.2:** Key characteristics of I<sup>2</sup>T100 MOS devices [2]

Device	Type	Floating	Breakdown	V <sub>T0</sub>	I <sub>DS</sub>
NMOS	N	No	5.5V	0.74V	358μA/μm
FNMOS	N	100V	5.5V	0.74V	358μA/μm
PMOS	P	5V	-5.5V	-0.95V	-176μA/μm
FPMOS	P	100V	-5.5V	-1.1V	-160μA/μm

**Table 2.3:** Key characteristics of I<sup>2</sup>T100 capacitors [2]

Device	Breakdown	Value
MOS capacitor	5.5V	2fF/μm <sup>2</sup>
Analogue capacitor	12V	0.750fF/μm <sup>2</sup>
High voltage transistor	12V	0.812fF/μm <sup>2</sup>
Poly-poly capacitor	30V	0.345fF/μm <sup>2</sup>
Metal-poly-metal capacitor	100V	0.091fF/μm <sup>2</sup>

to 5V. For referencing at higher voltages, a special floating PMOS is provided, however with different characteristics than the low voltage version. This also implies that the bulk of the standard NMOS is always at the same potential as the substrate, so even low voltage circuits need a special floating device if this is not practical. This FN MOS has the same characteristics as the regular NMOS, at the expense of silicon area.

### Capacitors

Several capacitors are available in I<sup>2</sup>T100, built by overlapping poly, metal or diffusion layers. The typical values are given in table 2.3, with specified deviations of 10 to 15%. Additionally, capacitors built only with metal or polysilicon layers will be less voltage and temperature dependent and are capable of withstanding positive and negative voltages on either plate. Capacitors using a diffusion layer as a plate also have leakage currents and lower breakdown voltages, but have a higher area efficiency.

### Resistors

The technology used offers a broad range of resistors as well, but only the polysilicon resistors are considered. Diffused resistors typically have too high or too low a sheet resistance, depending on the concentration of the doping, and mostly show an excessive temperature dependency. Metal resistors on the other hand have typical values of tens of milliohms per square and are impractical to implement resistors of a reasonable value. The resistors available for use are shown in

Table 2.4: Key characteristics of I<sup>2</sup>T100 resistors [2]

Device	Breakdown	Value
Low ohmic poly	100V	27Ω/□
Medium ohmic poly	100V	210Ω/□
High ohmic poly	100V	2000Ω/□

table 2.4 and all have a 20 to 25% specified tolerance. The low ohmic resistor also has a negative temperature coefficient, in contrast to the other two, so, theoretically, this can be used to compensate for temperature dependency of the resistors in the circuit.

## 2.3 Zeroth order

The most simple case is the zeroth order amplifier, where both  $F(s)$  and  $G(s)$  from Fig. 2.1 are low pass filters. In the presented circuit, only  $G(s)$  is implemented, while  $F(s)$  is replaced by a short. This design can be divided in three parts, namely the LPF to create the switching reference out of the output, the comparator deciding when to change state and the high voltage output stage delivering the power to the load.

### 2.3.1 Schematics and simulations

#### Output stage

The basic schematic of the output stage is given in Fig. 2.4. As the inductive load does not allow discontinuities in the current, additional diodes have been placed in parallel to the DMOS transistors to facilitate the flow of reverse currents through the asymmetric transistors. The sizing of the transistors is chosen so as to minimize the voltage drop at the output stage, as illustrated in Fig. 2.5. This leads to an initial value of 60 parallel NDMOS transistors with a width of  $300\mu\text{m}$  each and 60 parallel PDMOS transistors with a width of  $500\mu\text{m}$ . The diodes have an active area of  $242\mu\text{m}^2$ .

However there is a slight complication. The PDMOS gate must stay within 12V of the 50V supply, so a level shifter must be included. The gate area of both DMOS transistors also introduces a substantial capacitive load, therefore sufficient buffering must be provided to obtain a 10MHz switching frequency. Several power efficient level shifters have been proposed [3], but none of these solutions can be used due to high latency.

As such, the most simple topology was preferred, consisting of a DMOS to withstand the elevated voltages and a properly sized diode connected PMOS to mirror

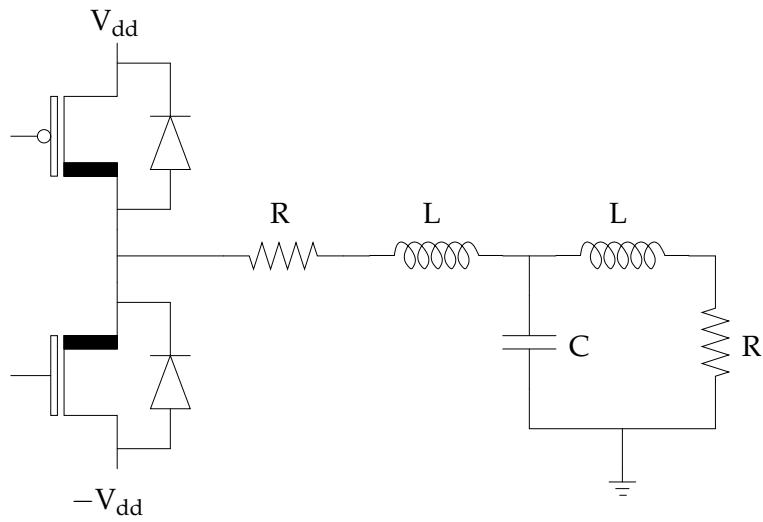


Figure 2.4: Schematic of the high voltage output stage

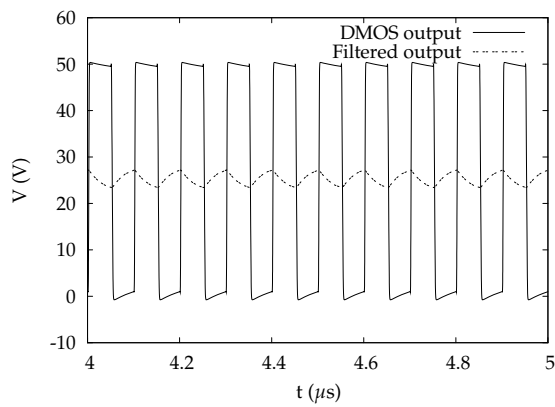


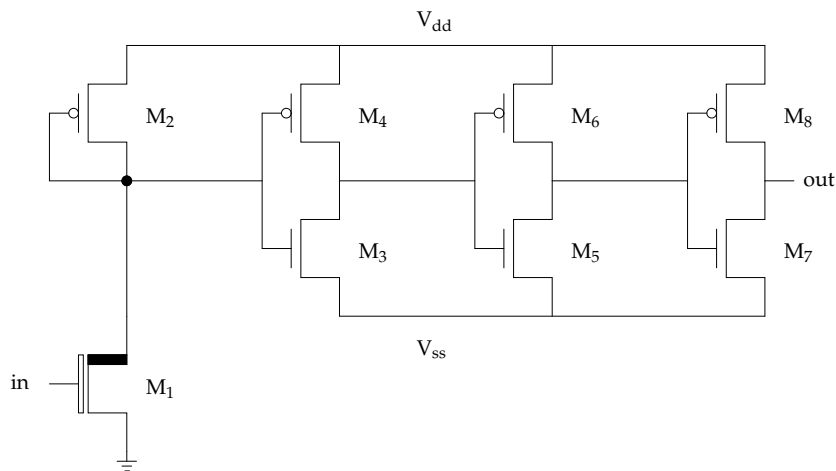
Figure 2.5: Simulation of the high voltage output stage

**Table 2.5:** Transistor dimensions of level shifter and buffer

Device	Width	Length
M <sub>1</sub>	21μm	4μm
M <sub>2</sub>	7μm	1μm
M <sub>3</sub>	70μm	0.7μm
M <sub>4</sub>	189μm	0.7μm
M <sub>5</sub>	150μm	0.7μm
M <sub>6</sub>	405μm	0.7μm
M <sub>7</sub>	300μm	0.7μm
M <sub>8</sub>	810μm	0.7μm

the input voltage, as depicted in Fig. 2.6. The buffer is powered by an additional supply voltage of 45V, also providing the driving strength required at the PDMOS gate for fast state transitions. Table 2.5 summarizes the dimensions of all transistors, while Fig. 2.7 shows the simulation results for the level shifter with buffer stage. The corresponding delay times are approximately 2ns for a rising edge and 6ns for the falling edge.

The buffer driving the NDMOS is straightforward and is identical to transistors M<sub>3</sub> to M<sub>8</sub> from Fig. 2.6 and table 2.5, the only difference being it is operated between ground and 5V.



**Figure 2.6:** Schematic of the level shifter with buffer

An additional advantage of buffering the DMOS gate signal is illustrated in Fig.

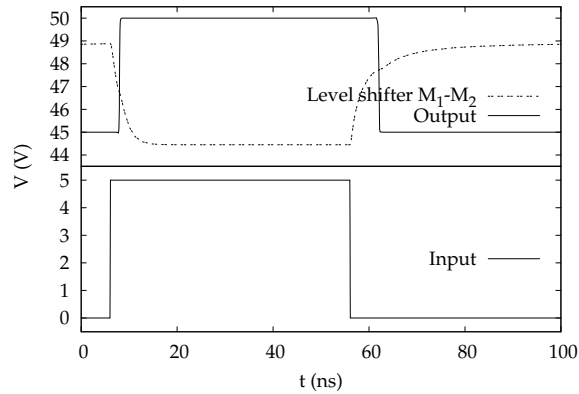


Figure 2.7: Simulation of the level shifter with buffer

2.8. The maximum  $dV/dt$  capability of a DMOS in the off state is derived in [4]:

$$\left[ \frac{dV_{DS}}{dt} \right]_{max} = \frac{V_T}{R_G C_{GD}} \quad (2.2)$$

where  $V_{DS}$  is the drain-source voltage,  $V_T$  the threshold voltage,  $R_G$  the gate resistance and  $C_{GD}$  the gate-drain capacitance. If  $dV/dt$  exceeds this maximum value, the resulting gate-source voltage will become larger than the threshold voltage, causing device turn-on and large feed-through currents. Since the choice of the devices and their width is determined by other constraints, the only parameter available to allow a higher slope at the switching output is the gate resistance  $R_G$ . Insertion of sufficiently wide buffers thus increases  $dV/dt$  by lowering  $R_G$ . A practical value for the maximum  $dV/dt$  capability is approximately 10V/ns.

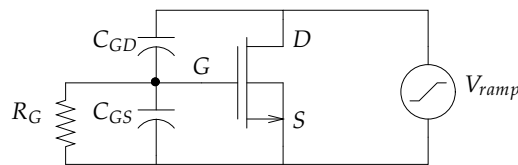


Figure 2.8: Illustration of turn-on in DMOS transistors

The next step is to look at the currents at the output stage. Since the NDMOS and PDMOS do not change state instantaneously, there will be a small amount of time where one DMOS already is partly on, while the complementary DMOS is not yet switched off completely. This causes a short circuit between power supply and ground resulting in excessive power dissipation. The solution is to delay switching on the DMOS without affecting the switch off, which can simply be done by

using the circuit from Fig. 2.9. This turn-on delay, however, should remain limited, since it adversely affects the linearity performance of the amplifier. Table 2.6 summarizes the optimized transistor dimensions.

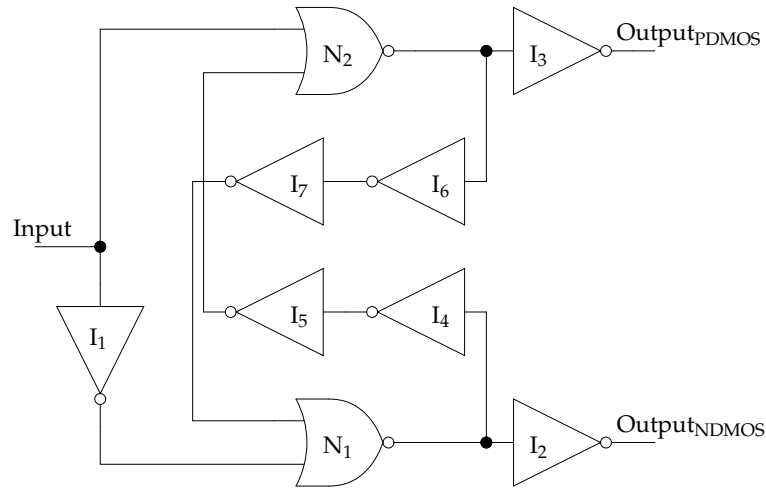


Figure 2.9: Schematic of the delay circuit

### Comparator

The very heart of the zeroth order amplifier is the comparator. Since the input signal is connected directly to the comparator, a rail-to-rail input stage is chosen, based on the circuit proposed in [5]. A simplified schematic is shown in Fig. 2.10 and can be divided in three major parts, a rail-to-rail input stage, a current summation stage and an output buffer.

**Input stage** Strictly speaking, only  $M_1$  and  $M_2$  from Fig. 2.10 are required to achieve rail-to-rail operation. However, as the common mode input voltage approaches a power supply rail, the corresponding transistor pair is cut off, halving the transconductance and the available output current. The result is a transconductor with varying gain, bandwidth and slew rate over the input common mode range, where the circuit used largely compensates these drawbacks.

For low common mode input voltages, none of the NMOS transistors  $M_1$ ,  $M_3$  and  $M_5$  are active, so a current  $I$  flows through the PMOS pairs  $M_2$ ,  $M_4$  and  $M_6$ . As a result, 2 PMOS transistors contribute to the input transconductance, with a total current of  $2I$ . A high common mode input voltage leads to the same result, now using the NMOS stages instead.



**Table 2.6:** Transistor dimensions of the delay circuit

Device	Width	Length
$N_{1,2,N}$	$1\mu\text{m}$	$0.7\mu\text{m}$
$N_{1,2,P}$	$2.7\mu\text{m}$	$0.7\mu\text{m}$
$I_{1,N}$	$1\mu\text{m}$	$0.7\mu\text{m}$
$I_{1,P}$	$3\mu\text{m}$	$0.7\mu\text{m}$
$I_{2,N}$	$15\mu\text{m}$	$0.7\mu\text{m}$
$I_{2,P}$	$45\mu\text{m}$	$0.7\mu\text{m}$
$I_{3,N}$	$2\mu\text{m}$	$0.7\mu\text{m}$
$I_{3,P}$	$6\mu\text{m}$	$0.7\mu\text{m}$
$I_{4,5,N}$	$1\mu\text{m}$	$12\mu\text{m}$
$I_{4,5,P}$	$3\mu\text{m}$	$12\mu\text{m}$
$I_{6,7,N}$	$1\mu\text{m}$	$7\mu\text{m}$
$I_{6,7,P}$	$3\mu\text{m}$	$7\mu\text{m}$

When the common mode voltage is such that both NMOS and PMOS transistors are saturated, no current can flow through  $M_5$  and  $M_6$ , so the pairs  $M_1$  to  $M_4$  each conduct a total current  $I$  of which only the tail currents of  $M_1$  and  $M_2$  contribute to the transconductance. Again, a total current  $2I$  is available and 2 input pairs are used.

As a result, if the transconductance of the NMOS and PMOS is closely matched, the input stage should behave identical, regardless of common mode input. For the circuit simulated, the current  $I$  is chosen to be  $150\mu\text{A}$ , leading to the values in table 2.7.

**Current summation** The resulting signal now must be calculated from the tail currents of the input stage by a current summation circuit. Basically, any current mirroring circuit could do, but in general, cascode mirrors are preferred due to better symmetry and higher output impedance. The folded cascode stage is well suited for operation with close to rail input signals, as it keeps the drain voltage of the active input transistors at approximately a saturation voltage from the supply rail, leaving enough headroom to stay saturated. Also the output can vary up to two saturation voltages from both supply voltages, allowing a near rail-to-rail output swing.

The main drawback of this folded cascode compared to the telescopic cascode is the power consumption. Proper functioning of the amplifier requires each current source of the cascode — transistors  $M_9$  and  $M_{10}$  in Fig. 2.10 — to source or sink the total current at the input stage. For Fig. 2.10 this means an additional  $4I$  drawn from the supply. Placing the current mirror on the PMOS side could reduce this bias current depending on the most likely input common mode voltage. However, for this application this would not mean a more efficient design



Table 2.7: Transistor dimensions of the comparator

Device	Width	Length
M <sub>1,3,5</sub>	1.0 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>2,4,6</sub>	2.7 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>7,8</sub>	10 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>9,10</sub>	26.9 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>11</sub>	10 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>12</sub>	26.9 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>13</sub>	1 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>14</sub>	2.7 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>15</sub>	1 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>16</sub>	2.7 $\mu\text{m}$	0.7 $\mu\text{m}$

and come at the cost of speed, so a NMOS mirror was chosen.

**Output stage** Basically, the output of the previous stage can be coupled directly to a minimal size inverter. However, this should not be done, since the combination of current steering and the capacitive load formed by the inverter gates implies the possibility to pull M<sub>7</sub> to M<sub>10</sub> out of saturation, leading to an increased comparator delay.

Therefore, a feedback current comparator, formed by M<sub>11</sub> to M<sub>14</sub>, is used to limit the output swing. Due to the negative feedback, the voltage at the output of the inverter formed by M<sub>13</sub> and M<sub>14</sub> can not deviate from the equilibrium more than the threshold of an NMOS in the positive sense, or that of a PMOS in the negative sense. As such, this provides large enough a margin to keep the transistors of the first two stages saturated. Although the input swing of the inverter M<sub>13</sub> – M<sub>14</sub> is limited, the output swing already is large enough to require only 1 additional inverter M<sub>15</sub> – M<sub>16</sub>, to acquire a fully digital compliant output.

**Simulation** The values of all transistors are summarized in table 2.7. Figure 2.11 shows the simulation results for a common mode voltage of 2.5V and extreme values of 0.5V and 4.5V. In all three cases, the positive input was kept constant, whereas a 10MHz sinewave was put at the negative input with 100mV and 500mV amplitude, simulating the filtered output of the switching amplifier. The corresponding delay times for both logic transitions are given in table 2.8.

This circuit clearly functions in the entire common mode range of interest. As could be expected, the delay time depends on both common mode and signal amplitude, leading to more advantageous and homogeneous delay times at higher amplitude levels.

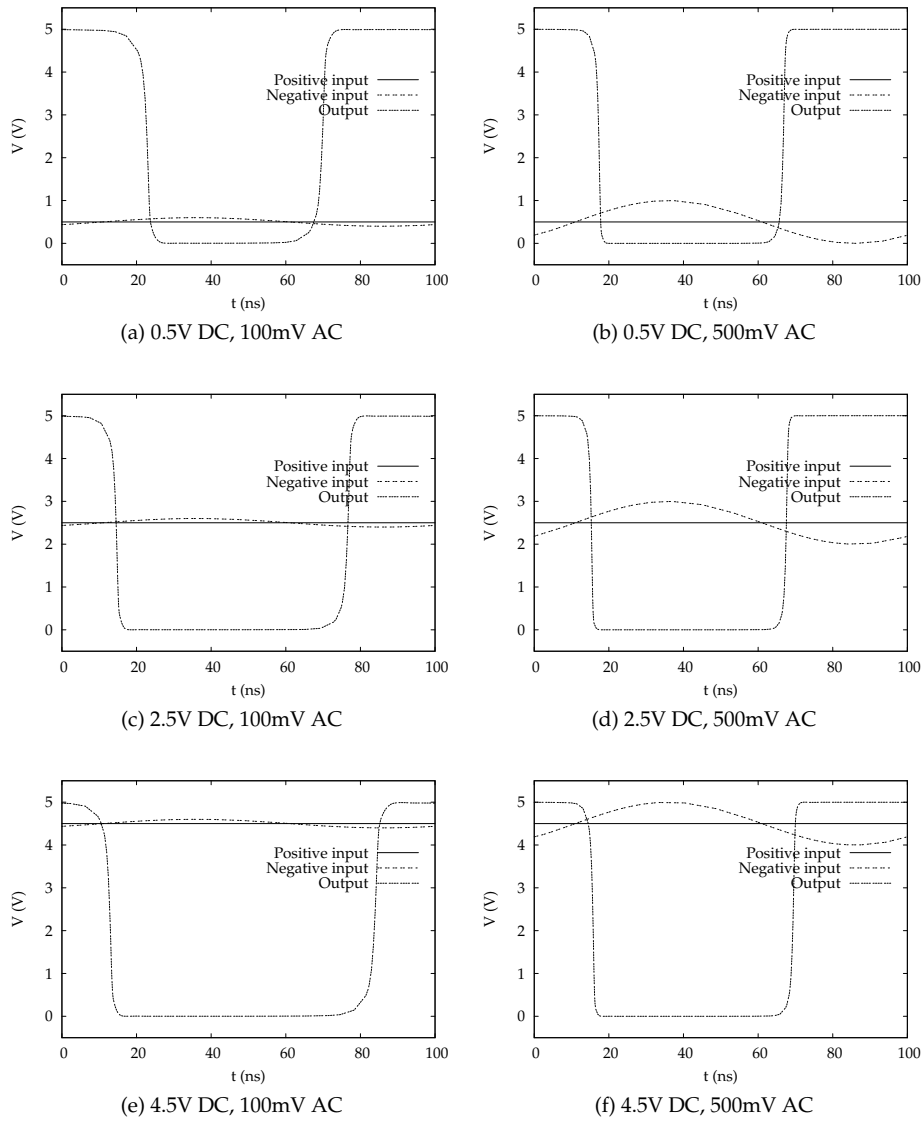


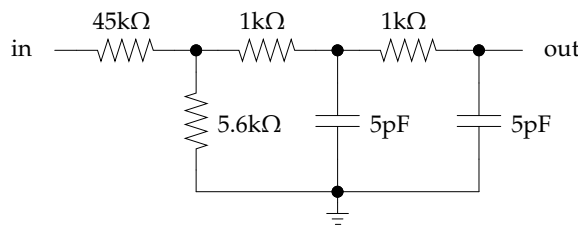
Figure 2.11: Simulation of the comparator

**Table 2.8:** Delay times of the comparator

Common mode	0.5V	2.5V	4.5V
Low – high, 100mV	8.8ns	15.7ns	22.9ns
High – low, 100mV	11.8ns	3.5ns	1.8ns
Low – high, 500mV	5.8ns	6.6ns	8.4ns
High – low, 500mV	6.3ns	4.3ns	4.7ns

**Full simulation**

The only block still missing to complete the schematic is the loop filter. Since the filter output is connected directly to the input of the comparator, it should range between 0V and 5V to avoid breakdown. Therefore, the circuit from Fig. 2.12 is chosen, with values tuned to have a simulated 11.9MHz cut-off frequency including model parasitics. This filter, together with the time delays of the other blocks, will set the maximum oscillating frequency of the amplifier at 11MHz.



**Figure 2.12:** Schematic of the loop filter

To speed up the simulations and corresponding optimizations, a single ended amplifier is used in most simulations. To emulate a balanced setup, the output of the filter in Fig. 2.2 is referenced to half the supply voltage and the output is measured over half the load resistance required. At the final stage, full balanced simulations are performed to compare both results, especially with regard to reduction of harmonic content.

The output voltage of a single amplifier is shown in Fig. 2.13 together with the ideal output waveform having a reference frequency of 200kHz and an amplitude of 10V. The output spectrum is given in Fig. 2.14. These calculations yield a DC voltage of 24.95V, being half the supply voltage and a fundamental amplitude of 9.481V at the output. The suppression of the second and third harmonic are respectively -29dBc and -31dBc, with a total harmonic distortion (THD) of 6.07%. The average switching frequency for this sinewave is found to be 10.7MHz.

The same simulation has also been performed for the balanced amplifier, now resulting in a doubled fundamental amplitude. The waveform and output spec-

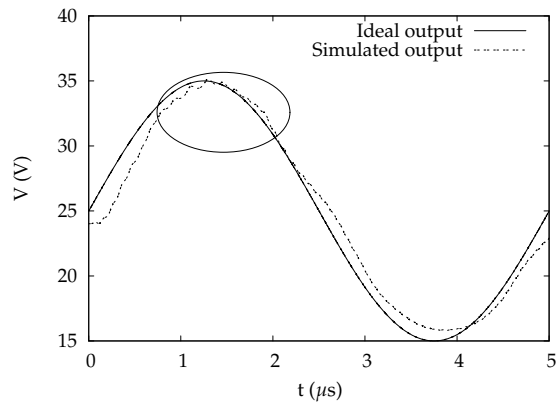


Figure 2.13: Simulated output of single ended amplifier @ 200kHz reference signal

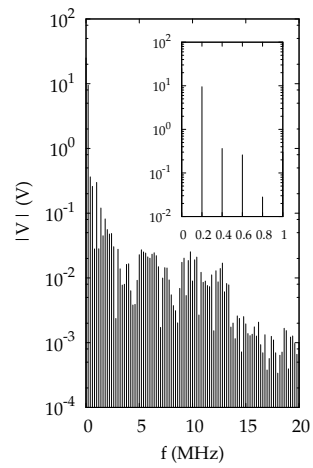


Figure 2.14: Simulated spectrum of single ended amplifier @ 200kHz reference signal

2.3 Zeroth order

trum are given in Fig. 2.15 and 2.16, showing a significant reduction of even harmonics, as can be expected for a balanced amplifier. The resulting THD is 4.14%, the second harmonic is at -60dBc and the third harmonic at -32dBc. These simulation results are summarized in table 2.9.

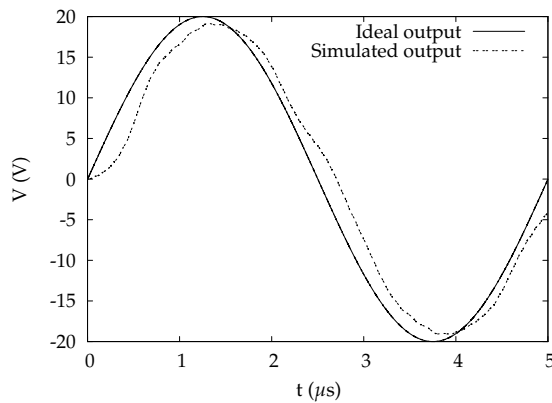


Figure 2.15: Simulated output of balanced amplifier @ 200kHz reference signal

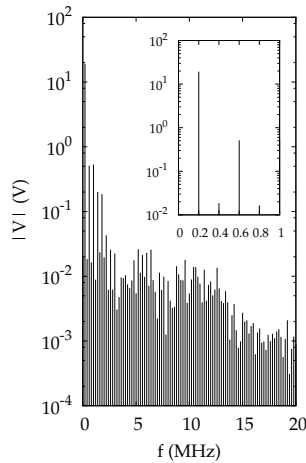


Figure 2.16: Simulated spectrum of balanced amplifier @ 200kHz reference signal

The achieved output power for the single ended amplifier is 0.90W with an input power of 3.22W. The NDMOS switch dissipates 0.61W, the PDMOS switch 0.53W and the matching resistor 1.18W. The matching resistor is dissipating more than the output resistor since its current still contains more high frequency compo-

**Table 2.9:** Summary of simulation results

	Single ended	Balanced
Fundamental	9.481V	18.96V
Second harmonic	-29dBc	-60dBc
Third harmonic	-31dBc	-32dBc
THD	6.07%	4.14%

nents. This results in an amplifier efficiency of 27.91%, which is over 55% of the maximum achievable output efficiency for an amplifier with a matched load, with a dissipation of 35.4% in the DMOS switches. These data are presented in table 2.10.

**Table 2.10:** Power dissipation of the single ended amplifier

	P(W)
$P_{in}$	3.22
$P_{out}$	0.90
$P_{NDMOS}$	0.61
$P_{PDMOS}$	0.53
$P_{matching\ resistor}$	1.18

Since the level shifter makes a large contribution to the delay time in the path to the PDMOS, the switching behaviour of the PDMOS transistor will be the main cause for distortion. For high output amplitudes, where the amplifier is delivering a net current into the inductive load, this results in ringing. The slow turning off of the PDMOS causes a large positive overshoot, whereas the delayed turning on yields a large negative undershoot since the diode in parallel with the NDMOS will be the only current path available. For low output amplitudes, this is not so pronounced as the diode parallel to the PDMOS can compensate for the fast turning off of the NDMOS. This effect is annotated in Fig. 2.13.

The possibility for DMOS turn-on, as explained before, can now be verified as well. The approximate values for the amplifier simulated are given in table 2.11 and both yield about 15V/ns. Since the full system simulations yield slopes of 10V/ns and less, as illustrated in Fig. 2.17, there is no turn-on expected. Although small spikes are visible on both gate signals when one of the transistors changes state, none of them is large enough to have an adversary effect.

Another point of concern is the accuracy of the available models and the simulator settings. While the modelling of low voltage components in mainstream

Table 2.11: Maximum  $dV/dt$  capability of the DMOS switches used

	NDMOS	PDMOS
$V_T$	2.4V	-1.12V
$R_G$	10 $\Omega$	10 $\Omega$
$C_{GD}$	15pF	8pF
$\frac{dV_{DS}}{dt}$	16V/ns	14V/ns

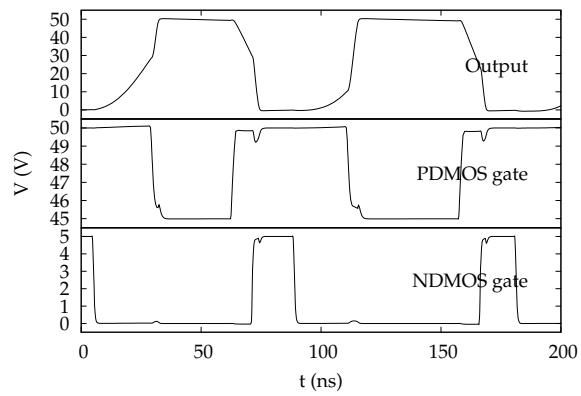


Figure 2.17: Simulated gate and output signals of the output stage

technologies is quite accurate, this is not really the case for high voltage DMOS transistors. Because of their complex, non-symmetric structure, these components are modelled by a circuit of active and passive components. However this has serious implications on the fitting of model parameters, causing the models of several active subcomponents to be limited to a level 2 or even a level 1 Spice model.

Furthermore these models are only valid for a limited transistor width. Since the DMOS transistors must be able to deliver enough power to the load, they have to be very wide. Therefore they have to be divided in several parallel transistors, as will be the case on the layout too, significantly increasing the simulation time. One also has to adjust the tolerance settings of the simulator to let the simulation converge, although this might cause some numerical oscillations, especially on signal currents, decreasing the accuracy.

### 2.3.2 Layout and measurement results

The simulated amplifier is processed in the AMIS I<sup>2</sup>T100 high voltage 0.7 $\mu$ m CMOS technology. Since the supply voltage used is 50V and slopes of 10V/ns are expected, special care must be taken while placing and routing the components, to avoid triggering of parasitic transistors and latch-up. Also EMC-issues must be taken into account to avoid excessive coupling of digitized signals into the analogue building blocks.

A die micrograph of the processed amplifier is shown in Fig. 2.18, where all different parts are annotated. The total area consumption of the chip is 3.3mm<sup>2</sup>. However, the circuit processed is not completely identical to the simulated one, since multiple measurement pads were inserted, increasing parasitic capacitances. Because of this, the circuit was expected to operate at a lower switching frequency, causing both a higher THD and efficiency. The measured output signal at a reference frequency of 200kHz and an output amplitude of 10V is given in Fig. 2.19. The THD was 7.49% with an efficiency of 31% at an average switching frequency of 8MHz, as opposed to the simulation results of Fig. 2.13, where the THD equaled 6.07%, with an efficiency of 27.91% at an average switching frequency of 10.7MHz.

In Fig. 2.20, both simulated and measured efficiencies are plotted versus frequency, while Fig. 2.21 shows the THD. The measured efficiency and distortion are both higher than the simulated ones, as expected. These figures also illustrate the impact of several design choices, for example there is a clear correspondence between efficiency and THD, as already mentioned before. Besides this, the THD is also influenced by the cut-off frequency of the output filter. Since this frequency is 2MHz, it will decrease the THD for higher frequencies by reducing harmonic content, while maintaining high efficiency.



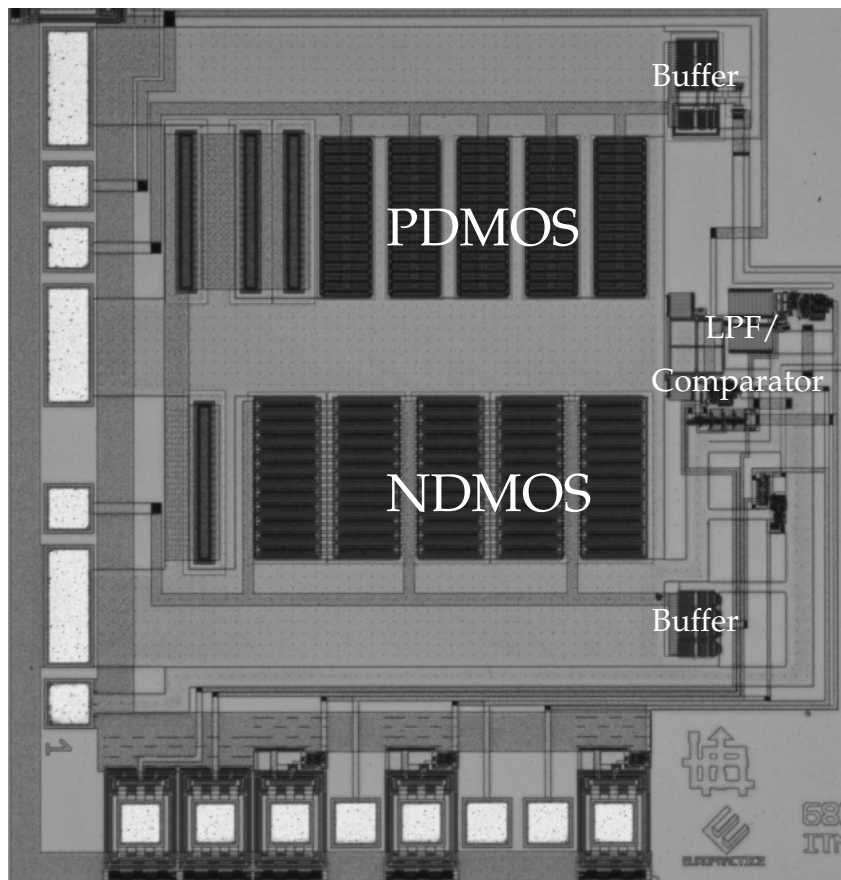


Figure 2.18: Die photograph of the amplifier processed

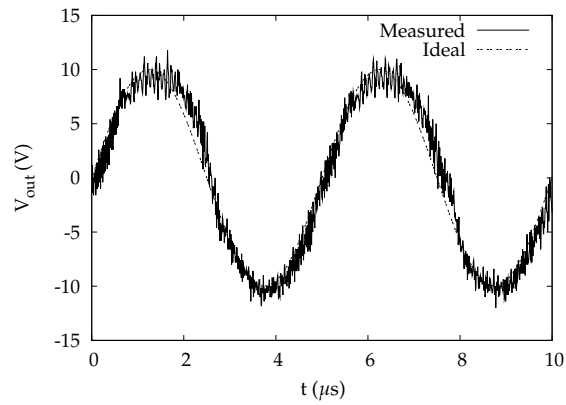


Figure 2.19: Measured and ideal output of the asynchronous switching amplifier

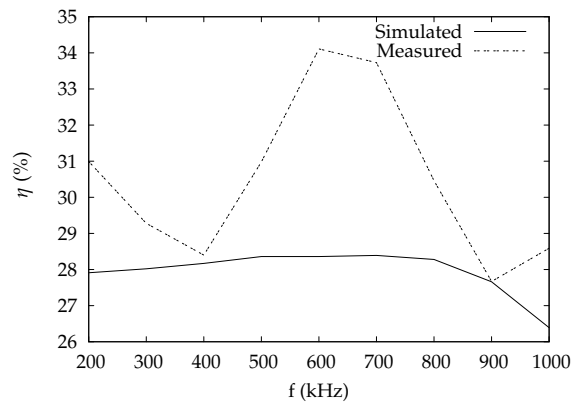


Figure 2.20: Efficiency of the asynchronous switching amplifier

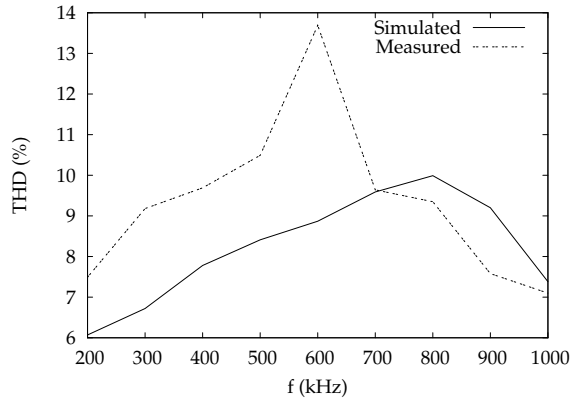


Figure 2.21: THD of the asynchronous switching amplifier

Fig. 2.22 shows the simulated and measured efficiency of the amplifier as a function of output amplitude, together with the ideal efficiency of a class AB amplifier. From this, it becomes clear that the amplifier almost has the efficiency of an ideal linear amplifier for high output amplitudes, whereas the dissipation of the switches reduces the efficiency at low output amplitudes. Therefore, the next design of the output stage will focus on a reduction of the idle power dissipation.

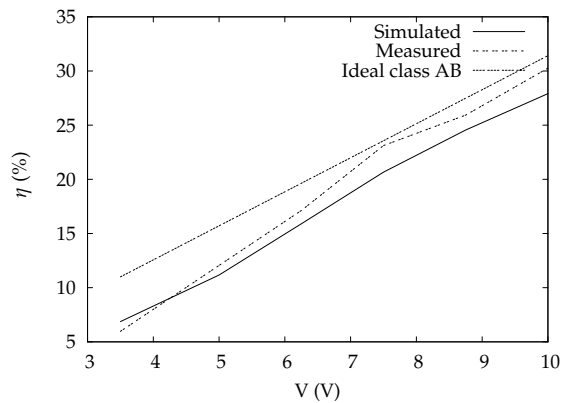


Figure 2.22: Efficiency of the asynchronous switching amplifier versus amplitude

## 2.4 First order

The next test case is the first order amplifier, where  $F(s)$  is an integrator and  $G(s)$  again is a low pass filter, using the same notations as in Fig. 2.1. The presence of the integrator in the circuit requires some additional building blocks, such as an operational amplifier and a biasing circuit, but the need for a rail-to-rail comparator vanishes. Also, the amplifier output now is made fully balanced by using two output stages, steered in counterphase, as shown in Fig. 2.23. The resulting subcircuits that will be discussed, are the integrator, the comparator, the biasing circuit and finally the new output stage.

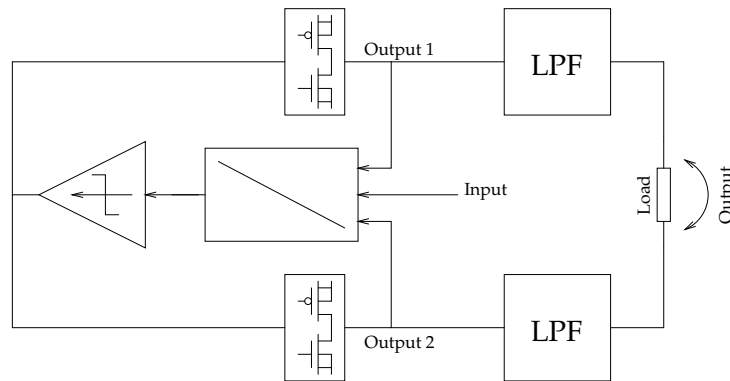


Figure 2.23: Block diagram of the modified balanced asynchronous class D amplifier

### 2.4.1 Schematics and simulations

#### Opamp and integrator

The integrator as used in Fig. 2.23 has three inputs, thus before designing the opamp itself, a suitable circuit must be selected. Using the nullator hypothesis, it is easily derived that the circuit from Fig. 2.24 has the following transfer function:

$$V_{out} = \frac{(V_{i1} - V_{i2}) - V_{in}}{sRC} \quad (2.3)$$

where  $V_{in}$  is the reference input,  $V_{out}$  the opamp output and  $V_{i1}$  and  $V_{i2}$  the in phase respectively counter phase filtered output signals of the line driver. This also implies an additional halving of the output signal by the loop filter, to map the balanced output range to the single ended input.

Since the fed back signals  $V_{i1}$  and  $V_{i2}$  will span a limited voltage range and are

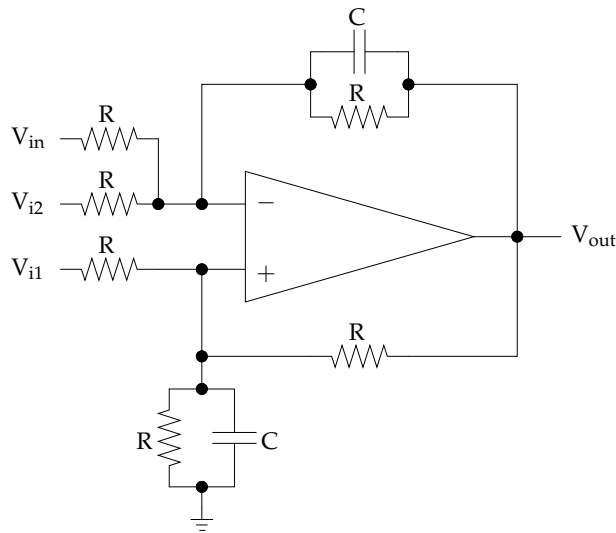


Figure 2.24: Integrator circuit

connected to the opamp input nodes by resistors, the opamp input stage needs not be rail-to-rail.

Figure 2.25 shows the schematic of the opamp, which consists of three parts, namely the input differential pair, a folded cascode and a class AB output stage. The opamp is designed for a 60MHz gain bandwidth product (GBW) and a capacitive load of 1pF, immediately leading to the first set of equations:

$$f_1 = \frac{g_{m1}}{2\pi C_L} \quad (2.4)$$

$$f_0 = \frac{1}{2}f_1 = \frac{g_{m3}}{2\pi C_{M1}} \quad (2.5)$$

where  $f_1$  is the first non-dominant pole,  $f_0$  the zero-dB bandwidth,  $C_L$  the load capacitance,  $C_{M1}$  the total Miller capacitance determining the dominant pole,  $g_{m3}$  the transconductance of each input transistor  $M_{31}$  and  $M_{32}$  and  $g_{m1}$  the total transconductance of the output stage transistors  $M_{11}$  and  $M_{12}$ . The GBW frequency  $f_0$  must be chosen half the value of the non-dominant pole  $f_1$  to ascertain a  $60^\circ$  phase margin.

Substituting the specified values in equation (2.4) immediately evaluates to

$$g_{m1} = 754\mu S \quad (2.6)$$

and

$$g_{m11} = g_{m12} = \frac{g_{m1}}{2} = 377\mu S \quad (2.7)$$



## 2.4 First order

37

Proposing a value  $I_B = 50\mu A$  and using these equations, the remaining parameters are calculated:

$$g_{m3} = 250\mu S \quad (2.15)$$

$$g_{m21} = 500\mu S \quad (2.16)$$

$$g_{m23} = 333.33\mu S \quad (2.17)$$

$$I_{D11} = 56.55\mu A \quad (2.18)$$

$$C_{M1} = 663fF \quad (2.19)$$

assuming all transistors  $M_{21}$  to  $M_{28}$  have the same  $V_{Dsat}$ . The values for  $\frac{W}{L}$  are then calculated as

$$\frac{W}{L} = \frac{g_m^2}{2KI_D} \quad (2.20)$$

with  $K = \mu C_{OX}$  a constant depending on the technology used. The only parameter left to be determined now is the size ratio of the class AB mesh formed by  $M_{13}$  and  $M_{14}$ . This mesh serves to fix the bias voltage of the output transistors, which has already been chosen by fixing  $V_{Dsat}$ . Since the cascode and output stage are designed with  $V_{Dsat} = 0.3V$ , the most logical choice is to use the same value for  $M_{13}$  and  $M_{14}$ , which will also simplify the reference circuit as discussed later. The only difference with transistors  $M_{23}$  and  $M_{25}$ , is the reduction of the tail current by a factor of 2, which immediately yields their sizing. The values for the transistor sizing as calculated, are given in table 2.12.

**Table 2.12:** Calculated dimensions of the opamp transistors

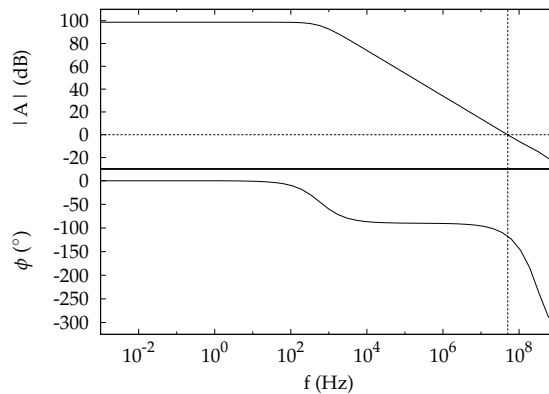
Device	$\frac{W}{L}$
$M_{11}$	67.85
$M_{12}$	25.13
$M_{13}$	30.00
$M_{14}$	11.11
$M_{21}$	33.33
$M_{23}$	22.22
$M_{25}$	59.99
$M_{31}$	69.44

The circuit is simulated using these parameters and tuned to ensure unity gain stability, leading to the final transistor dimensions in table 2.13. The value of the Miller capacitor had to be increased to 944.2fF instead of the calculated 663fF, to ensure stability.

The results of the AC small signal simulations are shown in Fig. 2.26 and summarized in table 2.14.

**Table 2.13:** Optimized component dimensions of the opamp

Device	Width	Length
M <sub>11</sub>	67.9μm	1μm
M <sub>12</sub>	25.1μm	1μm
M <sub>13</sub>	21.1μm	0.7μm
M <sub>14</sub>	7.8μm	0.7μm
M <sub>21</sub>	23.4μm	0.7μm
M <sub>23</sub>	15.6μm	0.7μm
M <sub>25</sub>	300μm	5μm
M <sub>31</sub>	69.4μm	1μm



**Figure 2.26:** Simulated amplitude and phase of the opamp

### Comparator

In contrast to the comparator used for the zeroth order amplifier, the input needs not be rail-to-rail since the output of the integrator is expected to be limited. As a result, a combination of the folded cascode amplifier described above and the output stage with current comparator as used in section 2.3 has been designed. The main difference compared to the opamp, is the doubling of the bias current and  $\frac{W}{L}$  of the transistors to keep the performance of the input stage and folded



Table 2.14: Simulation results of the opamp

Parameter	Value
Amplification	98.77dB
Bandwidth	581.6Hz
GBW product	50.5MHz
Phase margin	70.21°
Amplitude margin	-12.18dB

cascode, while making the output more responsive. The schematic of the comparator is shown in Fig. 2.27, with transistor sizes given in table 2.15.

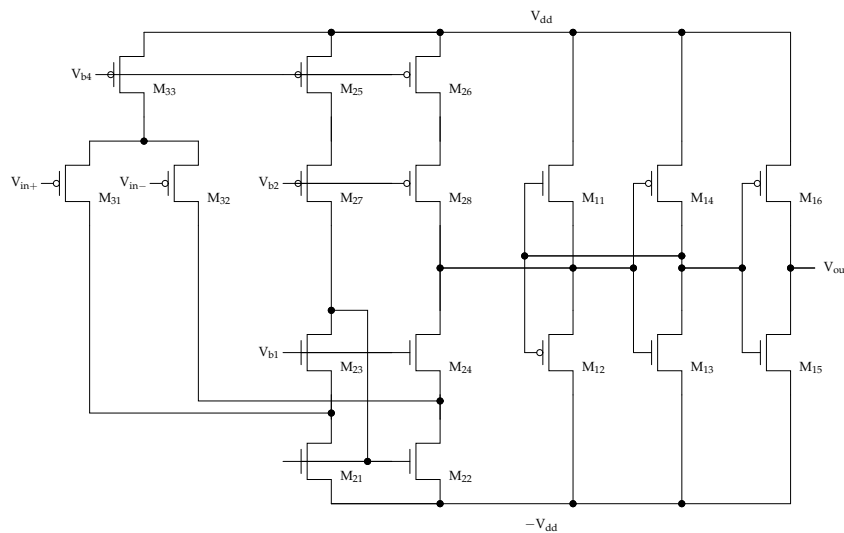
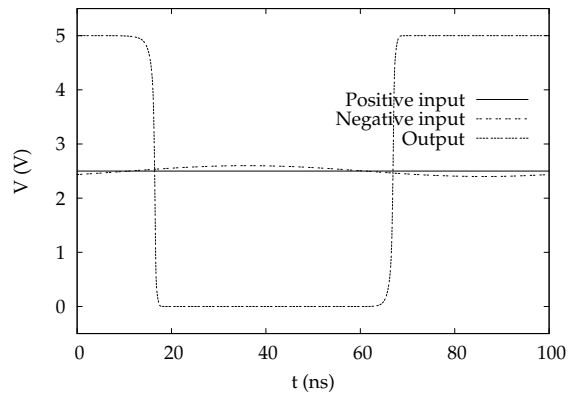
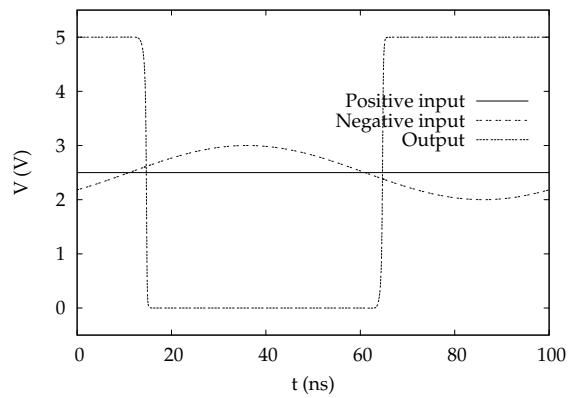


Figure 2.27: Schematic of the comparator

Since the output of the integrator is single ended, this is compared with a DC reference at half the supply voltage. The final result is, that simulations only need to be done at a single common mode input voltage with a single signal source, which is again the low pass filtered version of the output at a designed frequency of approximately 10MHz. The simulation results are depicted in Fig. 2.28 and the corresponding delay times are summarized in table 2.16. The resulting delay times are much more homogeneous than for the zeroth order comparator, both regarding direction of transition and input amplitude, due to a more robust design methodology.



(a) 2.5V DC, 100mV AC



(b) 2.5V DC, 500mV AC

Figure 2.28: Simulation of the comparator

**Table 2.15:** Transistor dimensions of the comparator

Device	Width	Length
M <sub>11</sub>	1μm	0.7μm
M <sub>12</sub>	2.7μm	0.7μm
M <sub>13</sub>	1μm	0.7μm
M <sub>14</sub>	2.7μm	0.7μm
M <sub>15</sub>	1μm	0.7μm
M <sub>16</sub>	2.7μm	0.7μm
M <sub>21</sub>	46.6μm	0.7μm
M <sub>23</sub>	31.1μm	0.7μm
M <sub>25</sub>	120μm	1μm
M <sub>31</sub>	138.9μm	1μm

**Table 2.16:** Delay times of the comparator

Transition	0.1V	0.5V
Low – high	5.92ns	3.70ns
High – low	5.42ns	6.66ns

### Biasing circuit

To ensure proper functioning of both opamp and comparator, voltage and current references of reasonable accuracy are required to keep the current sources and cascode transistors saturated. To minimize spread, the output should ideally not depend on sizing or technology related parameters. When using only mosfets, this is not possible, but with the circuit from Fig. 2.29, the output can be made a function of the threshold voltage by proper transistor sizing.

When all transistors operate in the saturated region, the basic equations are

$$I_D = \beta (V_{GS} - V_T)^2 \quad (2.21)$$

$$\beta = \frac{1}{2} \mu C_{OX} \frac{W}{L} \quad (2.22)$$

$$\Rightarrow V_{GS} = V_T + \sqrt{\frac{I_D}{\beta}} \quad (2.23)$$

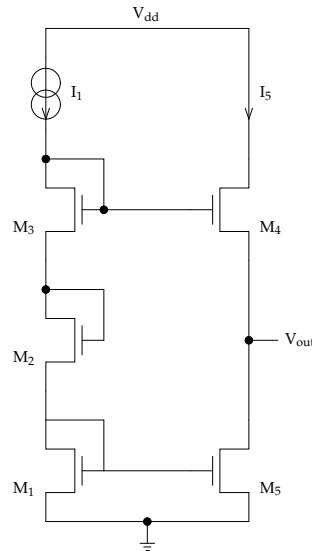


Figure 2.29: Diagram of the basic voltage reference

When applying these equations to Fig. 2.29, this yields

$$\begin{aligned} V_o &= V_{GS1} + V_{GS2} + V_{GS3} - V_{GS4} \\ &= 2V_T + 3\sqrt{\frac{I_1}{\beta}} - \sqrt{\frac{I_5}{\beta}} \end{aligned} \quad (2.24)$$

when transistors  $M_1$  to  $M_4$  are identical. This can be further simplified to

$$V_o = 2V_T \quad (2.25)$$

if the current  $I_5 = 9I_1$  by choosing  $\left(\frac{W}{L}\right)_5$  9 times wider than  $\left(\frac{W}{L}\right)_1$ .

The final implementation of the complete reference circuit is shown in Fig. 2.30. The main difference with the basic structure from Fig. 2.29 is the replacement of  $M_2$  by a PMOS. As a result, equation (2.25) now becomes

$$V_o = V_{TN} - V_{TP} \quad (2.26)$$

with  $V_{TN}$  and  $V_{TP}$  the threshold voltages of NMOS and PMOS respectively. Although not ideal from an accuracy point of view, this was preferred, since the required voltage levels were found to be almost symmetrical to the supply rails. Additional fine tuning of the "foreign" transistor dimensions then allows for a slight adjustment of the output voltage.

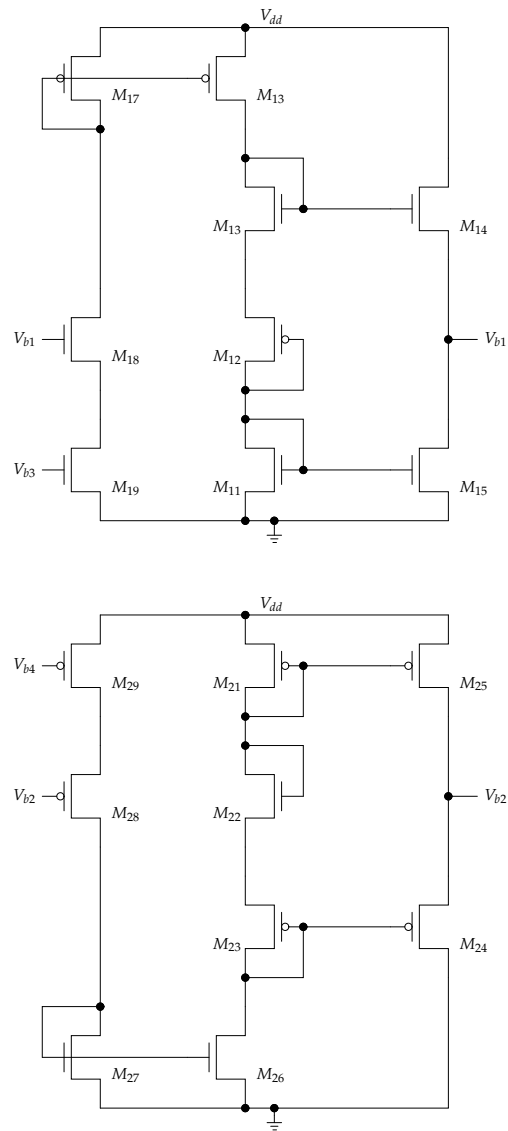


Figure 2.30: Schematic of the biasing circuit

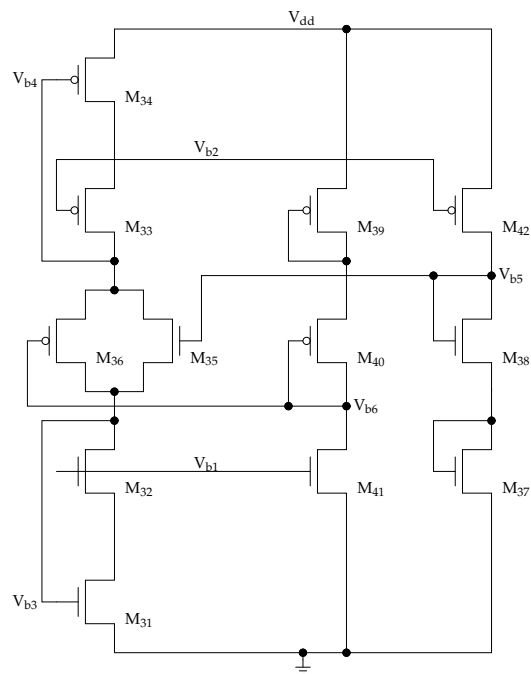


Figure 2.30: Schematic of the biasing circuit (cont.)

## 2.4 First order

45

The additional circuitry from Fig. 2.30 implements the remaining biasing of the current sources and the class AB mesh. Since the cascode, the output and the mesh transistors from the opamp in Fig. 2.25 were designed with identical  $V_{Dsat}$ ,  $M_{37}$  to  $M_{40}$  can have the same dimensions as  $M_{31}$  and  $M_{33}$  if they conduct the same current. The reference current is chosen 5 times smaller than for the opamp circuit, so the size ratio must be 5 times smaller as well. Table 2.17 gives a summary of all transistor dimensions, table 2.18 shows the resulting output voltages and currents.

**Table 2.17:** Transistor dimensions of the reference circuit

Device	Width	Length
$M_{11,13,14}$	$1.6\mu\text{m}$	$1\mu\text{m}$
$M_{12}$	$4.3\mu\text{m}$	$1\mu\text{m}$
$M_{15}$	$14.4\mu\text{m}$	$1\mu\text{m}$
$M_{16,17}$	$4.4\mu\text{m}$	$1\mu\text{m}$
$M_{18,19}$	$22.2\mu\text{m}$	$5\mu\text{m}$
$M_{21,23,24}$	$3.1\mu\text{m}$	$0.7\mu\text{m}$
$M_{22}$	$1.1\mu\text{m}$	$0.7\mu\text{m}$
$M_{25}$	$27.9\mu\text{m}$	$0.7\mu\text{m}$
$M_{26,27}$	$1.6\mu\text{m}$	$1\mu\text{m}$
$M_{28,29}$	$60\mu\text{m}$	$5\mu\text{m}$
$M_{31,32,37,38}$	$22.2\mu\text{m}$	$5\mu\text{m}$
$M_{33,34,39,40}$	$60\mu\text{m}$	$5\mu\text{m}$
$M_{35}$	$11.1\mu\text{m}$	$5\mu\text{m}$
$M_{36}$	$30\mu\text{m}$	$5\mu\text{m}$
$M_{41}$	$1\mu\text{m}$	$2\mu\text{m}$
$M_{42}$	$2.2\mu\text{m}$	$1\mu\text{m}$

### Output stage

The output stage has undergone a major revision, not so much in basic structure as in sizing, to decrease overall power consumption. First of all, the size of the output transistors is drastically reduced to 60 parallel NDMOS transistors with a width of  $100\mu\text{m}$  and 60 parallel PDMOS transistors with a width of  $150\mu\text{m}$  each, to reduce the parasitic capacitances and the feed-through currents. Additionally, the parallel diodes were removed, since they did not seem to significantly affect

**Table 2.18:** Voltages and currents from the reference circuit

Parameter	Value
$V_{b1}$	1.60V
$V_{b2}$	3.37V
$V_{b3}$	0.99V
$V_{b4}$	3.77V
$V_{b5}$	2.36V
$V_{b6}$	2.27V
$I_{D,M31}$	10.49 $\mu$ A

the performance and behaviour of the circuit. As a result, the reverse currents will flow through the parasitic diodes of the output transistors.

The transistor dimensions of the level shifter are also slightly changed, leading to less power consumption and a more homogeneous delay time of 2.5ns for both rising and falling edge. The buffer stage, however, is chosen to have an almost identical driving strength as with the zeroth order driver, which, combined with the reduced output transistors, results in steeper slopes and an even reduced chance of parasitic DMOS turn-on.

Finally, this also leads to an optimized delay circuit further preventing feed-through, which, again, is more symmetric because of the modified level shifter.

An alternative output stage is given in Fig. 2.31, where the DMOS transistors are used in a cascode stage. Since their gates are connected directly to a supply rail, parasitic turn-on should be non-existent. Furthermore, the gates of the mosfets are much smaller than the corresponding DMOS gates — the same total width, but a smaller length of 0.7 $\mu$ m — which in turn might lead to steeper output slopes and an even reduced turn-on delay. However, this delay is chosen identical, so an improved efficiency is to be expected.

The transistor dimensions of the level shifter, NDMOS buffer and delay circuit are summarized in tables 2.19 and 2.20, using the naming conventions from Fig. 2.6 and 2.9.

### Full simulation

The divider circuit for this amplifier is shown in Fig. 2.32 and provides the division by 10 to avoid breakdown, in addition to a supplementary division by 2 caused by the differential nature of the amplifier, leading to an overall division by 20. The connection to the 5V supply rail then shifts the common mode level to 2.5V for symmetry reasons. Additionally, the sizing of the resistors is chosen



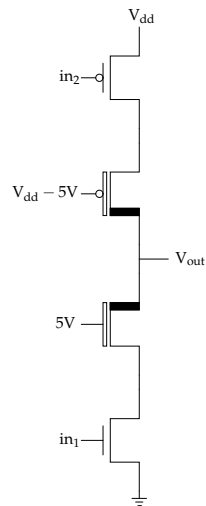


Figure 2.31: Diagram of the cascode output stage

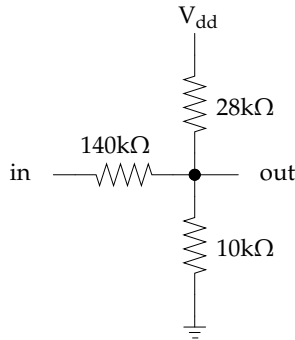
Table 2.19: Transistor dimensions of level shifter and buffer

Device	Width	Length
M <sub>1</sub>	10 $\mu\text{m}$	4 $\mu\text{m}$
M <sub>2</sub>	7 $\mu\text{m}$	1 $\mu\text{m}$
M <sub>3</sub>	25 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>4</sub>	75 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>5</sub>	100 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>6</sub>	300 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>7</sub>	300 $\mu\text{m}$	0.7 $\mu\text{m}$
M <sub>8</sub>	900 $\mu\text{m}$	0.7 $\mu\text{m}$

**Table 2.20:** Transistor dimensions of the delay circuit

Device	Width	Length
N <sub>1,2,N</sub>	5μm	0.7μm
N <sub>1,2,P</sub>	13.5μm	0.7μm
I <sub>1,N</sub>	1μm	0.7μm
I <sub>1,P</sub>	2.7μm	0.7μm
I <sub>2,N</sub>	20μm	0.7μm
I <sub>2,P</sub>	54μm	0.7μm
I <sub>3,N</sub>	1μm	0.7μm
I <sub>3,P</sub>	2.7μm	0.7μm
I <sub>4,5,N</sub>	1μm	10μm
I <sub>4,5,P</sub>	2.7μm	10μm
I <sub>6,7,N</sub>	1μm	8.6μm
I <sub>6,7,P</sub>	2.7μm	8.6μm

such that the resistor, in combination with its parasitic capacitance and the time delays of the loop, set the oscillating frequency again at 10MHz.



**Figure 2.32:** Schematic of the divider

The only variable left in the circuit, is the unity gain frequency of the integrator. By choosing all resistors 250kΩ and the capacitors 159fF, this yields 4MHz, which still provides gain to reduce signal distortion and filters the oscillation frequency. Simulations on both circuits were performed using a sinewave input at 200kHz, with 447mV amplitude, which is then amplified by a factor of 10 towards the 100Ω load, leading to 100mW output power conform the ADSL specification. Figures 2.33 and 2.34 show details of the waveforms at the input and output of the amplifier stage, where the increased buffer to gate area ratio demonstrates the reduced risk of DMOS turn-on compared to Fig. 2.17. Further simulation results are given in Fig. 2.35 to 2.38, showing the filtered out-

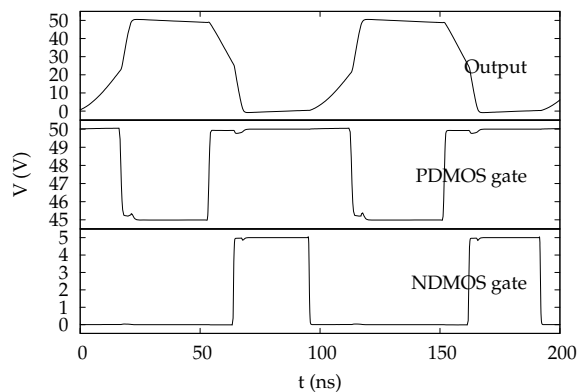


Figure 2.33: Simulation of DMOS in and outputs, basic version

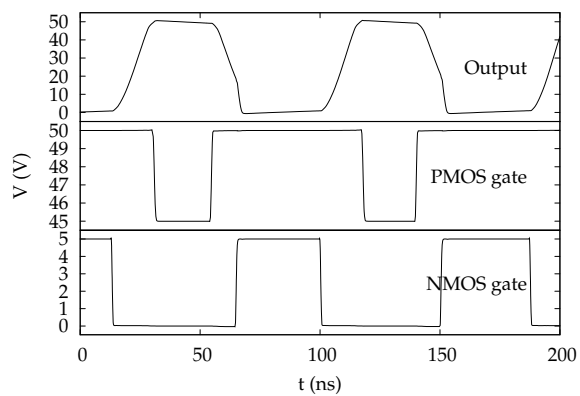


Figure 2.34: Simulation of DMOS in and outputs, cascode version

put and its spectrum. The simulation results are summarized in table 2.21. While the cascode version turns out to be the more efficient one with a slightly lower second order distortion, it also has the highest third order distortion, so there is no clear winner.

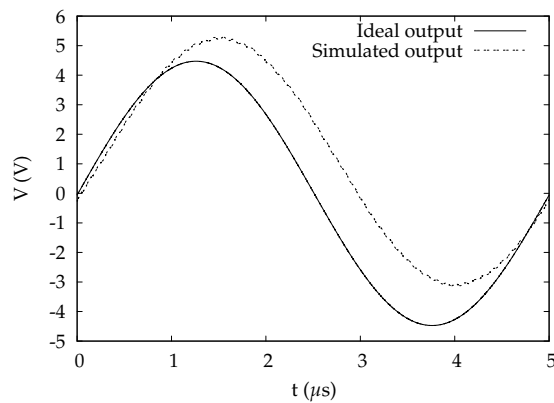


Figure 2.35: Simulated output of the basic amplifier @ 200kHz reference signal

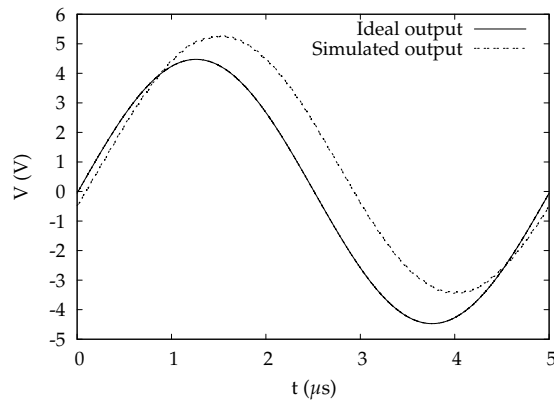


Figure 2.36: Simulated output of the cascode amplifier @ 200kHz reference signal

However, for an xDSL line driver, harmonic distortion is not really a good measure of linearity, since all specifications are based upon the multitone power ratio (MTPR). For this test, a DSL like signal, composing of all but some DMT tones, is amplified by the line driver and the MTPR is determined as the difference between the nominal tone power and the power measured at the missing tone frequency. Depending on the source, this ratio should be between 55dB and 65dB.

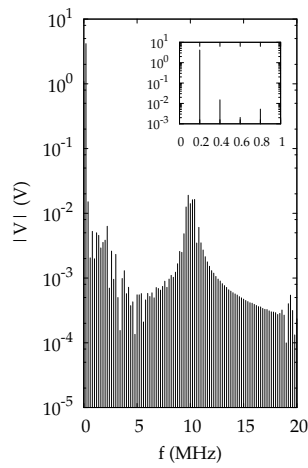


Figure 2.37: Simulated spectrum of the basic amplifier @ 200kHz reference signal

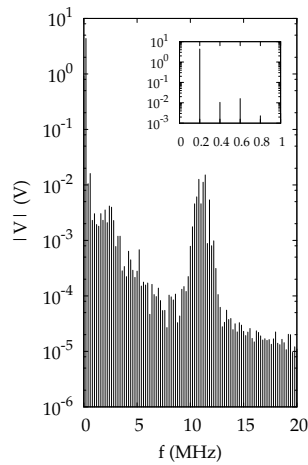


Figure 2.38: Simulated spectrum of the cascode amplifier @ 200kHz reference signal

**Table 2.21:** Summary of the simulation results

	Basic	Cascode
Oscillating frequency	10.1MHz	11.2MHz
$P_{50V}$	2.00W	1.30W
$P_{45V}$	-247mW	-184mW
$P_{5V}$	19.9mW	22.0mW
$P_{out}$	98.8mW	103.4mW
Efficiency @ 447mV input sinewave	5.55%	9.09%
Second harmonic	-48.84dBc	-52.35dBc
Third harmonic	-66.16dBc	-48.68dBc

So why not simulate conform the specifications? The main reason is simulation time. A MTPR signal is the sum of hundreds of sinewaves, spaced 4.3125kHz apart, leading to a 232 $\mu$ s period, which needs to be simulated a couple of periods to get sufficient accuracy for the FFT. Given the asynchronous nature of the amplifier, this would take days of simulation time, just for 1 possible CF.

As a result, a different approach is chosen, using the THD as a first parameter for optimizations, before performing a DC sweep on the amplifier. Using these simulation results, a piecewise linear approximation of the amplifier transfer is created, that can be used to calculate the expected response. The condition for this approach to be valid, is the assumption that the phase of the input signal changes monotonically but not significantly during one period of the oscillating frequency, so that the low pass filtered output signal can be considered a valid representation for that entire oscillation period. Given a nominal oscillating frequency of over 10MHz and a maximum signal frequency of 1.1MHz, both conditions can be considered fulfilled.

The DC linearity curves are simulated for both amplifiers, of which the results are depicted in Fig. 2.39. From this, it is to be expected that both amplifiers offer an almost identical linearity performance. After calculating the corresponding response, the MTPR is found to be 36dB for the basic amplifier and 35dB for the cascode amplifier.

An additional benefit of this technique, under the same assumptions, is that it can be used to predict the efficiency as well. In general, the efficiency is given by

$$\eta = \frac{\int_{V_a}^{V_b} pdf(V)P_{out}(V)dV}{\int_{V_a}^{V_b} pdf(V)P_{in}(V)dV} \quad (2.27)$$

where  $pdf(V)$  is the probability density function of the signal and  $P_{in}(V)$  and  $P_{out}(V)$  the DC input and output power for the given amplitude range. The DC efficiency is simply  $P_{out}/P_{in}$ , since in this case  $pdf(V) = \delta(V - V_{out})$ .

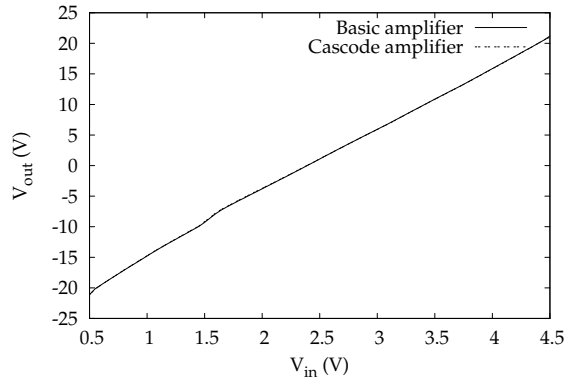


Figure 2.39: Simulated linearity of both amplifiers

It can be shown that the pdf of a xDSL signal is given by [6]

$$pdf(V) \approx \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{V^2}{2\sigma^2}} \quad (2.28)$$

where  $\sigma$  is the rms-value of the output signal, i.e.  $\sigma = \sqrt{10V}$ .

After substituting  $P_{out} = \frac{V^2}{R}$  for the DC output power, there are 2 ways to proceed. First of all one can use numerical integration on the simulated data points in Fig. 2.40, yielding 9.67% and 9.94% for the basic and cascode amplifier respectively. The second possibility starts from the observation that  $P_{in}$  can be approximated by

$$P_{in}(V) \approx aV^2 + b \quad (2.29)$$

where the quadratic form stems from the observation that the output power quadratically depends on the output voltage and the load resistance  $R_{load}$ , and the passive termination, which ideally is the only additional source of dissipation, simply doubles this to yield the input power. As a result, the factor  $a$  should be  $\frac{2}{R_{load}}$ , with  $b$  the static dissipation of the amplifier, so the efficiency can be calculated by evaluating an analytical expression. In this case, the calculation yields 10.06% and 10.18% respectively, so the results of both methods are in close correspondence.

Table 2.22 gives an overview of all calculated results for an MTPR stimulus. Comparing these results with the THD results from table 2.21, the cascode amplifier still has a slight efficiency advantage at the cost of some linearity, but the differences are less pronounced as with the THD simulations. The cascode amplifier however will be the most expensive solution, since it needs more silicon area than the basic version.

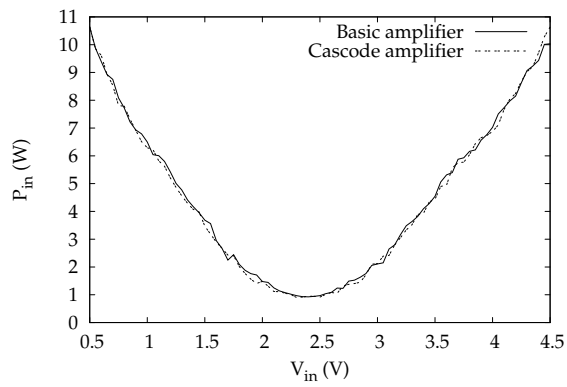


Figure 2.40: Simulated input power of both amplifiers

Table 2.22: Summary of the calculated results

	Basic	Cascode
MTPR	36dB	35dB
Efficiency (numerical integration)	9.67%	9.94%
Efficiency (quadratic approximation)	10.06%	10.18%



### 2.4.2 Layout and measurement results

Both the basic and cascode amplifier are processed in the AMIS I<sup>2</sup>T100 high voltage 0.7 $\mu$ m CMOS technology. In contrast to the zeroth order amplifier, no measurement pads were inserted to get better correspondence between simulations and measurements. Additionally, the biasing circuit is provided separately to verify its outputs.

Both die micrographs with annotations are shown in Fig. 2.41 - 2.42, the version with the basic output stage measuring 3.6mm<sup>2</sup> and the cascode output stage measuring 4.3mm<sup>2</sup>.

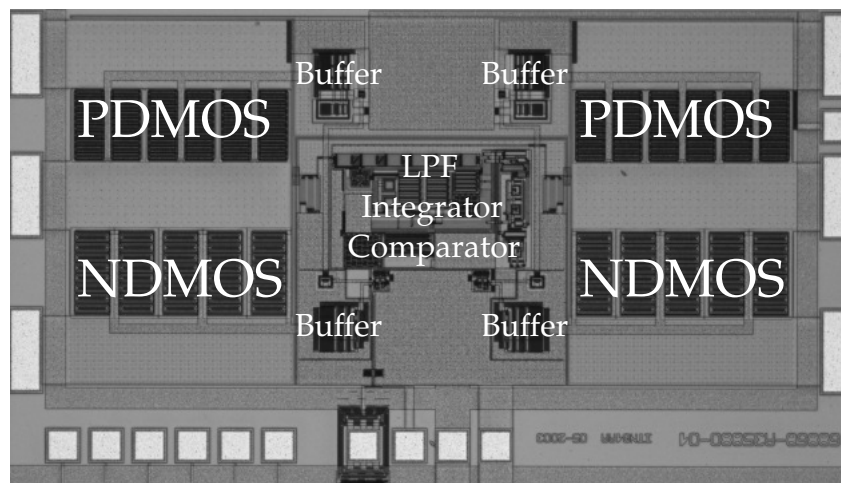


Figure 2.41: Die photograph of the amplifier processed, basic output stage

#### Reference circuit

The voltage levels from Fig. 2.30 are measured on 18 different circuits, leading to the values in table 2.23. In general it can be concluded that simulation and measurement correspond very well, with little process variation between different circuits.

#### Amplifiers

A first important observation when characterizing both amplifiers, was a significant reduction of the oscillating frequency, from over 10MHz simulated to 4.7MHz measured for both circuits. As a result, the amplifiers are expected to be somewhat more efficient, but less linear. This discrepancy was tracked down

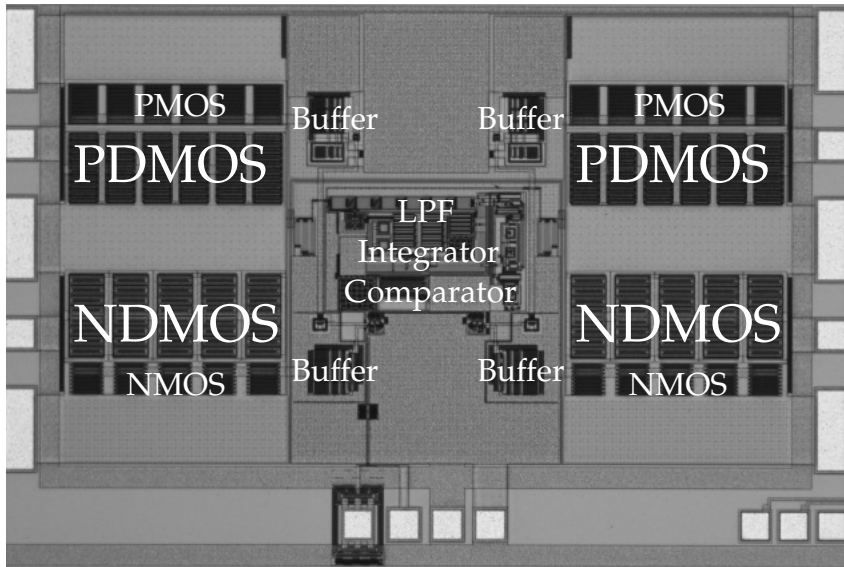


Figure 2.42: Die photograph of the amplifier processed, cascode output stage

Table 2.23: Measured voltages from the reference circuit

Parameter	Simulated value	Average value	Standard deviation
$V_{b1}$	1.60V	1.65V	0.07V
$V_{b2}$	3.37V	3.43V	0.03V
$V_{b3}$	0.99V	0.97V	0.01V
$V_{b4}$	3.77V	3.75V	0.01V
$V_{b5}$	2.36V	2.26V	0.03V
$V_{b6}$	2.27V	2.16V	0.04V

## 2.4 First order

57

to extra parasitics introduced by the layout and missing modelling of parasitic capacitances in certain components. A post layout simulation including these parasitics showed a reduction to 6MHz, in close correspondence with the measurements.

Extensive linearity and efficiency measurements were performed on both amplifiers. Figures 2.43 and 2.44 show the simulated and measured curves of the linearity of both amplifiers and Fig. 2.45 depicts the measured results together.

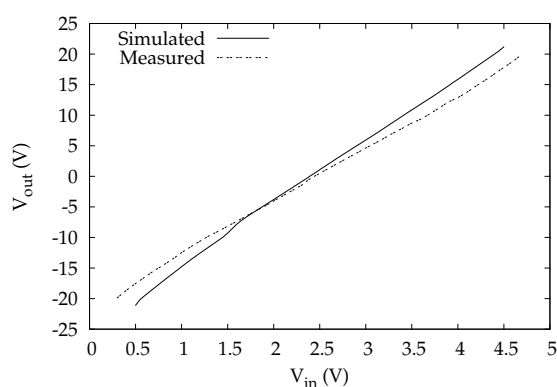


Figure 2.43: Simulated and measured linearity of the basic amplifier

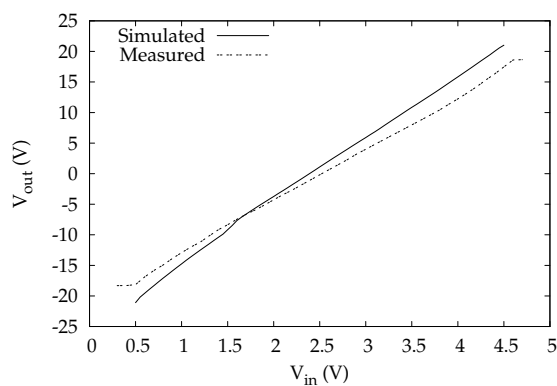


Figure 2.44: Simulated and measured linearity of the cascode amplifier

When comparing simulations and measurements of both amplifiers, two common differences can be observed. First of all, the measurements show a reduced amplification for the middle voltage range, which first diminishes even further

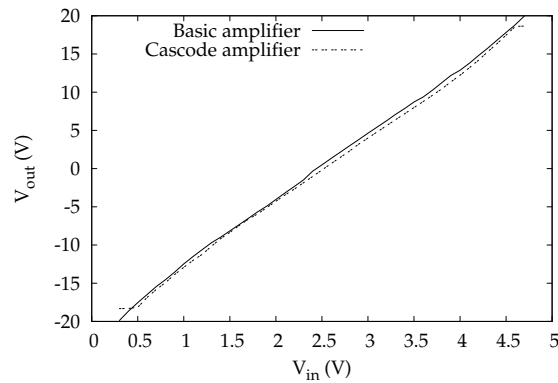


Figure 2.45: Measured linearity of both amplifiers

and then increases when approaching the supply rails. This can be explained by the inherent reduction of the switching frequency at increasing amplitudes, combined with the time delays introduced by the control loop. Second, the response seems to be less linear than simulated, but on the other hand, there is no twist anymore around the input voltage of 1.5V. Besides these effects, the cascode amplifier also saturates earlier due to the additional voltage drop over the cascode transistors, while the basic version seems less linear in general. As a result, it is not immediately clear which amplifier is the most linear.

The power consumption for these DC measurements is given in Figures 2.46 to 2.48. The measurements yield favourable results, due to the lower switching frequency, as expected. Again, there is no significant difference between both versions of the amplifier, so the final MTPR measurements will be decisive.

The full downstream spectrum as measured is shown in Fig. 2.49. The minimum MTPR was 40dB for the basic version and 39dB for the cascode amplifier, where the basic version reaches values of over 45dB as in Fig. 2.50. The power consumption was 765mW and 778mW respectively, so the basic amplifier turns out to be the best solution.

In general, this means that the calculated values for linearity and efficiency slightly underestimate the measured performance, illustrating the usefulness of this technique.

Table 2.24 summarizes the measurement results and compares with references [7] and [8]. While it is much harder to reach the linearity achieved by a class AB amplifier, the efficiencies of both amplifiers are comparable. It should be noted however, that while class AB amplifiers can use active termination, switching amplifiers are stuck with passive termination and filtering, due to the absence of an appropriate feedback path. As a result, the matching and filtering circuit will

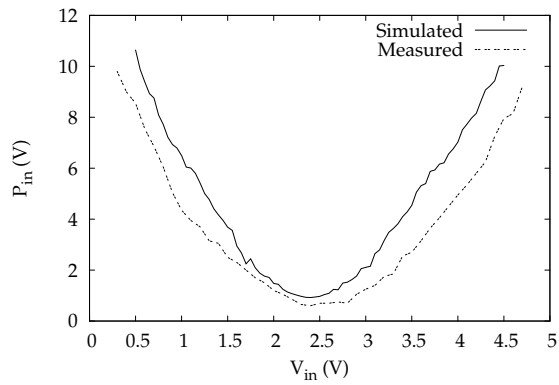


Figure 2.46: Simulated and measured input power of the basic amplifier

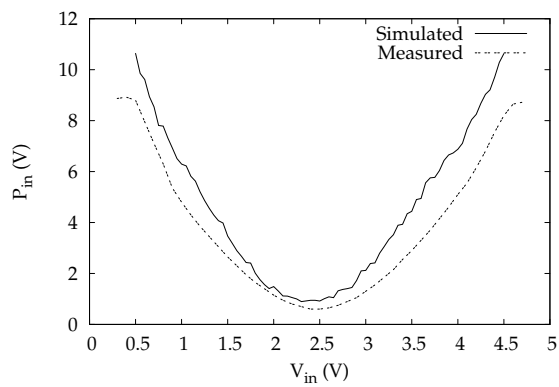


Figure 2.47: Simulated and measured input power of the cascode amplifier

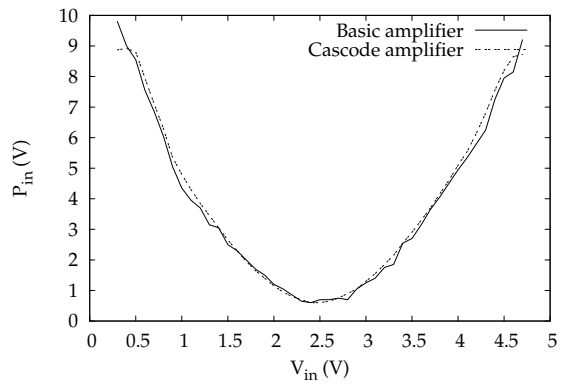


Figure 2.48: Measured input power of both amplifiers

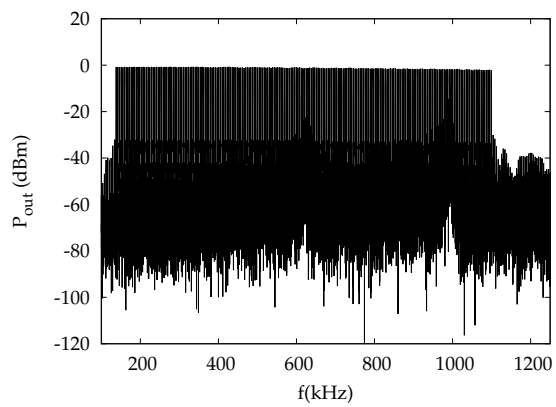


Figure 2.49: Full-rate ADSL output spectrum

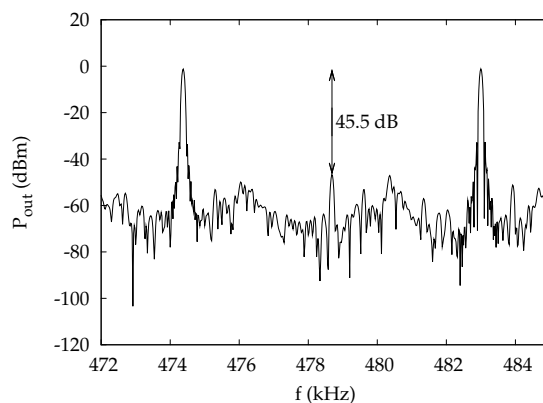


Figure 2.50: Detail of the MTPR output spectrum

dissipate at least the output power and require a doubling of the supply voltage ( $\pm 25V$  versus  $\pm 12V$ ), thus effectively halving the maximum achievable efficiency to less than 50%.

Table 2.24: Comparison of measurement results

	Basic	Cascode	Reference [7]	Reference [8]
Class	D	D	G	AB
Termination	passive	passive	active	active
Supply voltage	$\pm 25V$	$\pm 25V$	$\pm 3V$	$\pm 12V$
Power consumption	765mW	778mW	700mW	740mW
Efficiency	13.1%	12.9%	14.3%	13.5%
MTPR	40dB	39dB	72dB	75dB
Process	I <sup>2</sup> T100 0.7 $\mu$ m	I <sup>2</sup> T100 0.7 $\mu$ m	0.25 $\mu$ m CMOS	XFCB-26V
Die size	3.6mm <sup>2</sup>	4.3mm <sup>2</sup>	5.3mm <sup>2</sup>	3.36mm <sup>2</sup>

## 2.5 Conclusion

A zeroth and first order line driver are simulated and characterized. In general, the functionality of this amplifier is verified, with simulations and measurements corresponding well. Both amplifiers however do not meet the specifications yet,

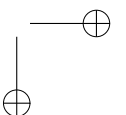
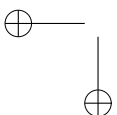
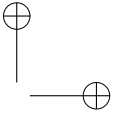
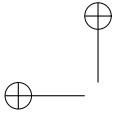
so the next steps are as follows.

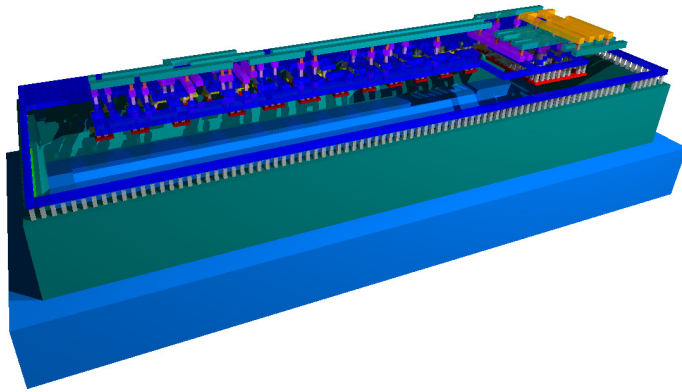
To increase the linearity, alternative loop filters must be investigated. Additionally, increasing the oscillating frequency also has a positive impact, so changing to a high voltage extension of a  $0.35\mu\text{m}$  technology will be favourable. As a side effect, the more efficient high voltage devices in this technology are also expected to further increase the efficiency.



## References

- [1] *Asymmetric digital subscriber line (ADSL) transceivers*, ITU-T Recommendation G.992.1, Jul. 1999.
- [2] Europractice IC service. (2007, Mar.) AMI Semiconductor I2T100 technology. [Online]. Available: [http://www.europractice-ic.com/docs/AMIS.datasheets/AMIS\\_I2T100.v8.pdf](http://www.europractice-ic.com/docs/AMIS.datasheets/AMIS_I2T100.v8.pdf)
- [3] J. Doutreloigne, H. De Smet, J. Van den Steen, and G. Van Doorselaer, "Low-power high-voltage CMOS level-shifters for liquid crystal display drivers," in *Proceedings of the 11th international conference on microelectronics*, State of Kuwait, Nov. 1999, pp. 213–216.
- [4] B. J. Baliga, *Modern Power Devices*. Malabar, Florida: Krieger Publishing Company, 1992.
- [5] W. Redman-White, "A high bandwidth constant  $g_m$  and slew-rate rail-to-rail CMOS input circuit and its application to analog cells for low voltage VLSI systems," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 701–712, May 1997.
- [6] D. J. G. Mestdagh, P. M. P. Spruyt, and B. Biran, "Effect of amplitude clipping in DMT-ADSL transceivers," *Electronics Letters*, vol. 29, no. 15, pp. 1354–1355, July 22 1993.
- [7] A. Bicakci, C.-S. Kim, and S.-S. Lee, "A CMOS line driver for ADSL central office applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2201–2208, Dec. 2003.
- [8] F. Sabouri and R. Shariatdoust, "A 740mW ADSL line driver for central office with 75dB MTPR," in *ISSCC Digest of Technical Papers*, San Francisco, USA, Feb. 2002, pp. 322–323.





# 3

## Theory of operation

This chapter provides a numerical framework, to predict the most important properties of an asynchronous amplifier, being its oscillating frequency and distortion. The formulæ will first be derived and later verified by block level simulations.

### 3.1 Introduction

In chapter 2, two different silicon implementations of the basic principle are demonstrated. However, the design path followed merely consists of a trial-and-error method, so the question arises if there is a way to more systematically describe the functioning and performance of the circuit. Since there is a plethora of methods for describing linear circuits, the main challenge is to accurately model the non-linearity introduced into the system by the comparator.

Existing techniques, such as direct time domain response calculation as utilized with classical PWM and the z-domain representation adopted with  $\Sigma\Delta$  converters, are not readily available for the asynchronous amplifier. The main difference is the absence of a fixed time base, such as a clock or sawtooth, in favour of the output square wave, filtered to a sawtooth like reference with an input dependent period.

As such, a different approach will be followed, describing the non-linearity in a linearized way, combined with a direct time domain description to predict the

linearity performance of the system.

In section 3.2, the technique used to linearize a non-linearity will be discussed. Section 3.3 will further expand the behavioural description of the system to linearity prediction and in section 3.4 both techniques will be verified using block level numerical simulations.

## 3.2 Describing functions linearization

### 3.2.1 Small and large signals

The main objective of this section is to derive a suitable linear approximation of a non-linear component and calculate the resulting transfer function in the case of an ideal comparator without hysteresis. A first source of inspiration is the technique used in the small signal analysis of non-linear systems. In this case, the non-linearity is a smooth function where both this function and its first derivative are continuous in a given interval and the input signal is considered sufficiently small so as to not have a significantly distorted output response. To calculate the resulting small signal output, the input signal is simply multiplied by the first derivative of the non-linearity at the DC working point. The resulting output signal then is the superposition of this small signal output and the DC response. This method is illustrated in Fig. 3.1 in the simple case of an exponential transfer function, as used frequently to model bipolar components.

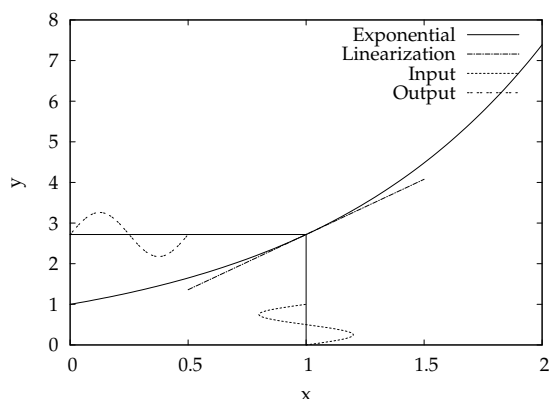


Figure 3.1: Exponential transfer function with small signal parameters

However, as already mentioned before, the input signal to the non-linearity will be a low-pass filtered square wave with significant amplitude, rendering the above method invalid. This can be demonstrated using the exponential function

### 3.2 Describing functions linearization

from Fig. 3.1:

$$V_{out} = e^{V_{in}} \tag{3.1}$$

For a small signal analysis, the resulting output simply is

$$e^A + e^A B \sin(2\pi ft) \tag{3.2}$$

for a sinusoidal input signal  $V_{in} = A + B \sin(2\pi ft)$  with offset  $A$ , amplitude  $B$  and frequency  $f$ . This linearized output and the exact output from equation (3.1) are shown in Fig. 3.2 for an input signal  $V_{in} = 1 + \sin(2\pi t)$ . Besides the noticeable distortion from the exponential function causing an increased peak-to-peak value, there also is a significant difference in average value, increasing from 2.72 for the linearized version to 3.44 for the exact response.

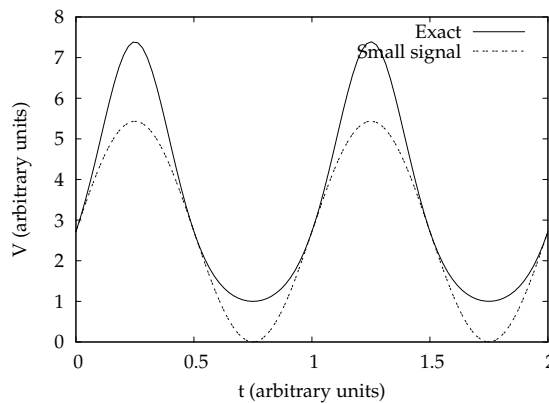


Figure 3.2: Exact and small signal output response

As a result, for larger signals, the linearized description of the circuit involves the construction of a linear approximator for *each* input signal instead of a single function for all inputs as with linear systems. This corresponds with the observation that the goal is not to derive a “one function always describes” technique, but a means to accurately and systematically describe a system in a strictly defined environment. A general block level diagram of this non-linear component is shown in Fig. 3.3, together with a representation of its linear approximation.

#### 3.2.2 Large signal approximation

The outcome of the previous section now leads to the starting point of the describing function theory, where a set of functions  $w_i(t)$  needs to be found, possibly depending on all input variables and minimizing the mean squared error of the output signal:

$$e(t) = y_a(t) - y(t) \tag{3.3}$$

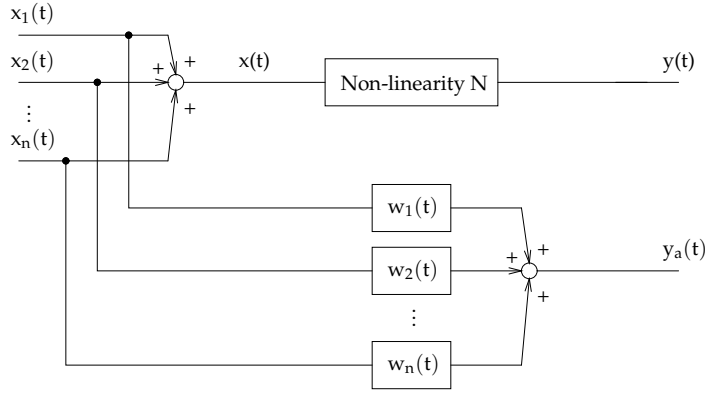


Figure 3.3: Block diagram of non-linearity and approximation

where  $y(t)$  is the ideal output signal,  $y_a(t)$  the approximated output and  $e(t)$  the error signal, with a mean squared value

$$\overline{e(t)^2} = \overline{y_a(t)^2} - 2\overline{y_a(t)y(t)} + \overline{y(t)^2} \quad (3.4)$$

Further using the notations from Fig. 3.3,  $y_a(t)$  can be written as

$$y_a(t) = \sum_{i=1}^n \int_0^\infty w_i(\tau) x_i(t - \tau) d\tau \quad (3.5)$$

and

$$\overline{y_a(t)^2} = \sum_{i=1}^n \sum_{j=1}^n \int_0^\infty d\tau_1 \int_0^\infty d\tau_2 w_i(\tau_1) w_j(\tau_2) \varphi_{ij}(\tau_1 - \tau_2) \quad (3.6)$$

where

$$\varphi_{ij}(\tau) = \overline{x_i(t) x_j(t + \tau)} \quad (3.7)$$

After assuming a small variation on the optimal value of the approximator  $w_i(t)$

$$w_i(t) = w_{oi}(t) + \delta w_i(t) \quad (3.8)$$

equation (3.4) can be further rewritten as

$$\overline{e(t)^2} = \overline{e(t)_0^2} + \delta \overline{e(t)^2} + \delta^2 \overline{e(t)^2} \quad (3.9)$$

### 3.2 Describing functions linearization

69

where

$$\begin{aligned} \overline{e(t)}_0^2 = & \sum_{i=1}^n \sum_{j=1}^n \int_0^\infty d\tau_1 \int_0^\infty d\tau_2 w_{oi}(\tau_1) w_{oj}(\tau_2) \varphi_{ij}(\tau_1 - \tau_2) \\ & - 2 \sum_{i=1}^n \int_0^\infty d\tau_1 w_{oi}(\tau_1) \overline{y(t)x_i(t - \tau_1)} + \overline{y(t)}^2 \end{aligned} \quad (3.10)$$

$$\delta \overline{e(t)}^2 = 2 \sum_{i=1}^n \int_0^\infty d\tau_1 \delta w_i(\tau_1) \left[ \sum_{j=1}^n \int_0^\infty d\tau_2 w_{oj}(\tau_2) \varphi_{ij}(\tau_1 - \tau_2) - \overline{y(t)x_i(t - \tau_1)} \right] \quad (3.11)$$

$$\delta^2 \overline{e(t)}^2 = \sum_{i=1}^n \sum_{j=1}^n \int_0^\infty d\tau_1 \int_0^\infty d\tau_2 \delta w_i(\tau_1) \delta w_j(\tau_2) \varphi_{ij}(\tau_1 - \tau_2) \quad (3.12)$$

For the solution  $w_{oi}(t)$  to be a minimum, the first order error from equation (3.11) should be zero for every  $\delta w_i(\tau_1)$ , which holds if for every possible  $i$

$$\sum_{j=1}^n \int_0^\infty d\tau_2 w_{oj}(\tau_2) \varphi_{ij}(\tau_1 - \tau_2) - \overline{y(t)x_i(t - \tau_1)} = 0 \quad (3.13)$$

which leads to the conclusion that the input-output cross-correlations of the ideal result and the approximation must be equal:

$$\overline{x_i(t)y(t + \tau_1)} = \overline{x_i(t)y_a(t + \tau_1)} \quad (3.14)$$

When combining these equations with the observation that the input and error signal are not correlated and the cross-correlation between the ideal and approximated outputs equals the autocorrelation of the approximated output, equation (3.13) can be rewritten as

$$\int_0^\infty w_{oi}(\tau_2) \varphi_{ii}(\tau_1 - \tau_2) d\tau_2 = \overline{y(t)x_i(t - \tau_1)} \quad (3.15)$$

under the assumption that all input signals are uncorrelated.

From this it can be concluded that, although the input signals are statistically independent and the resulting signals for every approximator are uncorrelated, the approximator parameters will still depend on the nature of *every* input signal, due to the dependency of equation (3.15) on the exact output  $y(t)$ . This, of course, corresponds to the absence of superposition in non-linear circuits.

Furthermore, since equations (3.6) and (3.12) have the same form, the second order term of the error will always be positive, thus the solution will be a minimum.

### 3.2.3 An example

This theory can now be applied to the exponential transfer function from Fig. 3.1. From Fig. 3.2 it became clear that the small signal approximation failed to accurately predict both the offset and amplitude, so now the question arises if and to which extent the result from equation (3.15) is the better method.

#### Offset

Using equation (3.15) directly on the transfer from equation (3.1), with an input signal

$$V_{in} = A + B \sin(2\pi ft) \quad (3.16)$$

this immediately leads to

$$\int_0^\infty w_A(\tau_2) A^2 d\tau_2 = A \overline{y(t)} \quad (3.17)$$

which is fulfilled if

$$w_A(\tau_2) = \frac{1}{A} \overline{y(t)} \delta(\tau_2) \quad (3.18)$$

with  $\delta(\tau)$  the impulse function. As a result, in this case a suitable approximator for the DC component is a static gain block with value

$$N_A(A, B) = \frac{1}{A} \overline{y(A, B, t)} \quad (3.19)$$

which is called the *describing function* for the bias component  $A$ . This leads to exactly the average value of the analytical solution, as calculated in section 3.2.1. Thus, from a bias point of view, the describing function approximation is the better technique.

#### Sinewave

The bias response however is only part of the solution, so the AC response needs to be calculated as well. In this case, the autocorrelation is readily calculated as

$$\varphi_{ii}(\tau) = \frac{1}{2} B^2 \cos(2\pi f\tau) \quad (3.20)$$



### 3.2 Describing functions linearization

71

leading to

$$\begin{aligned}
 \int_0^\infty w_{oi}(\tau_2) \varphi_{ii}(\tau_1 - \tau_2) d\tau_2 &= \int_0^\infty w_{oi}(\tau_2) \frac{B^2}{2} \cos(2\pi f(\tau_1 - \tau_2)) d\tau_2 \\
 &= \frac{B^2}{2} \cos(2\pi f\tau_1) \int_0^\infty w_{oi}(\tau_2) \cos(2\pi f\tau_2) d\tau_2 \\
 &\quad + \frac{B^2}{2} \sin(2\pi f\tau_1) \int_0^\infty w_{oi}(\tau_2) \sin(2\pi f\tau_2) d\tau_2
 \end{aligned} \tag{3.21}$$

for the left hand side of equation (3.15) and

$$\begin{aligned}
 \overline{y(t)x_i(t - \tau_1)} &= Bf \int_0^{\frac{1}{T}} e^{A+B \sin(2\pi ft)} \sin(2\pi f(t - \tau_1)) dt \\
 &= e^A Bf \cos(2\pi f\tau_1) \int_0^{\frac{1}{T}} e^{B \sin(2\pi ft)} \sin(2\pi ft) dt \\
 &\quad - e^A Bf \sin(2\pi f\tau_1) \int_0^{\frac{1}{T}} e^{B \sin(2\pi ft)} \cos(2\pi ft) dt \\
 &= \frac{e^A B}{2\pi} \cos(2\pi f\tau_1) \int_0^{2\pi} e^{B \sin(x)} \sin(x) dx \\
 &\quad - e^A Bf \int_0^{\frac{1}{T}} \frac{e^{B \sin(2\pi ft)}}{2\pi f B} d(B \sin(2\pi ft)) \\
 &= \frac{e^A B}{2\pi} \cos(2\pi f\tau_1) \int_0^{2\pi} e^{B \sin(x)} \sin(x) dx
 \end{aligned} \tag{3.22}$$

for the right hand side.

Since equations (3.21) and (3.22) must be equal, regardless the value of  $\tau_1$ , identification of the terms  $\cos(2\pi f\tau_1)$  and  $\sin(2\pi f\tau_1)$  yields the following possible solution:

$$w_{oi}(\tau_2) = \frac{e^A}{\pi B} \int_0^{2\pi} e^{B \sin(x)} \sin(x) dx \delta(\tau_2) \tag{3.23}$$

leading to a describing function

$$N_B(A, B) = \frac{e^A}{\pi B} \int_0^{2\pi} e^{B \sin(x)} \sin(x) dx \tag{3.24}$$

### Full response

Using the describing functions from equations (3.19) and (3.24), the approximated response to an input signal  $V_{in} = 1 + \sin(2\pi t)$  is now calculated as

$$\begin{aligned} V_{out} &\approx N_A(1,1) + N_B(1,1) \sin(2\pi t) \\ &= 3.44 + 3.07 \sin(2\pi t) \end{aligned} \tag{3.25}$$

This response is plotted in Fig. 3.4 together with the exact solution and the small signal approximation from section 3.2.1. The response, calculated with the describing function approximation, shows better correspondence with the exact output signal than the small signal output, illustrating the usefulness of this theory for non-linear transfer functions, despite the more complex calculation compared to the small signal linearization.

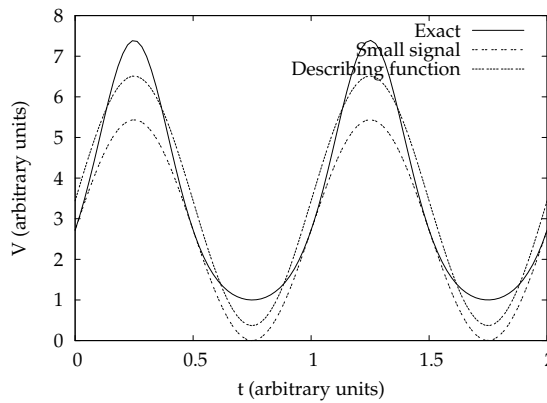


Figure 3.4: Exact, small and large signal output response

## 3.2.4 Sinusoidal input signals

### A single sinusoid

If the input signal consists of a single sinusoid, a different approach could be to rewrite the exact output as a Fourier series and consider the ratio of the amplitude of the first harmonic output component to the input amplitude as the sinusoidal-input describing function.

Considering an input signal

$$x = A \sin(2\pi ft) \tag{3.26}$$

### 3.2 Describing functions linearization

73

without offset and an odd non-linearity given by  $y(x, \dot{x})$ , the exact output can be written as

$$y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) = \sum_{n=1}^{\infty} A_n(A, f) \sin(n2\pi ft + \varphi_n(A, f)) \quad (3.27)$$

The sinusoidal-input describing function then is given by

$$\begin{aligned} N(A, f) &= \frac{\text{phasor representation of the output at frequency } f}{\text{phasor representation of the input at frequency } f} \\ &= \frac{A_1(A, f)}{A} e^{j\varphi_1(A, f)} \end{aligned} \quad (3.28)$$

As such, in the limit of a linear system, the describing function is exactly what would be considered the gain of this linear system. The main differences between linear and non-linear systems are the principle of superposition which only holds for linear systems and the fact that knowledge of the response to an infinite spectrum of sinusoids also describes the response of a linear system to every possible input while this is not the case for non-linear systems.

Further evaluation of the response from equation (3.27) and identification of the corresponding terms now leads to

$$A_1 \cos(\varphi_1) = \frac{1}{\pi} \int_0^{2\pi} y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) \sin(2\pi ft) d(2\pi ft) \quad (3.29)$$

$$A_1 \sin(\varphi_1) = \frac{1}{\pi} \int_0^{2\pi} y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) \cos(2\pi ft) d(2\pi ft) \quad (3.30)$$

for the fundamental harmonic coefficients. When using the phasor notation

$$e^{j\varphi} = \cos(\varphi) + j \sin(\varphi) \quad (3.31)$$

equations (3.29) and (3.30) can be combined to

$$\frac{A_1 e^{j\varphi_1}}{A} = \frac{j}{\pi A} \int_0^{2\pi} y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) e^{-j2\pi ft} d(2\pi ft) \quad (3.32)$$

which has the form of equation (3.28).

The only thing left to prove, is the equivalence between the Fourier series approximation from equation (3.32) and the mean-squared approximation as used in section 3.2.2. Writing the describing function as  $\rho_N e^{j\theta_N}$ , the error signal can be written as

$$\overline{e^2} = f \int_0^{\frac{1}{f}} e^2(t) dt \quad (3.33)$$

with

$$e(t) = y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) - A\rho_N \sin(2\pi ft + \theta_N) \quad (3.34)$$

The proposed solution is a least mean-squared solution if

$$\begin{cases} \frac{\partial \bar{e}^2}{\partial \rho_N} = 0 \\ \frac{\partial \bar{e}^2}{\partial \theta_N} = 0 \end{cases} \quad (3.35)$$

Evaluating these partial derivatives using equations (3.33) and (3.34), leads to

$$\rho_N = \frac{2f}{A} \int_0^{\frac{1}{f}} y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) \sin(2\pi ft + \theta_N) dt \quad (3.36)$$

$$0 = \frac{2f}{A} \int_0^{\frac{1}{f}} y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) \cos(2\pi ft + \theta_N) dt \quad (3.37)$$

which can be rewritten in complex form as

$$\rho_N e^{j\theta_N} = \frac{j}{\pi A} \int_0^{2\pi} y(A \sin(2\pi ft), A2\pi f \cos(2\pi ft)) e^{-j2\pi ft} d(2\pi ft) \quad (3.38)$$

This is identical to equation (3.32), so it can be concluded that the Fourier series expansion is a least mean-squares method and thus also leads to the describing function of the non-linearity.

### A sinusoid with other signals

It can also be shown [1] that the Fourier series expansion technique also yields valid results in the case of multiple sinusoidal inputs with an offset. This is an important result, since many analogue electronic systems are characterized using periodical input signals, that can be decomposed as a sum of sinewaves. The response can then simply be approximated using a familiar mathematical technique.

### Exponential transfer revisited

As an illustration, the response to the exponential transfer used throughout this section can be calculated again. Using the definition of the Fourier series expansion, this yields

$$a_0 = f \int_0^{\frac{1}{f}} e^{A+B \sin(2\pi ft)} dt \quad (3.39)$$

### 3.2 Describing functions linearization

75

for the DC offset term, which, again, is exactly the average of the exact response to the non-linearity, leading to the result from equation (3.19).

Calculation of the sine and cosine terms of the Fourier series is analogous:

$$a_1 = 2f \int_0^{\frac{1}{f}} e^{A+B \sin(2\pi ft)} \cos(2\pi ft) dt = 0 \quad (3.40)$$

$$b_1 = 2f \int_0^{\frac{1}{f}} e^{A+B \sin(2\pi ft)} \sin(2\pi ft) dt \quad (3.41)$$

This in turn directly leads to equation (3.24), illustrating the equivalence of both methods.

#### 3.2.5 Limit cycle calculation

When using a linear system in a closed loop configuration, the Nyquist criterion serves to determine the stability. Calculation of the closed loop transfer, using the notations from Fig. 3.5, leads to

$$\frac{V_{out}}{V_{in}} = \frac{F(s)}{1 + F(s)G(s)} \quad (3.42)$$

Stability of the system imposes the requirement that only complex roots in the left half plane exist for the denominator:

$$1 + F(s)G(s) = 0 \Rightarrow \Re(s) < 0 \quad (3.43)$$

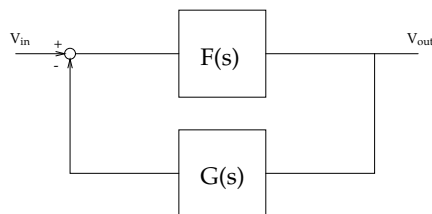


Figure 3.5: Block diagram of a closed loop system

If a non-linearity exists in this loop, the Nyquist criterion can still be applied by replacing the non-linearity by a suitable describing function. However, three conditions must be fulfilled to obtain accurate results:

1. The non-linearity is time-invariant

2. The non-linear output is filtered, such that only a limited spectral content is fed back
3. A sinusoidal input to the non-linearity will not generate subharmonics in its output

In practice, the second condition will lead to the approximation of the input signal of the non-linearity by a sinewave.

If evaluation of the Nyquist criterion on the linearized system leads to a solution with at least one pole in the right half plane, the system will exhibit oscillatory behaviour, called *limit cycling*. For the asynchronous oscillating amplifier, this is exactly what is needed, thus the requirement for oscillation is exactly equation (3.43) using the conventions from Fig. 3.5, where  $F(s)$  is to be replaced by the combination of a linear transfer function and the describing function of the non-linearity in the loop and  $s$  is replaced by  $j\omega$  with  $\omega$  the oscillating frequency.

A more extensive description of this phenomenon can be found in [1].

### 3.3 Distortion calculation

When it comes to calculating the distortion of a limit cycling system, the properties of the non-linearity must be taken into account. This, of course, will slightly complicate the mathematics. Using the generalized block diagram from Fig. 3.6 and assuming an ideal comparator with transfer function

$$E(t) = \text{signum}(e(t)) = \begin{cases} -1 & e(t) < 0 \\ 1 & e(t) \geq 0 \end{cases} \quad (3.44)$$

the linearity can now be analyzed for a loop of arbitrary order. For practical reasons, the following discussion will be limited to zeroth, first, second and third order loops.

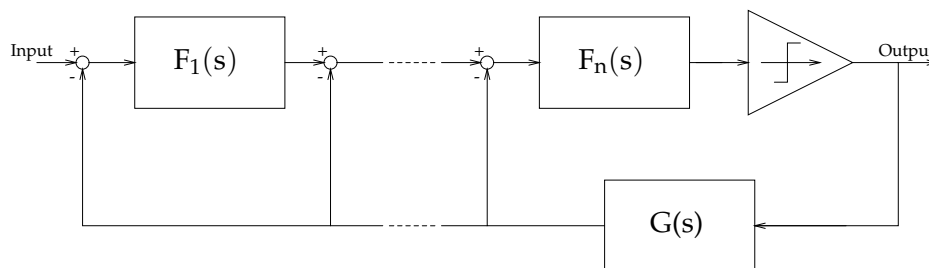


Figure 3.6: Generalized block diagram of a closed loop system

### 3.3 Distortion calculation

#### 3.3.1 Zeroth and first order loop

From a block level point of view, the zeroth and first order loops are equivalent, since the only difference is the exact implementation of the blocks. The mathematical derivation will thus hold for both cases up to the point where the transfer functions are chosen. The numerical evaluation however is done only for the first order loop, since it is expected to yield better performance.

The basis of the entire analysis is the time domain description of the system in Fig. 3.6, where  $n = 1$ :

$$\begin{cases} v(t) &= v_m \cos(\mu t) \\ e(t) &= v(t) * f_1(t) - \text{signum}(e(t)) * f_1(t) * g(t) \end{cases} \quad (3.45)$$

where  $v(t)$  is the input signal with amplitude  $v_m$  and pulsation  $\mu = 2\pi f$ ,  $e(t)$  is the error signal at the comparator input,  $f_1(t)$  and  $g(t)$  are the impulse response of  $F_1(s)$  and  $G(s)$  respectively and "\*" denotes a convolution. If  $\text{signum}(e(t))$  is written as a Fourier series, with duty cycle  $DC$  and oscillating pulsation  $\omega_k$ , this finally yields [2]

$$\begin{aligned} &v_k F_1(\mu) - (2DC - 1)F_1(\mu)G(\mu) \\ &= \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2\pi n DC)}{n} \Re(F_1(n\omega_k)G(n\omega_k)) \end{aligned} \quad (3.46)$$

The subscript  $k$  is used to indicate the value of the parameter during a single period of oscillation. Due to the asynchronous behaviour of the amplifier, a change in the input signal will also alter the oscillating frequency in addition to the duty cycle. For a sinusoidal input, this means a constantly changing period, where subscript  $k$  is used to attract attention to this fact. However, it can be shown [2] that the final results are still valid under following assumptions:

1. A monotonic phase behaviour during each period of the oscillator
2. The in-band signal frequency must be sufficiently lower than the oscillating frequency

The relation between oscillating frequency with a sinusoidal input  $f_k$  and the limit cycle  $f_0$  is given by [2]

$$f_k = \left(1 - \frac{v_k^2}{2}\right) f_0 \quad (3.47)$$

Since it can also be proven [2] that in the ideal case

$$DC = \frac{v_k + 1}{2} \quad (3.48)$$

it is obvious that the infinite sum on the right-hand side of equation (3.46) describes the distortion. Further simplification of this sum requires knowledge of the order of the transfer functions.

This does not refrain us however from making some qualitative observations regarding the eventual form of the required transfer functions  $F_1(s)$  and  $G(s)$ . Minimizing the right-hand side of equation (3.46) can be achieved by choosing  $F_1(s)G(s)$  a low pass filter at oscillating frequency and higher. Comparing the left-hand side of equation (3.46) with the ideal transfer from equation (3.48) leads to the conclusion that  $F_1(s)$  can be chosen freely at signal frequency, while  $G(s)$  should be constant over the frequency range of interest and close to unity to map the entire input voltage range onto the duty cycle space.

Additionally, equation (3.46) also suggests an interesting class of candidates for  $F_1(s)$ . Since the system under consideration is not a classical PWM, comparing input signal with a fixed clock reference to determine duty cycle, but has to regulate both duty cycle and oscillating frequency asynchronously in the loop, small deviations of the duty cycle from its ideal value can be detected more easily by *amplifying* their values before comparison.

This finally leads to the conclusion that  $F_1(s)$  should amplify at the signal band and suppress high frequency out of band signals and  $G(s)$  should be a low pass filter. An appropriate choice for  $F_1(s)$  thus could be an integrator, as used in the first order system from section 2.4.

The analysis of the distortion can now be completed for the first order system by assuming following transfer functions for  $F_1(s)$  and  $G(s)$ :

$$\begin{aligned} F_1(s) &= \frac{1}{s\tau_{f_1}} \\ G(s) &= \frac{1}{(1 + s\tau_g)^2} \end{aligned} \quad (3.49)$$

Taking into account the approximation

$$\Re(F_1(n\omega_k)G(n\omega_k)) \approx \frac{\Re(F_1(\omega_k)G(\omega_k))}{n^4} \quad (3.50)$$

the right-hand side of equation (3.46) can now further be evaluated:

$$\begin{aligned} \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2\pi nDC)}{n} \Re(F_1(n\omega_k)G(n\omega_k)) &\approx \frac{2}{\pi} \Re(F_1(\omega_k)G(\omega_k)) \sum_{n=1}^{\infty} \frac{\sin(2\pi nDC)}{n^5} \\ &= \frac{2}{\pi} \Re(F_1(\omega_k)G(\omega_k)) \frac{-(2\pi)^5}{240} B_5(DC) \end{aligned} \quad (3.51)$$



### 3.3 Distortion calculation

**Table 3.1:** Bernoulli numbers

Number	Value
$B_1$	$\frac{1}{6}$
$B_2$	$\frac{1}{30}$
$B_3$	$\frac{1}{42}$
$B_4$	$\frac{1}{30}$
$B_5$	$\frac{5}{66}$
$B_6$	$\frac{691}{2730}$
$B_7$	$\frac{7}{6}$

The last step uses the equality [3]

$$\sum_{m=1}^{\infty} \frac{\sin(m\theta)}{m^{2n+1}} = \frac{(-1)^{n+1}(2\pi)^{2n+1}}{2(2n+1)!} B_{2n+1} \left( \frac{\theta}{2\pi} \right) \quad (3.52)$$

with  $n = 0, 1, 2, \dots$ ;  $0 \leq \theta \leq 2\pi$  and where  $B_n(x)$  is a Bernoulli polynomial, given by

$$B_n(x) = x^n - \frac{1}{2}nx^{n-1} + \sum_{m=1}^{\lfloor \frac{1}{2}n \rfloor} \binom{n}{2m} B_m x^{n-2m} \quad (3.53)$$

The Bernoulli numbers  $B_k$  are then calculated as

$$B_k = (-1)^{k+1} B_{2k}(1) = (-1)^{k+1} B_{2k}(0) = \frac{2(2k)!}{(2\pi)^{2k}} \sum_{m=1}^{\infty} \frac{1}{m^{2k}} \quad (3.54)$$

A list of relevant Bernoulli numbers is given in table 3.1

After replacing the duty cycle  $DC$  by its ideal value from equation (3.48), this leads to

$$\begin{aligned} & V F_1(\mu) - (2DC - 1)F_1(\mu)G(\mu) \\ &= -\frac{4\pi^4}{15} \Re(F_1(\omega_k)G(\omega_k)) \left( \frac{V^5}{32} - \frac{5V^3}{48} + \frac{23V}{96} + \frac{1}{6} \right) \end{aligned} \quad (3.55)$$

where the instantaneous amplitude  $v_k$  is replaced by the frequency domain representation  $V$  of the input signal  $v(t)$ .

Since  $2DC - 1$  can be considered the low pass filtered output voltage  $V_{out}$ , the last equation (3.55) can be rewritten as

$$\begin{aligned}
 V_{out} = & \frac{2\pi^4 \Re(F_1(\omega_k)G(\omega_k))}{45F_1(\mu)G(\mu)} \\
 & + \frac{360F_1(\mu) + 23\pi^4 \Re(F_1(\omega_k)G(\omega_k))}{360F_1(\mu)G(\mu)} V \\
 & - \frac{\pi^4 \Re(F_1(\omega_k)G(\omega_k))}{36F_1(\mu)G(\mu)} V^3 \\
 & + \frac{\pi^4 \Re(F_1(\omega_k)G(\omega_k))}{120F_1(\mu)G(\mu)} V^5
 \end{aligned} \tag{3.56}$$

After substituting

$$V = v_m \cos(\mu t) \tag{3.57}$$

into equation (3.56) and expanding the powers of the cosine function, this finally leads to the amplitudes of the components at fundamental frequency and odd multiples thereof. The third order harmonic distortion then simply is

$$HD_3 = \frac{5\pi^4 \Re(F_1(\omega_k)G(\omega_k))v_m^2(3v_m^2 - 8)}{5760F_1(\mu) + 2\pi^4 \Re(F_1(\omega_k)G(\omega_k))(15v_m^4 - 60v_m^2 + 184)} \tag{3.58}$$

This confirms the qualitative observations made on page 78, namely a large  $F_1(\mu)$  and small  $F_1(\omega_k)G(\omega_k)$  minimize the distortion. Also note that equation (3.58) does not depend on the *exact* transfer functions  $F_1(s)$  and  $G(s)$ , but only on the *order of their real part*. It is also obvious that this derivation can be repeated for any exotic transfer function, which, again, should lead to this very conclusion.

### 3.3.2 Second order loop

For the second order loop, the analysis is completely equivalent. In this case,  $n = 2$ , leading to a loop transfer

$$e(t) = ((v(t) - \text{signum}(e(t)) * g(t)) * f_1(t)) * f_2(t) - \text{signum}(e(t)) * g(t) * f_2(t) \tag{3.59}$$

By defining

$$\begin{cases} a(t) = f_1(t) * f_2(t) \\ b(t) = g(t) * f_1(t) * f_2(t) + g(t) * f_2(t) \end{cases} \tag{3.60}$$

equation (3.59) can be written as

$$e(t) = v(t) * a(t) - \text{signum}(e(t)) * b(t) \tag{3.61}$$

### 3.3 Distortion calculation

81

which is equivalent to equation (3.45). By choosing

$$\begin{aligned} F_1(s) &= \frac{1}{s\tau_{f_1}} \\ F_2(s) &= \frac{1}{s\tau_{f_2}} \\ G(s) &= \frac{1}{(1 + s\tau_g)^2} \end{aligned} \quad (3.62)$$

the calculation of third order harmonic distortion is completely analogous to the first order case, since again  $\Re(B(n\omega_k)) \sim \frac{1}{n^4}$ . The final expression is given by

$$HD_3 = \frac{5\pi^4 \Re(B(\omega_k)) v_m^2 (3v_m^2 - 8)}{5760A(\mu) + 2\pi^4 \Re(B(\omega_k)) (15v_m^4 - 60v_m^2 + 184)} \quad (3.63)$$

with  $A(\mu)$  and  $B(\omega_k)$  the Laplace transform of equation (3.60) evaluated at their respective frequencies.

Equation (3.63) turns out to be similar to equation (3.58). However a suitable choice of the time constants in the transfer functions in equation (3.62) will lead to lower distortion levels, due to the higher value of  $A(\mu)$  compared to  $F_1(\mu)$  and the lower value of  $\Re(B(\omega_k))$  with respect to  $\Re(F_1(\omega_k)G(\omega_k))$ .

#### 3.3.3 Third order loop

For the third order loop,  $n = 3$ , the transfer function can also be written as equation (3.61), where

$$\begin{cases} a(t) = f_1(t) * f_2(t) * f_3(t) \\ b(t) = g(t) * f_1(t) * f_2(t) * f_3(t) + g(t) * f_2(t) * f_3(t) + g(t) * f_3(t) \end{cases} \quad (3.64)$$

After choosing the transfer functions as in equation (3.62)

$$\begin{aligned} F_1(s) &= \frac{1}{s\tau_{f_1}} \\ F_2(s) &= \frac{1}{s\tau_{f_2}} \\ F_3(s) &= \frac{1}{s\tau_{f_3}} \\ G(s) &= \frac{1}{(1 + s\tau_g)^2} \end{aligned} \quad (3.65)$$

this yields following expression for the third order harmonic:

$$HD_3 = \frac{7\pi^6 \Re(B(\omega_k)) v_m^2 (9v_m^4 - 60v_m^2 + 368)}{-967680A(\mu) + \pi^6 \Re(B(\omega_k)) C(v_m)} \quad (3.66)$$

where

$$C(v_m) = 105v_m^6 - 840v_m^4 + 7728v_m^2 + 19520 \quad (3.67)$$

In this case sixth order terms appear since  $\Re(B(n\omega_k)) \sim \frac{1}{n^6}$  for the transfer functions chosen.

When comparing equations (3.66) and (3.63), it is immediately clear that the scaling factor of  $A(\mu)$  is drastically increased. This, combined with a significant increase of the out of band suppression  $B(\omega_k)$ , leads to the conclusion that increasing the loop order is advantageous for the system linearity.

This also once more confirms the validity of the qualitative observations made on page 78.

### 3.4 Numerical verification

For all calculations made in this section, the non-linearity is supposed to be an ideal comparator with symmetric saturation levels  $\pm D$ . Using the describing function theory from section 3.2, the corresponding transfer function is found to be

$$N(A, \omega) = \frac{4D}{\pi A} \quad (3.68)$$

This describing function  $N(A, \omega)$  only depends on the input amplitude  $A$  relative to the saturation level  $D$  and is independent of the phase of the input sinewave.

#### 3.4.1 First order loop

##### Oscillating frequency

For a first order loop, using the transfer functions from equation (3.49) and an ideal comparator, the oscillating frequency can be calculated by evaluating equation (3.43)

$$1 + F_1(j\omega)G(j\omega)N(A, \omega) = 0 \quad (3.69)$$

leading to

$$2\omega^2 \tau_{f_1} \tau_g = N(A, \omega) \quad (3.70)$$

$$\omega \tau_{f_1} (1 - \omega^2 \tau_g^2) = 0 \quad (3.71)$$

### 3.4 Numerical verification

83

since  $N(A, \omega)$  is real and independent of frequency. Equation (3.71) now yields the oscillating frequency

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\tau_g} \quad (3.72)$$

while equation (3.70) then leads to the amplitude  $A$  of the limit cycle component at the comparator input.

When choosing an oscillating frequency of 6MHz, corresponding to the system from section 2.4, this immediately leads to

$$\tau_g = \frac{1}{2\pi \cdot 6 \cdot 10^6 \text{Hz}} \quad (3.73)$$

#### Third order harmonic distortion

Evaluation of equation (3.58) using the transfer functions from equation (3.49) leads to

$$HD_3 = \frac{10\pi^4 \tau_g v_m^2 (3v_m^2 - 8)}{\left( (1 - \omega_k^2 \tau_g^2)^2 + 4\omega_k^2 \tau_g^2 \right) \left( \frac{5760j}{\mu} + \frac{4\pi^4 \tau_g (15v_m^4 - 60v_m^2 + 184)}{(1 - \omega_k^2 \tau_g^2)^2 + 4\omega_k^2 \tau_g^2} \right)} \quad (3.74)$$

This equation only depends on the parameter  $\tau_g$ , which already has been chosen. Taking into account the considerations regarding the integrator time constants, a suitable choice would be a value between the maximum signal frequency and the oscillating frequency. A possible value for  $\tau_{f1}$  then would be

$$\tau_{f1} = \frac{1}{20 \cdot 10^6 \text{Hz}} \approx \frac{1}{2\pi \cdot 3.2 \cdot 10^6 \text{Hz}} \quad (3.75)$$

since ADSL2 contains tones up to 1.104MHz.

The resulting distortion for the values chosen in equations (3.73) and (3.75) is shown in Fig. 3.7 for a fixed oscillating frequency and in Fig. 3.8 for an oscillating frequency compensated according to equation (3.47).

In general, there is a tendency of decreasing linearity with increasing input amplitude  $v_m$  and signal frequency  $f$ . The main difference between both results, is the increased distortion level at higher values of  $v_m$  for the compensated oscillating frequency. This is to be expected, since higher input amplitudes lead to a lower oscillating frequency, which in turn further impairs the distortion levels.

#### Simulation

Block level simulations in Matlab Simulink, using the time constants from equations (3.73) and (3.75) lead to a limit cycle of 5810662.5Hz, close to the calculated

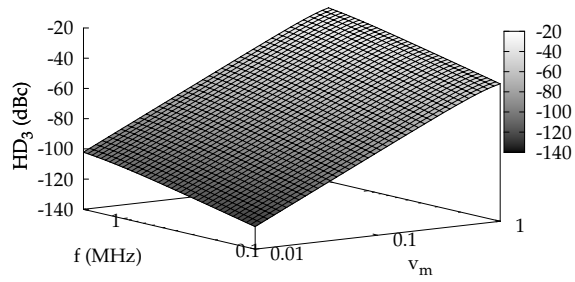


Figure 3.7: HD<sub>3</sub> as function of  $v_m$  and  $f$ , 6MHz first order loop, fixed  $f_0$

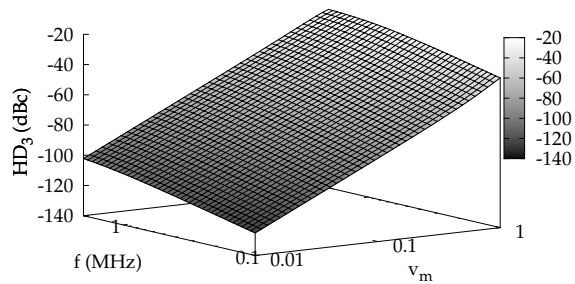


Figure 3.8: HD<sub>3</sub> as function of  $v_m$  and  $f$ , 6MHz first order loop,  $v_m$  compensated  $f_0$

### 3.4 Numerical verification

6MHz.

For the simulation of the third order harmonic distortion, an ideal comparator with saturation levels -1 and 1 is chosen. Figures 3.9, 3.10 and 3.11 show the simulated results for values of  $v_m$  between 0.1 and 1 and signal frequencies of 200kHz, 500kHz and 1MHz respectively, together with the calculated values according to equation (3.74), with and without compensation for the oscillation frequency.

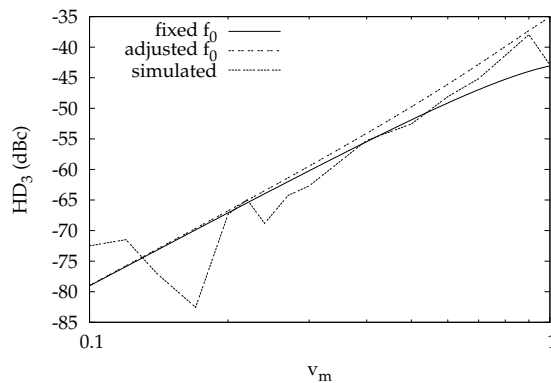


Figure 3.9: Comparison of calculated and simulated  $HD_3$ , first order loop, 200kHz signal

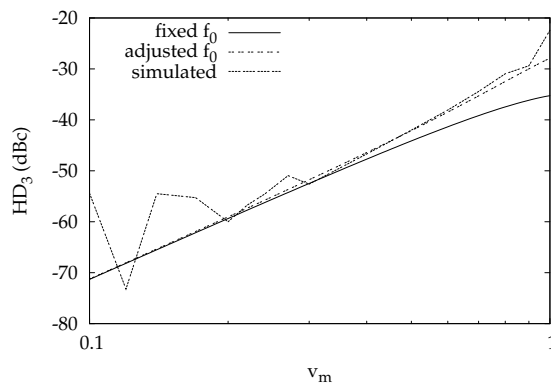


Figure 3.10: Comparison of calculated and simulated  $HD_3$ , first order loop, 500kHz signal

In general, the model gives a quite accurate prediction of the linearity, given the approximations made throughout its derivation. The most notable and consistent deviation from the model is for low values of  $v_m$ , due to the low power of the fundamental harmonic compared to the noise floor of the spectrum, which

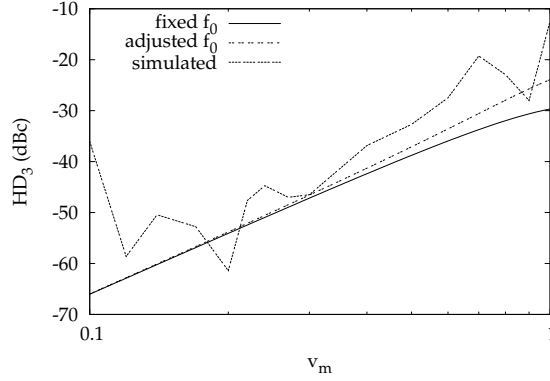


Figure 3.11: Comparison of calculated and simulated HD<sub>3</sub>, first order loop, 1MHz signal

merely is a limitation imposed by simulation accuracy.

For a signal frequency of 1MHz, there also is worse correspondence between model and simulation, in this case due to the higher signal to oscillating frequency ratio as required by condition 2 on page 77.

These simulations again confirm the tendency of lower linearity with increasing signal amplitude or frequency.

### 3.4.2 10MHz second order loop

#### Oscillating frequency

For the second order loop, the limit cycle frequency is calculated in analogy to the first order system:

$$1 + F_2(j\omega)G(j\omega)N(A, \omega)(1 + F_1(j\omega)) = 0 \quad (3.76)$$

which, for the functions chosen in equation (3.62) leads to

$$\omega^6 \tau_{f_1} \tau_{f_2} \tau_g^4 + 2\omega^4 \tau_{f_1} \tau_{f_2} \tau_g^2 + \omega^2 (\tau_{f_1} \tau_{f_2} + N(A, \omega) \tau_g^2 - 2N(A, \omega) \tau_{f_1} \tau_g) = N(A, \omega) \quad (3.77)$$

$$N(A, \omega) \omega^3 \tau_{f_1} \tau_g^2 + N(A, \omega) \omega (2\tau_g - \tau_{f_1}) = 0 \quad (3.78)$$

Equation (3.78) immediately evaluates to

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2} \frac{\sqrt{\tau_{f_1} (\tau_{f_1} - 2\tau_g)}}{\pi \tau_{f_1} \tau_g} \quad (3.79)$$

and equation (3.77) subsequently yields the limit cycle amplitude  $A$ .



### 3.4 Numerical verification

87

Since the limit cycle frequency now depends on two parameters  $\tau_{f_1}$  and  $\tau_g$ , the third order harmonic distortion should be calculated first to allow for an optimal choice of all system parameters.

#### Third order harmonic distortion

The third order harmonic distortion is calculated from equation (3.63), using the definition from equation (3.60) and the functions from equation (3.62):

$$HD_3 = \frac{5}{2} \frac{\pi^6 \tau_{f_1}^2 \tau_g v_m^2 (3v_m^2 - 8) f^2}{-2880\tau_g + 1440\tau_{f_1} + 15\pi^6 \tau_{f_1}^2 \tau_g v_m^4 f^2 - 60\pi^6 \tau_{f_1}^2 \tau_g v_m^2 f^2 + 184\pi^6 \tau_{f_1}^2 \tau_g f^2} \quad (3.80)$$

This result, again, is independent of the time constant of the integrator just before the comparator. In contrast to the first order loop, where both distortion and limit cycle frequency are completely defined by the single parameter  $\tau_g$ , there now are two parameters  $\tau_g$  and  $\tau_{f_1}$  to optimize both.

Also note that the oscillating frequency  $\omega_k$ , as occurring in equation (3.63), is not compensated for signal amplitude according to equation (3.47), to reduce complexity. This is an acceptable approach, since ADSL has a low root mean square amplitude and significant deviation between distortion with fixed and compensated oscillating frequency requires a sufficiently large input.

The denominator can now be written as

$$-2880\tau_g + 1440\tau_{f_1} + \pi^6 \tau_{f_1}^2 \tau_g f^2 (15v_m^4 - 60v_m^2 + 184) \quad (3.81)$$

where the terms depending on frequency  $f$  and amplitude  $v_m$  are *always positive*. The formula for the limit cycle in equation (3.79) also leads to the requirement

$$\tau_{f_1} > 2\tau_g \quad (3.82)$$

which suggests a maximal value for  $\tau_{f_1}$  and a minimal value for  $\tau_g$  will be optimal for determining the limit cycle frequency mainly by the parameters of the feedback components. However, both values are depending on each other through the chosen value of the limit cycle frequency  $f_0$ :

$$\tau_g = \frac{\sqrt{1 + \omega_0^2 \tau_{f_1}^2} - 1}{\omega_0^2 \tau_{f_1}} \quad (3.83)$$

As a result, an increase of the time constant  $\tau_{f_1}$  will imply a sublinear increase of  $\tau_g$ , thus a maximum  $\tau_{f_1}$  will be optimal.

An additional constraint on the value of  $\tau_{f_1}$  is the signal bandwidth. Given the requirements on page 78 and a design limit cycle frequency of 10MHz, following

will be a suitable choice:

$$\tau_{f_1} = \frac{1}{10 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 1.6 \cdot 10^6 \text{ Hz}} \quad (3.84)$$

$$\tau_{f_2} = \frac{1}{20 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 3.2 \cdot 10^6 \text{ Hz}} \quad (3.85)$$

$$\tau_g = 0.0000000134 \text{ s} \approx \frac{1}{2\pi \cdot 11.88 \cdot 10^6 \text{ Hz}} \quad (3.86)$$

Figures 3.12 and 3.13 depict the distortion as a function of signal amplitude  $v_m$  and frequency  $f$  for a fixed and compensated oscillating frequency, showing similar behaviour as with the first order loop, but with a reduced distortion level.

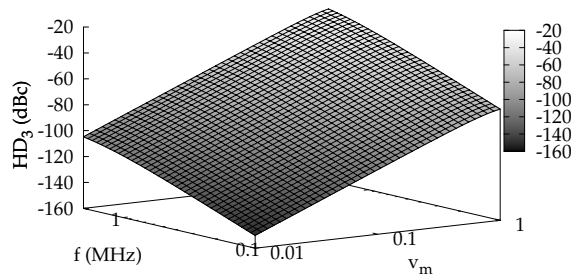


Figure 3.12:  $HD_3$  as function of  $v_m$  and  $f$ , 10MHz second order loop, fixed  $f_0$

### Simulation

The simulated oscillating frequency now is 9600056.2Hz, or again slightly below the calculated frequency of 10MHz.

The results of the third order harmonic distortion simulations are given in Fig. 3.14, 3.15 and 3.16, again for a 200kHz, 500kHz and 1MHz sinewave respectively. The simulated values correspond closely to the values calculated using equation (3.80), also for the 1MHz input signal as opposed to the first order loop. This is mainly due to the higher limit cycle frequency, causing better compliance to condition 2 on page 77.

For low values of  $v_m$ , the same explanation as for the first order loop in section 3.4.1 still holds.

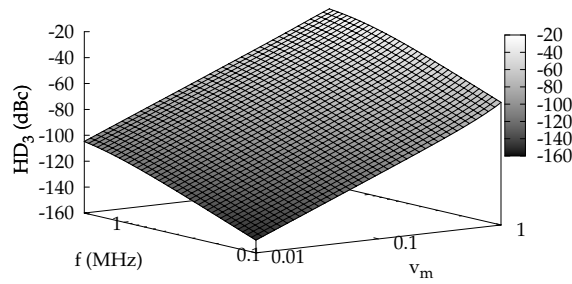


Figure 3.13: HD<sub>3</sub> as function of  $v_m$  and  $f$ , 10MHz second order loop,  $v_m$  compensated  $f_0$

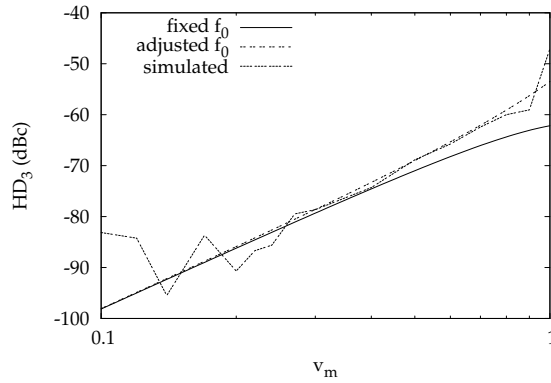


Figure 3.14: Comparison of calculated and simulated HD<sub>3</sub>, 10MHz second order loop, 200kHz signal

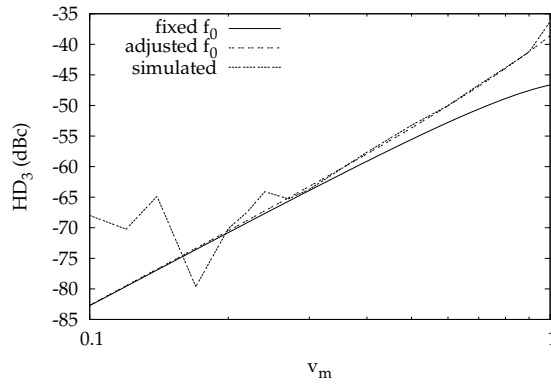


Figure 3.15: Comparison of calculated and simulated  $HD_3$ , 10MHz second order loop, 500kHz signal

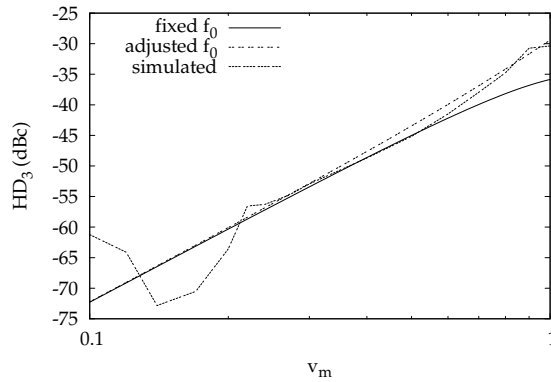


Figure 3.16: Comparison of calculated and simulated  $HD_3$ , 10MHz second order loop, 1MHz signal

### 3.4 Numerical verification

#### 3.4.3 30MHz second order loop

The discussion of this case is completely analogous to section 3.4.2, so only the results are given for reference.

The values of  $\tau_{f_1}$  and  $\tau_{f_2}$  remain identical, while  $\tau_g$  is decreased to obtain the 30MHz oscillating frequency:

$$\tau_{f_1} = \frac{1}{10 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 1.6 \cdot 10^6 \text{ Hz}} \quad (3.87)$$

$$\tau_{f_2} = \frac{1}{20 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 3.2 \cdot 10^6 \text{ Hz}} \quad (3.88)$$

$$\tau_g = \frac{1}{200 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 32 \cdot 10^6 \text{ Hz}} \quad (3.89)$$

The curves showing distortion as a function of signal amplitude  $v_m$  and frequency  $f$  for a fixed and compensated oscillating frequency are given in Fig. 3.17 and 3.18.

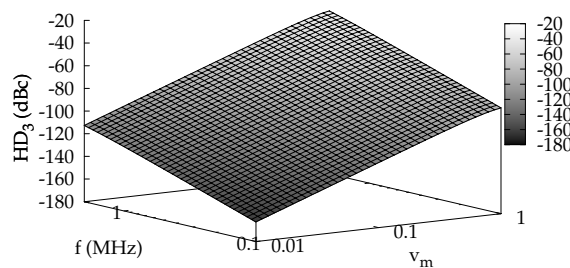


Figure 3.17:  $HD_3$  as function of  $v_m$  and  $f$ , 30MHz second order loop, fixed  $f_0$

Figures 3.19, 3.20 and 3.21 give a comparison between simulated and calculated values, again at 200kHz, 500kHz and 1MHz signal frequencies. The simulation corresponds rather well to the calculated values, except for low amplitudes of  $v_m$  due to noise floor limitations and amplitudes in excess of 80% of the full scale amplitude, caused by the subsequent approximations and assumptions regarding duty cycle, input and output amplitude. The simulated oscillating frequency in this case is 27.6MHz.

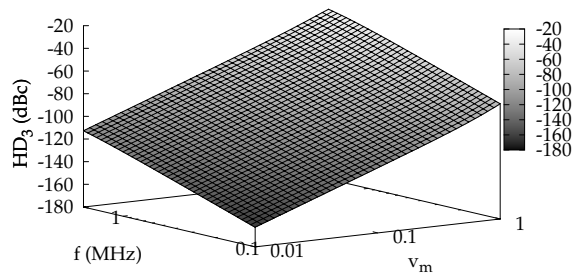


Figure 3.18: HD<sub>3</sub> as function of  $v_m$  and  $f$ , 30MHz second order loop,  $v_m$  compensated  $f_0$

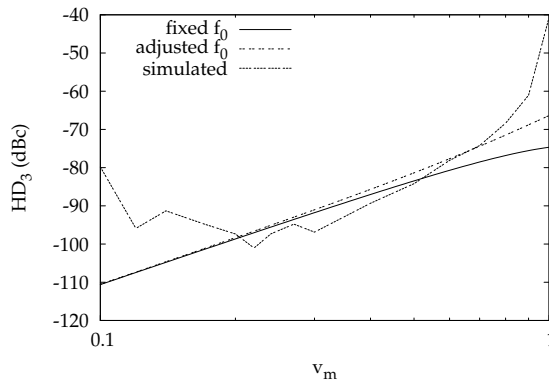


Figure 3.19: Comparison of calculated and simulated HD<sub>3</sub>, 30MHz second order loop, 200kHz signal

3.4 Numerical verification

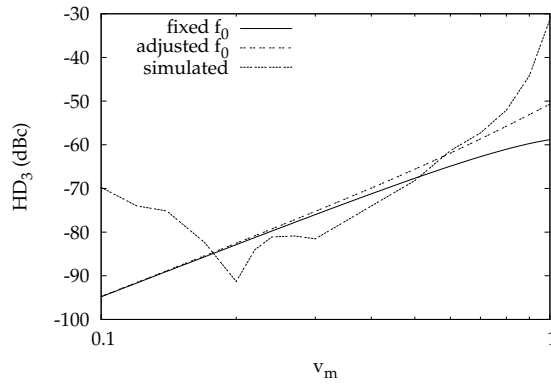


Figure 3.20: Comparison of calculated and simulated HD<sub>3</sub>, 30MHz second order loop, 500kHz signal

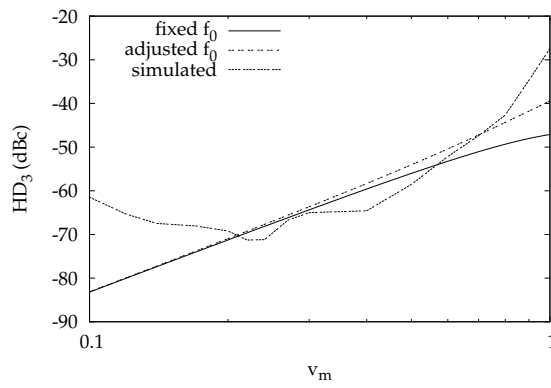


Figure 3.21: Comparison of calculated and simulated HD<sub>3</sub>, 30MHz second order loop, 1MHz signal

### 3.4.4 Third order loop

#### Oscillating frequency

The basic equation to determine the limit cycle frequency of the third order system is

$$1 + F_3(j\omega)G(j\omega)N(A, \omega)(1 + F_2(j\omega) + F_1(j\omega)F_2(j\omega)) = 0 \quad (3.90)$$

which eventually leads to

$$f_0 = \frac{\omega_0}{2\pi} = \frac{\sqrt{\tau_g^2 - 2\tau_{f_1}\tau_g + \tau_{f_1}\tau_{f_2} + \sqrt{\tau_g^4 - 4\tau_{f_1}\tau_g^3 - 2\tau_{f_1}\tau_{f_2}\tau_g^2 + 4\tau_{f_1}^2\tau_g^2 - 4\tau_{f_1}^2\tau_{f_2}\tau_g + \tau_{f_1}^2\tau_{f_2}^2}}}{2\sqrt{2}\pi\sqrt{\tau_{f_1}\tau_{f_2}\tau_g}} \quad (3.91)$$

using the system transfer functions in equation (3.65).

Evaluation of the third order harmonic distortion in the next section will provide for additional boundary conditions to determine suitable values for all time constants.

#### Third order harmonic distortion

The basic formula for the third order harmonic distortion is given in equation (3.66). The resulting functions  $A(\mu)$  and  $\Re(B(\omega_k))$  are given by

$$A(\mu) = \frac{j}{\mu^3\tau_{f_1}\tau_{f_2}\tau_{f_3}} \quad (3.92)$$

$$\Re(B(\omega_k)) = \frac{2\tau_g - \tau_{f_1} + \omega_k^2\tau_{f_1}\tau_g^2 - 2\omega_k^2\tau_{f_1}\tau_{f_2}\tau_g}{\omega_k^2\tau_{f_1}\tau_{f_2}\tau_{f_3}(1 + 2\omega_k^2\tau_g^2 + \omega_k^4\tau_g^4)} \quad (3.93)$$

Since the time constant of the last integrator in the forward path  $\tau_{f_3}$  is found directly as a factor in the denominator of both terms, the result will once more be completely independent of this time constant.

For the simplicity of further calculations, the oscillating frequency  $f_k$  again is replaced by its maximum value  $f_0$  from equation (3.91). The time constant  $\tau_g$  can now be written as

$$\tau_g = \pm \frac{\sqrt{\omega_0^2\tau_{f_1}^2 - 2\omega_0^2\tau_{f_1}\tau_{f_2} + \omega_0^4\tau_{f_1}^2\tau_{f_2}^2 + 1} - \omega_0\tau_{f_1}}{(\omega_0^2\tau_{f_1}\tau_{f_2} - 1)\omega_0} \quad (3.94)$$

based on equation (3.91).

Both equations (3.91) and (3.94) lead to the conclusion that



### 3.4 Numerical verification

95

1. The existence of a value for  $\tau_g$  requires minimum values for  $\tau_{f_1}$  and  $\tau_{f_2}$
2. The dependence of  $\tau_g$  on  $\tau_{f_1}$  and  $\tau_{f_2}$  is sublinear

These conclusions are equivalent to those for the second order system, but the exact formulæ are far more complex. As a result, similar values are chosen for the time constants  $\tau_{f_1}$ ,  $\tau_{f_2}$  and  $\tau_{f_3}$ , which are upward limited by the signal bandwidth, with a calculated value for  $\tau_g$  according to equation (3.94), leading to a limit cycle frequency of approximately 13.7MHz:

$$\tau_{f_1} = \frac{1}{10 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 1.6 \cdot 10^6 \text{ Hz}} \quad (3.95)$$

$$\tau_{f_2} = \frac{1}{20 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 3.2 \cdot 10^6 \text{ Hz}} \quad (3.96)$$

$$\tau_{f_3} = \frac{1}{20 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 3.2 \cdot 10^6 \text{ Hz}} \quad (3.97)$$

$$\tau_g = \frac{1}{109 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 17.3 \cdot 10^6 \text{ Hz}} \quad (3.98)$$

The resulting graphs for distortion as a function of  $v_m$  and  $f$  are shown in Fig. 3.22 and 3.23 for fixed and compensated oscillating frequencies respectively.

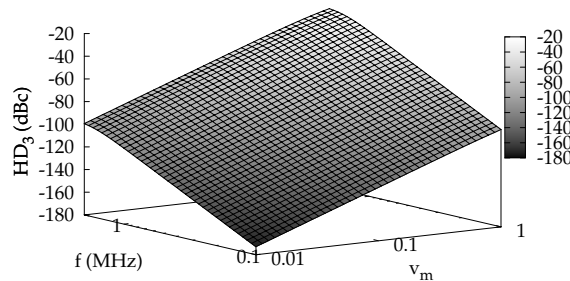


Figure 3.22: HD<sub>3</sub> as function of  $v_m$  and  $f$ , 10MHz third order loop, fixed  $f_0$

### Simulation

Finally, also simulations were performed on a third order system using the above parameters, of which the results are given in Fig. 3.24 to 3.26 for signal frequencies of 200kHz, 500kHz and 1MHz. The simulated limit cycle frequency now is 13MHz, or 5% under the calculated value of 13.7MHz.

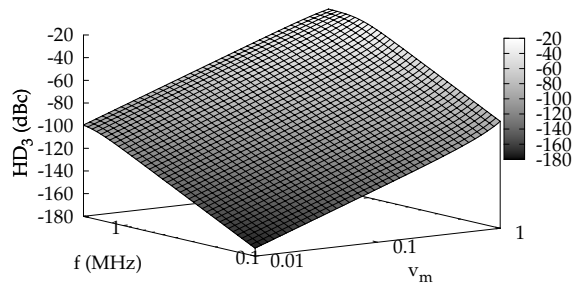


Figure 3.23: HD<sub>3</sub> as function of  $v_m$  and  $f$ , 10MHz third order loop,  $v_m$  compensated  $f_0$

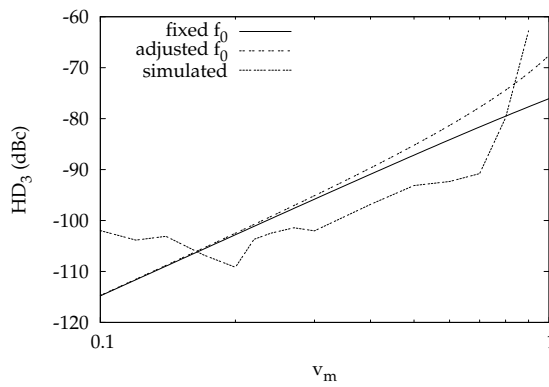


Figure 3.24: Comparison of calculated and simulated HD<sub>3</sub>, third order loop, 200kHz signal

### 3.4 Numerical verification

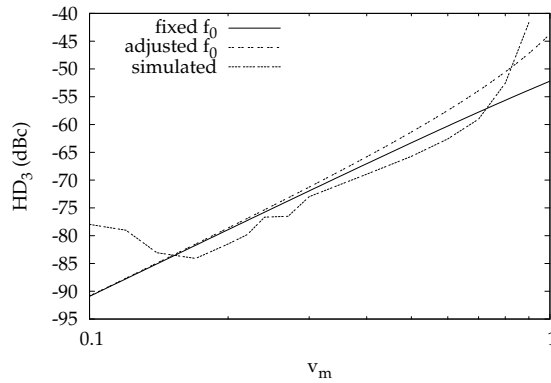


Figure 3.25: Comparison of calculated and simulated  $HD_3$ , third order loop, 500kHz signal

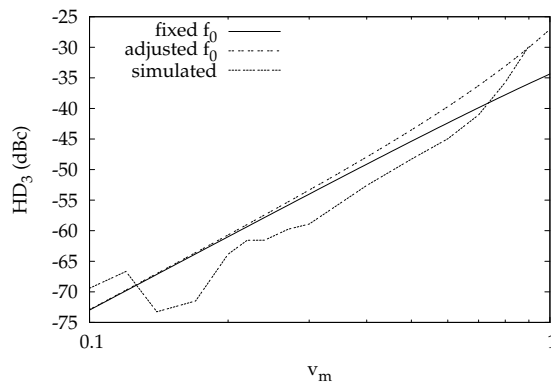


Figure 3.26: Comparison of calculated and simulated  $HD_3$ , third order loop, 1MHz signal

**Table 3.2:** Calculated and simulated limit cycle frequencies

Loop order	Calculated	Simulated	Deviation
First	6MHz	5.8MHz	3.3%
Second	10MHz	9.6MHz	4%
Second	30MHz	27.6MHz	8%
Third	13.7MHz	13MHz	5.1%

As for the previously discussed systems, there is a discrepancy at low signal amplitudes due to numeric accuracy and a slight peaking at extreme amplitudes. For the large range of values in between these extremities, the distortion never is underestimated, but overestimated by about 5dB.

### 3.4.5 Discussion

#### Limit cycle frequency

The calculated and simulated limit cycle frequencies of all four systems are given in table 3.2. All simulated values are below and within 10% of the calculated value, as was expected based on [1].

There also is a striking resemblance between the equations (3.72), (3.79) and (3.91) for the limit cycle frequency, not only because of the independence from the integrator just in front of the comparator, but also the inverse proportionality with  $\tau_g$ . Additionally, when the time constants of all integrators approach infinity, the limit cycle is equal to that of a first order system due to the apparent absence of a higher order loop.

This also provides a simple means to systematically make a first estimate of the time constant of the passive low pass filter in the loop. The integrator time constants then will be limited upwards by the frequency requirements of the input signal. This is illustrated by the values of  $\tau_g$  as chosen in equations (3.73), (3.86), (3.89) and (3.98) and their relatively small deviation from the ultimately calculated limit cycle frequency, given the rough approximation.

#### Third order harmonic distortion

Besides the good correspondence between the calculated and simulated distortion, the comparison of the distortion of all different topologies is an equally important matter. Figure 3.27 shows the calculated distortion for all four systems as a function of the signal frequency  $f$  with compensated oscillating frequency. The value for  $v_m$  is chosen the root mean square voltage of an ADSL signal. In analogy with the practical implementations from chapter 2, this means 12.6% of the comparator saturation voltage when using a symmetrical voltage supply  $\pm V_{CC}$ .

3.4 Numerical verification

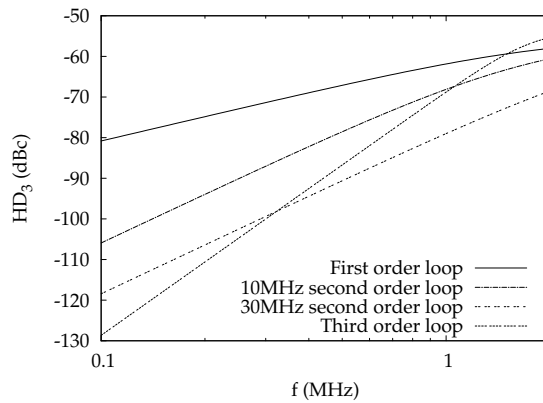


Figure 3.27: Comparison of all calculated loops, rms input voltage  $v_m = 0.126$

Figures 3.28 to 3.30 give the distortion as a function of  $v_m$  at the same signal frequencies as before, also for compensated oscillating frequency.

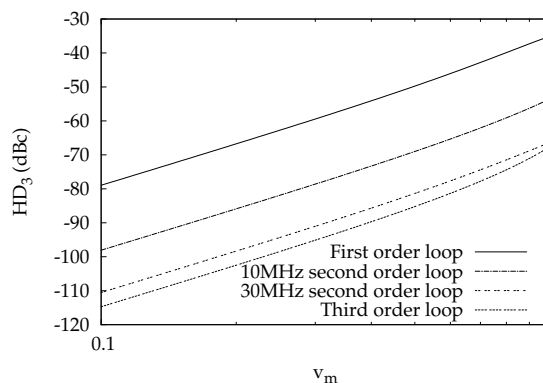


Figure 3.28: Comparison of all calculated loops, 200kHz input signal

These figures lead to the observation that both loop order and limit cycle play a significant role in the behaviour of the system. A higher order loop will lead to a lower distortion, but with comparable limit cycle frequencies, all loops will lead to similar levels of distortion at elevated signal frequencies. As a result, a sufficient ratio of limit cycle to signal frequency must be chosen, based on the maximum allowable distortion.

This over switching ratio should however remain modest, since in practical implementations this will lead to higher switching losses, which might jeopardize

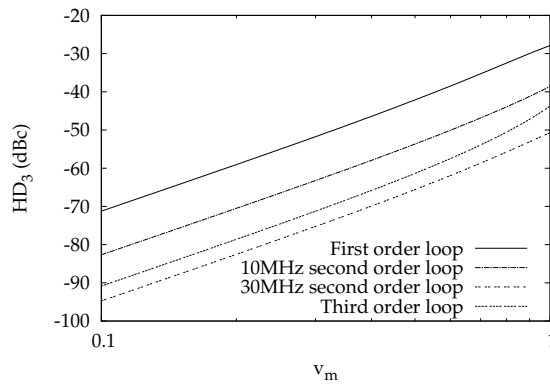


Figure 3.29: Comparison of all calculated loops, 500kHz input signal

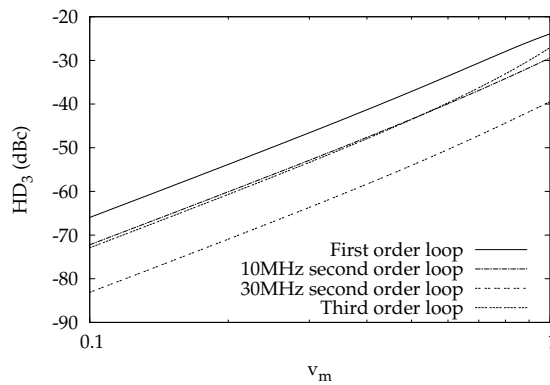


Figure 3.30: Comparison of all calculated loops, 1000kHz input signal

**Table 3.3:** Simulated MTPR

Loop order	Limit cycle	MTPR
First	6MHz	42.5dB
Second	10MHz	52dB
Second	30MHz	54dB
Third	13.7MHz	57dB

the advantage of a switching amplifier over its linear counterpart.

#### What about MTPR?

With regard to the final goal being the processing of ADSL signals, one question still remains. How does this translate into MTPR? Several numerical simulations in Matlab with MTPR test signals were performed, leading to the results from table 3.3. Note that for the first order loop the input used is an ADSL2 signal with frequencies up to 1.1MHz, while the other loops were simulated using a 2.2MHz ADSL2+ signal.

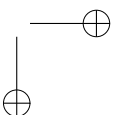
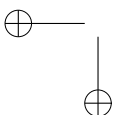
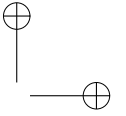
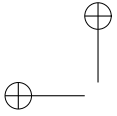
As a result, at least a 30MHz second order loop or a 10MHz third order loop will be required to reach the specification of 55dB.

### 3.5 Conclusion

A mathematical description of the system is given, to predict both the oscillating frequency and the third order harmonic distortion. This theory is verified by several numerical simulations, leading to the following observations:

1. An increase of the loop order lowers the distortion
2. A higher limit cycle also decreases distortion

With regard to MTPR, the over switching ratio should be at least 5 for a third order loop.

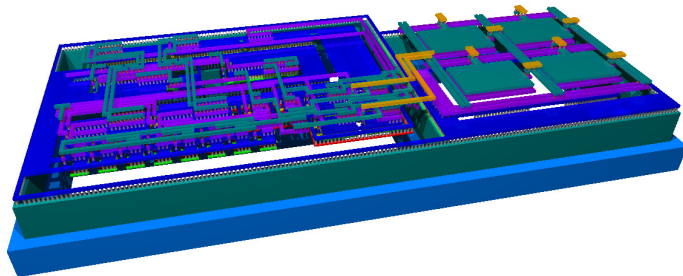




## References

- [1] A. Gelb and W. E. Vander Velde, *Multiple-input Describing Functions and Non-linear System Design*. McGraw-Hill Book Company, 1968.
- [2] E. Roza, "Analog-to-digital conversion via duty-cycle modulation," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 11, pp. 907–914, Nov. 1997.
- [3] V. Mangulis, *Handbook of Series for Scientists and Engineers*. New York: Academic Press Inc., 1965.





# 4

## Designing the loop

In this chapter, an overview is given of the different building blocks required to implement the final circuit, in accordance with the results from chapter 3. Simulation results are then presented for both the building blocks and the full asynchronous amplifier, with some additional recommendations for the final layout.

### 4.1 Introduction

The system parameters, as proposed in chapter 3, can now be used in a practical implementation, to further verify the theory and identify the potential bottlenecks for future designs. All four different loops will be implemented as a differential input, differential output amplifier, with the outputs in forced counterphase as already demonstrated in section 2.4. In addition, also a version with two independent single input, single output 10MHz loops with counterphase inputs will be tested.

The technology chosen for this design, is the AMI Semiconductor I<sup>3</sup>T80 0.35 $\mu$ m technology, offering devices with breakdown voltages of up to 80V. In addition, the transformer ratio is chosen 1:2 to further reduce the supply voltage to 25V, which also means a doubling of the rms output current to deliver the 20dBm nominal power. From a line driver point of view, the 100 $\Omega$  line impedance is transformed down to 25 $\Omega$ .

**Table 4.1:** Key characteristics of I<sup>3</sup>T80 DMOS devices [1]

Device	Type	Floating	Breakdown	R <sub>on</sub> * Area
VFNDM80	N	80V	70V	0.26Ω*mm <sup>2</sup>
VFNDM80a	N	80V	70V	0.325Ω*mm <sup>2</sup>
LFPDM80	P	80V	-70V	0.28Ω*mm <sup>2</sup>

Section 4.2 gives an overview of the most important I<sup>3</sup>T80 device parameters, which will be used in the different building blocks in section 4.3. Sections 4.4 to 4.7 give the implementation of the first, second and third order systems as dimensioned in sections 3.4.1 to 3.4.4 and section 4.8 explores the functioning of a second order system with two independent loops. The layout of these amplifiers then is discussed in section 4.9.

## 4.2 Technology overview

Analogous to the I<sup>2</sup>T100 0.7μm technology, the I<sup>3</sup>T80 0.35μm technology is a standard 3.3V, 0.35μm CMOS process with high voltage extensions, allowing for breakdown voltages of up to 80V. Again, the only components of interest are the high voltage DMOS structures, the MOS transistors, resistors and capacitors.

### 4.2.1 DMOS transistors

Of all DMOS transistors offered by the technology, only two N-type and one P-type DMOS are withheld based on supply voltage constraints, some important parameters of which are given in table 4.1. The NDMOS transistors are a digital (VFNDM80) and an analogue (VFNDM80a) variant of the same basic structure. The main difference between both is the lower on-resistance of the analogue device at identical conditions and channel width, while the digital device is more area efficient. The final choice between both candidates will be based on simulations of the output stage.

### 4.2.2 MOS transistors

For the MOS transistors, the situation is slightly different from I<sup>2</sup>T100. Again, both the "classical" low voltage mosfets and their floating counterparts exist, but this time they behave completely identical. This is caused by a particularity of the technology. Since the processing starts from a wafer with a N-type epitaxial layer on top of a P-type substrate, the devices can be isolated from one another by implanting P-type dopants around the structure, which is done automatically

## 4.2 Technology overview

107

**Table 4.2:** Key characteristics of I<sup>3</sup>T80 MOS devices [1]

Device	Type	Floating	Breakdown	V <sub>T0</sub>	I <sub>DS</sub>
NMOS	N	3.6V	3.6V	0.59V	530μA/μm
FNMOS	N	80V	3.6V	0.59V	530μA/μm
PMOS	P	3.6V	-3.6V	-0.57V	-250μA/μm
FPMOS	P	80V	-3.6V	-0.57V	-250μA/μm

**Table 4.3:** Key characteristics of I<sup>3</sup>T80 capacitors [1]

Device	Breakdown	Value
Metal 2 - metal 2.5	35V	1.5fF/μm <sup>2</sup>
Metal - poly stack	80V	<0.5fF/μm <sup>2</sup>

outside of the common boundary of a set of devices. As a result, the floating and non-floating devices are processed in an identical environment, as opposed to I<sup>2</sup>T100, where buried layers must be implanted underneath each floating device and the PMOS requires a differently doped nwell.

Table 4.2 gives an overview of their most important characteristics.

### 4.2.3 Capacitors

No implanted capacitors exist in I<sup>3</sup>T80. The two options available are a special structure using the second metal layer and an additional metal layer with a thin dielectric in between and to stack the regular polysilicon and metal layers. Both types are listed in table 4.3. The intrinsic available capacitor has the advantage of withstanding high voltage differences between the plates, but has a low capacitance per unit of area. The special capacitor has a lower breakdown voltage, which is still sufficient for the application, but a higher capacitance per unit of area, so this device is preferred.

### 4.2.4 Resistors

The recommended resistors are polysilicon based, as shown in table 4.4. Since the value of most resistors in the circuit will turn out to be rather large, the high ohmic poly will be the best choice.

Table 4.4: Key characteristics of I<sup>3</sup>T80 resistors [1]

Device	Breakdown	Value
High ohmic poly	80V	975Ω/□
Unsalicide P+ poly	80V	240Ω/□
Unsalicide N+ poly	80V	292Ω/□

### 4.3 Building blocks

This section will list the basic blocks used in the amplifiers, which, again, are opamps for the integrator and voltage follower, a comparator, a turn-on delay, level shifter and buffers, the output stage and the passive voltage divider and feedback filter.

#### 4.3.1 Opamps

Two opamps are to be designed, namely a single ended opamp to buffer the divided output signal and provide a strong signal to the integrators and a differential input, differential output opamp for the integrators.

#### Integrator

**Opamp design** For the integrator, an opamp with differential input and differential output is chosen, since for higher order loops this will lead to a cleaner and more natural circuit, as opposed to the asymmetrical circuit from Fig. 2.24. Furthermore, two design parameters should be determined in advance, namely the gain bandwidth product and the load capacitance, the first depending on the signal properties, the latter merely on the final layout.

To be on the safe side, the load capacitance is chosen

$$C_L = 1pF \tag{4.1}$$

The gain bandwidth product will also have a direct impact on the distortion of the integrator, since this is affected by the return difference or amount-of-feedback [2]. As a result, choosing the gain bandwidth product sufficiently high compared to the unity gain bandwidth of the closed loop circuit will be beneficial.

The integrator time constants in sections 3.4.1 to 3.4.4 are set at frequencies of 1.6MHz and 3.2MHz, so a gain bandwidth product of 275MHz is chosen, leading to approximately 40dB of excess opamp gain capability. This relatively high frequency and the minimum signal frequency of 138kHz finally lead to a preference for a two stage folded cascode topology, the basic schematic of which is given in Fig. 4.1.

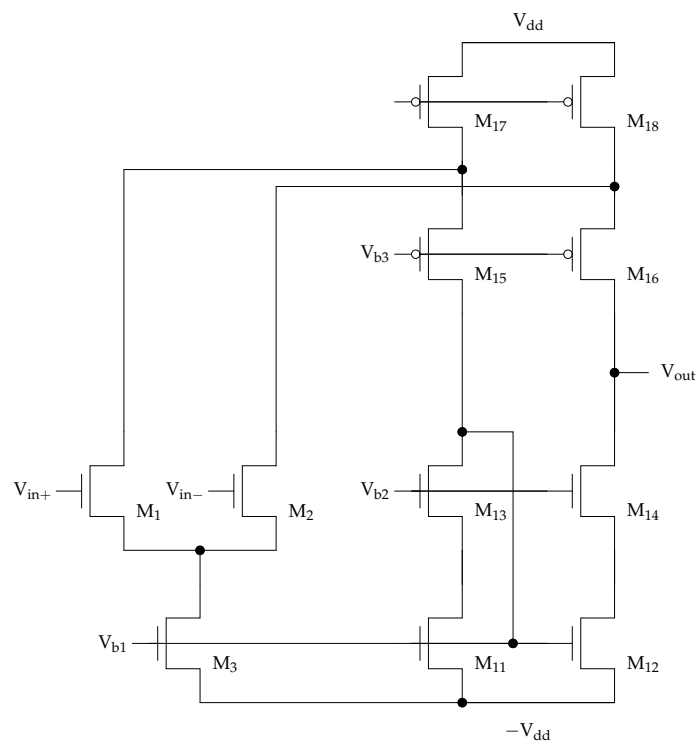


Figure 4.1: Basic schematic of a two stage folded cascode opamp

For the two stage folded cascode amplifier, the dominating pole  $f_d$  is located at the output and depends on the load resistance [3]:

$$f_d = \frac{1}{2\pi R_L C_L} \quad (4.2)$$

where  $R_L$  consists of the resistive part of the opamp load, in parallel with the output resistance of cascode transistors  $M_{14}$  and  $M_{16}$ . This also implies the maximum gain will be limited by the load.

The non-dominating pole  $f_0$  is determined by the transconductance of the input stage and the load capacitance:

$$f_0 = \frac{g_{m1}}{2\pi C_L} \quad (4.3)$$

Stability of the final design will thus require a minimum capacitive load, as opposed to the three stage designs from chapter 2.

Using a 1pF load capacitance and a 275MHz gain bandwidth product, the non-dominating pole leads to

$$g_{m1} = 2\pi f_0 C_L = 1.728 \text{ mS} \quad (4.4)$$

Using a drain current

$$I_B = 100 \mu\text{A} \quad (4.5)$$

for the input transistors  $M_1$  and  $M_2$ , this yields

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{m1}^2}{2I_B \mu_N C_{OX}} = 106 \quad (4.6)$$

Using the  $100 \mu\text{A}$  bias current and a 0.3V for  $V_{Dsat} = V_{GS} - V_T$ , the dimensioning of the cascode transistors  $M_{11}$  to  $M_{18}$  is straightforward:

$$\left(\frac{W}{L}\right)_{11-14} = \frac{2I_B}{\mu_N C_{OX} V_{Dsat}^2} = 15.75 \quad (4.7)$$

$$\left(\frac{W}{L}\right)_{15-16} = \frac{2I_B}{\mu_P C_{OX} V_{Dsat}^2} = 39.05 \quad (4.8)$$

$$\left(\frac{W}{L}\right)_{17-18} = 2 \frac{2I_B}{\mu_P C_{OX} V_{Dsat}^2} = 78.10 \quad (4.9)$$

Starting from these calculated values, the basic diagram from Fig. 4.1 can now be transformed to a differential output setup by omitting the current mirror formed by the connection between the drain of transistor  $M_{13}$  and the gates of transistors  $M_{11}$  and  $M_{12}$ .



### 4.3 Building blocks

111

This, however, means there is no direct coupling of the common mode component of both output voltages any more. Since the components in the loop should compensate for a common mode difference generated by the output stage and not the other way around, a so called long tail pair is included to compensate for a common mode difference [3][4][5]. By using the output of this long tail pair to determine the current on the folded cascode side of the opamp, the output common mode will be adjusted such that

$$V_{G21} + V_{G24} = V_{G22} + V_{G23} = 2V_{CM,out} \quad (4.10)$$

using the conventions from Fig. 4.2. This means both output signals must have the same common mode voltage  $V_{CM,out}$  as applied to the input of the long tail pair and be in counterphase.

To simplify the design, the dimensions from the folded cascode opamp are used as a reference, but to limit the current consumption, the dimensions of transistors  $M_{21}$  to  $M_{28}$  are halved, which still allows for reliable current mirroring if using multiples of the same basic transistors.

Table 4.5 gives an overview of the final optimized dimensions of all transistors.

**Table 4.5:** Final dimensions of the opamp

Device	Width	Length
$M_{1,2}$	$35.50\mu\text{m}$	$0.35\mu\text{m}$
$M_3$	$15.80\mu\text{m}$	$0.35\mu\text{m}$
$M_{11,12,13,14}$	$7.90\mu\text{m}$	$0.5\mu\text{m}$
$M_{15,16}$	$19.55\mu\text{m}$	$0.5\mu\text{m}$
$M_{17,18}$	$39.10\mu\text{m}$	$0.5\mu\text{m}$
$M_{21,22,23,24}$	$17.80\mu\text{m}$	$0.5\mu\text{m}$
$M_{25,26}$	$19.55\mu\text{m}$	$0.5\mu\text{m}$
$M_{27,28}$	$7.90\mu\text{m}$	$0.5\mu\text{m}$

The simulated Bode transfer of the opamp, with common mode output voltage 1.65V, is given in Fig. 4.3, resulting in a 339.87MHz gain bandwidth product and a 61.27° phase margin. The DC gain is 842 or 58.5dB, leading to a bandwidth of 400kHz.

**Integrator circuit** The realized integrating circuit, using the differential input, differential output amplifier is shown in Fig. 4.4. This circuit is simulated using a fixed feedback capacitance of 500fF and a resistor depending on the integrator time constant, 199kΩ for the 1.6MHz integrator and 99.5kΩ for the 3.2MHz integrator, as determined in section 3.4.

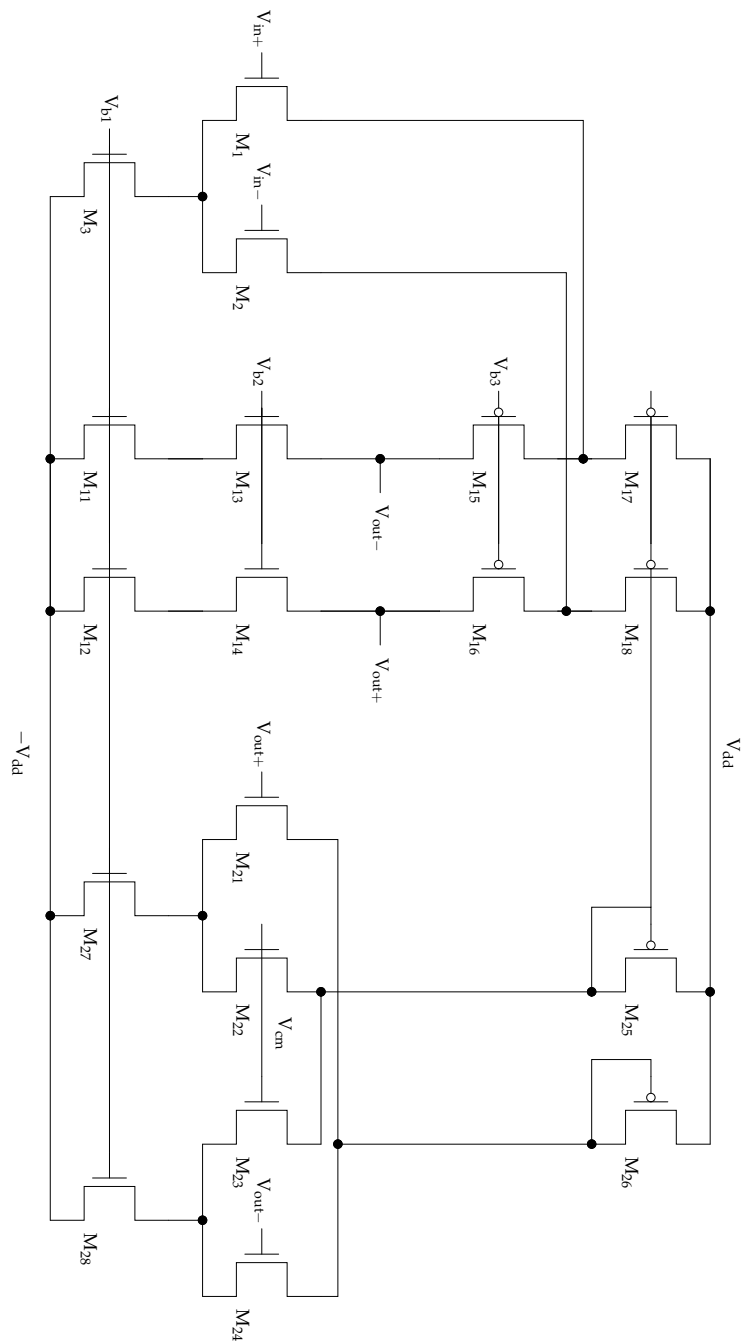


Figure 4.2: Schematic of the two stage folded cascode opamp with output common mode control

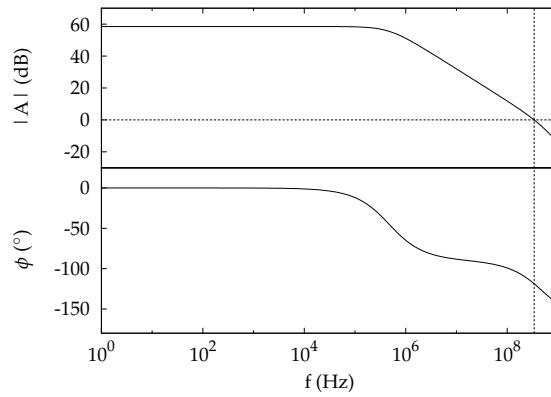


Figure 4.3: Simulated Bode diagram of the opamp

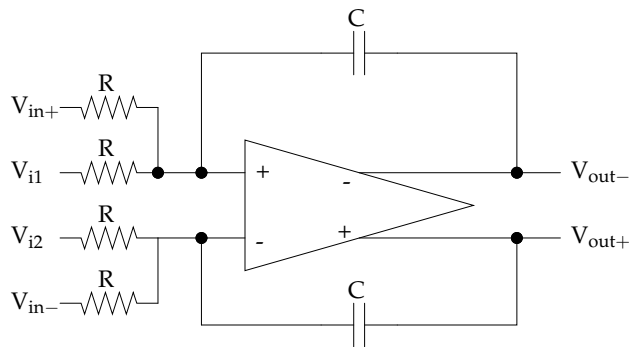


Figure 4.4: Realized integrator

The simulated Bode diagrams of both implementations are given in Fig. 4.5 and 4.6. These simulation results clearly demonstrate the integrating behaviour of the circuit in the frequency range of interest in between the dashed lines. The amplitude characteristic has a 20dB roll-off as expected for a first order transfer function, while the phase stays within  $1^\circ$  of the ideal  $90^\circ$  phase shift of an integrator at ADSL signal frequencies,  $3^\circ$  when expanding the range to the 10MHz limit cycle frequencies and  $9^\circ$  for the 30MHz high frequency second order system.

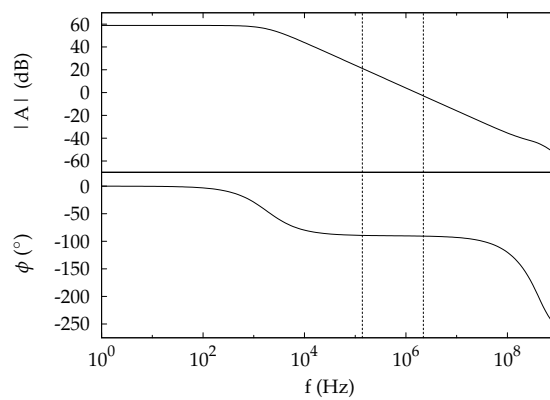


Figure 4.5: Bode plot of the 1.6MHz integrator

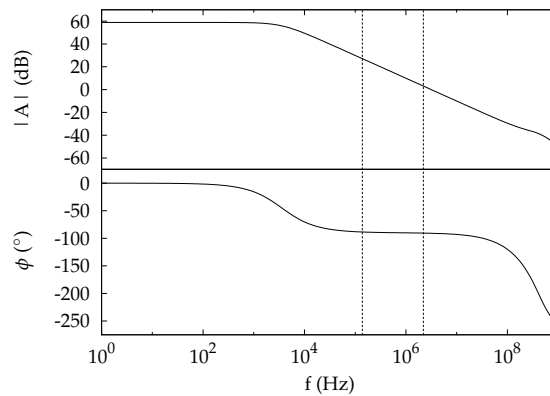


Figure 4.6: Bode plot of the 3.2MHz integrator

### 4.3 Building blocks

#### Voltage follower

The voltage follower used is the same folded cascode amplifier as used in the integrator, but with a single ended output. Since the main use for this amplifier will be buffering of the divided and low pass filtered output signal, an additional PMOS input pair is inserted to accommodate for input voltages below the sum of the saturation voltage of the NMOS current mirror and minimum gate-source voltage of the NMOS input pair, to maintain saturation in the remainder of the opamp transistors.

Figure 4.7 shows the schematic of the opamp simulated. In contrast to the comparator in section 2.3.1, no compensation for the variable transconductance is used, since the voltages are not expected to reach extreme values under normal operation due to the filter-divider.

The final dimensions of all transistors are given in table 4.6.

**Table 4.6:** Final dimensions of the opamp

Device	Width	Length
M <sub>1,2</sub>	35.50μm	0.35μm
M <sub>3</sub>	15.80μm	0.35μm
M <sub>11,12,13,14</sub>	7.90μm	0.5μm
M <sub>15,16</sub>	19.55μm	0.5μm
M <sub>17,18</sub>	39.10μm	0.5μm
M <sub>21,22</sub>	88.00μm	0.35μm
M <sub>23</sub>	39.10μm	0.5μm

Figure 4.8 gives the Bode plot of the amplifier for a common mode input voltage of 1.65V, resulting in a 338.34MHz gain bandwidth product and 57.88° phase margin. Furthermore, Fig. 4.9 shows the phase margin as a function of the common mode input voltage, leading to a minimal phase margin of 57.5° at 2.35V. Finally, in Fig. 4.10, the gain bandwidth product is plotted, depending on the common mode input voltage. In this figure, the gain bandwidth product at 1.65V common mode is higher than 338.34MHz, which is caused by the simulator algorithm used to generate this data.

Since ideally the gain bandwidth product only depends on the transconductance of the input differential pair and the load capacitance, as in equation (4.3), this gives a good measure of the transconductance. As expected, the bandwidth is maximal when both input pairs are active, while this is drastically reduced for extreme common mode input voltages, where only the NMOS or PMOS stage is active.



### 4.3 Building blocks

117

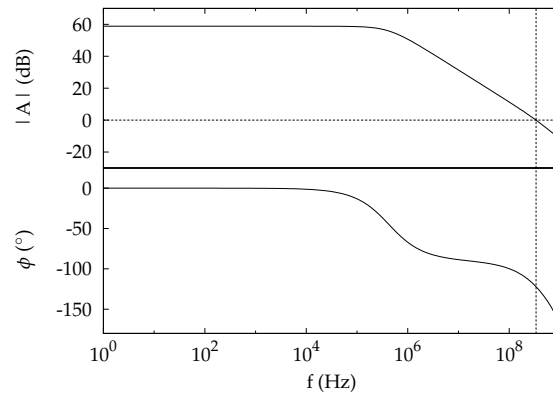


Figure 4.8: Bode diagram of the voltage follower, 1.65V input common mode

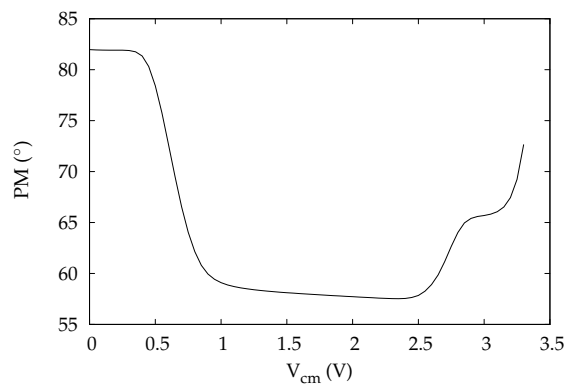


Figure 4.9: Phase margin of the opamp, depending on the common mode input voltage

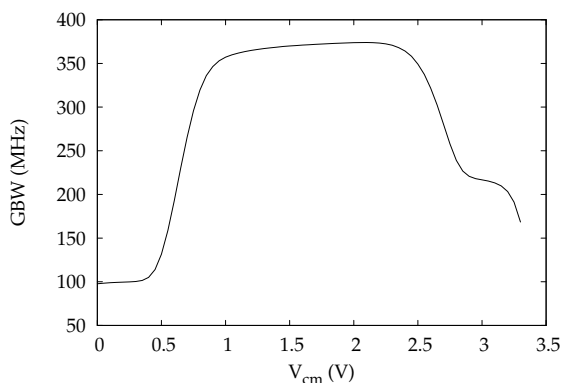


Figure 4.10: Gain bandwidth product of the opamp, depending on the common mode input voltage

### Biasing circuit

The one thing missing from Fig. 4.2 and 4.7 is the biasing circuit for the cascode transistors  $M_{13,14}$  and  $M_{15,16}$ . The schematic of the biasing circuit used, is given in Fig. 4.11, which is a Souch cascode current mirror [4]. This circuit actually takes care of the complete biasing, since transistor  $M_1$  can be used to bias the current sources. In addition, it can be shown that the voltage at the gate of transistor  $M_2$  equals the sum of the gate-source voltage of  $M_2$  and the saturation voltage of  $M_1$ , being exactly the voltage needed. Table 4.7 gives the transistor sizing for both the NMOS and PMOS biasing circuit.

Table 4.7: Transistor dimensions of the biasing circuit

Device	Width	Length
$M_{1,N}$	$7.90\mu\text{m}$	$0.5\mu\text{m}$
$M_{2,N}$	$7.90\mu\text{m}$	$0.5\mu\text{m}$
$M_{3,N}$	$2.65\mu\text{m}$	$0.5\mu\text{m}$
$M_{4,N}$	$7.90\mu\text{m}$	$0.5\mu\text{m}$
$M_{1,P}$	$19.55\mu\text{m}$	$0.5\mu\text{m}$
$M_{2,P}$	$19.55\mu\text{m}$	$0.5\mu\text{m}$
$M_{3,P}$	$6.50\mu\text{m}$	$0.5\mu\text{m}$
$M_{4,P}$	$19.55\mu\text{m}$	$0.5\mu\text{m}$

In the actual silicon implementation, the current sources will externally be re-



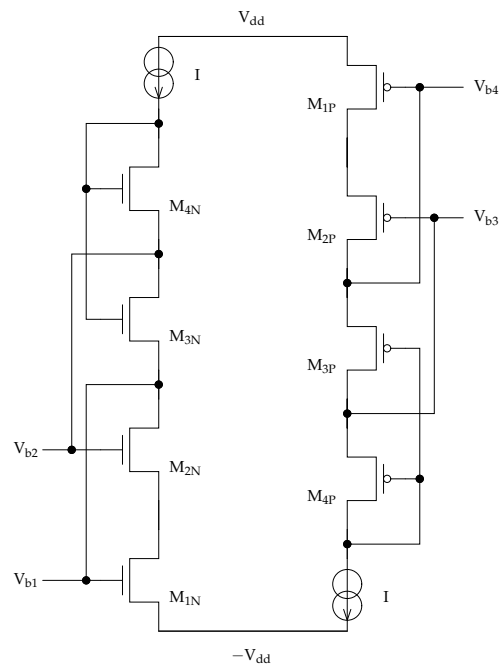


Figure 4.11: Biasing circuit for the folded cascode stage

placed by a trimpot in series with precision resistors to accurately tune the bias current to the nominal value from the simulations.

### 4.3.2 Comparator

Instead of using a regular opamp in open loop as comparator, as in chapter 2, a circuit based on a differential pair with positive feedback, as illustrated in Fig. 4.12, is used [5][6][7]. Both outputs then are sent to an inverter and latch, to source a fully digital compatible signal [8].

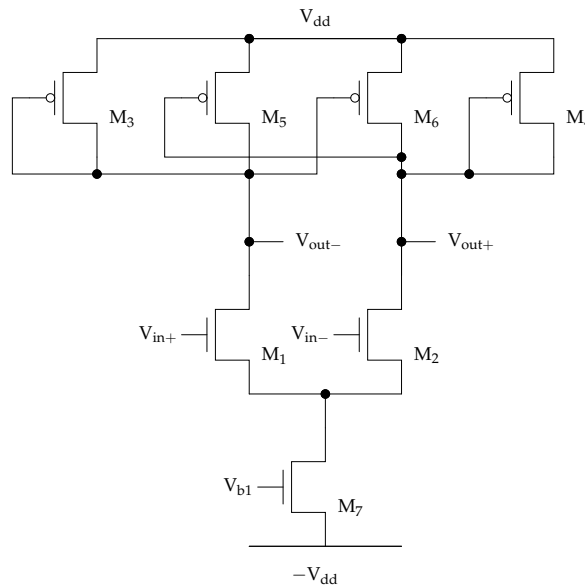


Figure 4.12: Basic circuit of the comparator

When omitting transistors  $M_5$  and  $M_6$  in Fig. 4.12, this is a classic differential pair with active load and balanced output. The gain of this stage simply is

$$A = \frac{g_{m1}}{g_{m3}} \quad (4.11)$$

The positive feedback by transistors  $M_5$  and  $M_6$  now forms an additional load to the differential pair, decreasing the current through  $M_3$  and  $M_4$ , which also decreases  $g_{m3}$  and increases the gain.

### 4.3 Building blocks

121

The trip point voltage of this comparator is [6]

$$V_{trip} = \frac{I_B}{g_{m1}} \frac{\frac{\beta_5}{\beta_3} - 1}{\frac{\beta_5}{\beta_3} + 1} \quad (4.12)$$

where

$$\beta = \frac{W}{L} \quad (4.13)$$

When transistors  $M_3$  and  $M_5$  have the same width to length ratio, there will be no hysteresis.

The bias current  $I_B$  through  $M_7$  is chosen  $32\mu A$ , which leads to the transistor dimensions in table 4.8, when using a saturation voltage of 0.5V for the current source  $M_7$  and 0.2V for  $M_1$  through  $M_6$ .

**Table 4.8:** Transistor dimensions of the basic comparator

Device	$\frac{W}{L}$
$M_{1,2}$	5.7
$M_{3,4}$	7.0
$M_{5,6}$	7.0
$M_7$	1.8

The circuit from Fig. 4.12 has one disadvantage, being the common mode voltage level at the outputs. This is overcome in the final circuit from Fig. 4.13 by inserting an additional load with positive feedback. Further optimization leads to the transistor dimensions in table 4.9.

The simulation result for a 10MHz, 200mV sinewave input is given in Fig. 4.14, leading to a 2.46ns delay for a rising edge at the output and 2.8ns for a falling edge. This slight asymmetry is not a problem, since this can be used as a part of the time delay to avoid feed-through currents at the output stage.

#### 4.3.3 Output stage

The schematic of the high voltage output stage is given in Fig. 4.15. As with the first order system from section 2.4, the parallel free running diodes as seen in Fig. 2.4 are omitted, while the intrinsic parasitic diodes of the DMOS output transistors take over their role.

The output filter chosen is a third order Chebychev low pass filter with 1dB ripple in the passband. The normalized component values are given in table 4.10 [9].

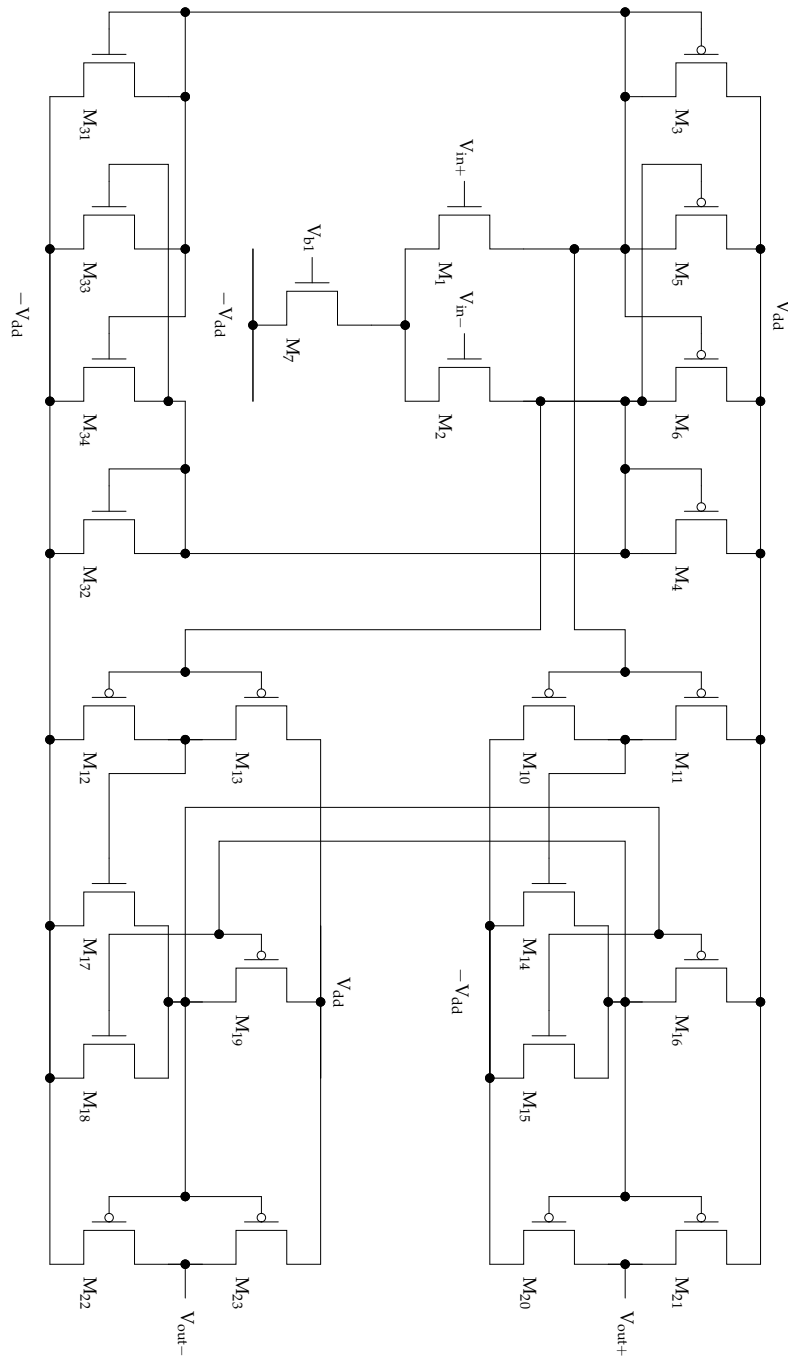


Figure 4.13: Final circuit of the comparator

Table 4.9: Transistor dimensions of the comparator

Device	Width	Length
$M_{1,2}$	$2.40\mu\text{m}$	$0.35\mu\text{m}$
$M_{3,4}$	$2.00\mu\text{m}$	$0.35\mu\text{m}$
$M_{5,6}$	$2.00\mu\text{m}$	$0.35\mu\text{m}$
$M_7$	$1.80\mu\text{m}$	$1.00\mu\text{m}$
$M_{10,12}$	$0.80\mu\text{m}$	$0.35\mu\text{m}$
$M_{11,13}$	$2.80\mu\text{m}$	$0.35\mu\text{m}$
$M_{14,17}$	$2.00\mu\text{m}$	$0.35\mu\text{m}$
$M_{15,18}$	$0.80\mu\text{m}$	$0.35\mu\text{m}$
$M_{16,19}$	$2.00\mu\text{m}$	$0.35\mu\text{m}$
$M_{20,22}$	$0.80\mu\text{m}$	$0.35\mu\text{m}$
$M_{21,23}$	$2.00\mu\text{m}$	$0.35\mu\text{m}$
$M_{31,32}$	$0.80\mu\text{m}$	$0.55\mu\text{m}$
$M_{33,34}$	$0.80\mu\text{m}$	$0.55\mu\text{m}$

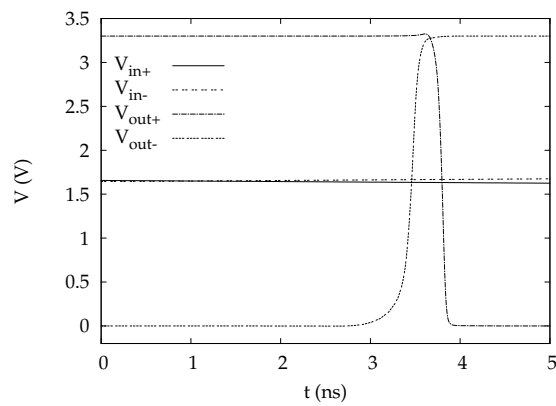


Figure 4.14: Simulation result of the comparator

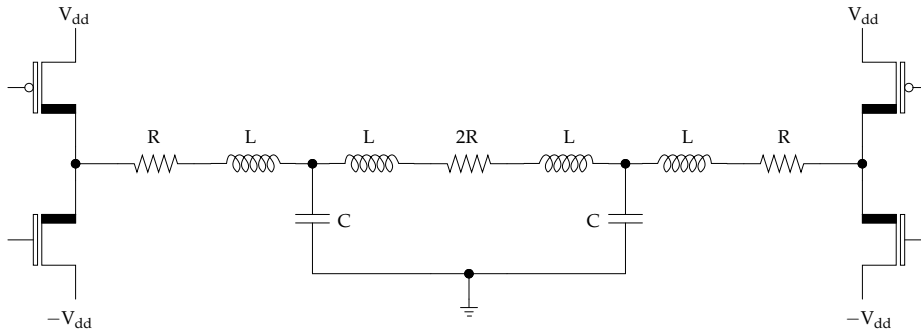


Figure 4.15: Schematic of the high voltage output stage

The final values, depending on the actual value of the termination resistance  $R$  and cut-off frequency  $f$  are

$$L = \frac{R}{2\pi f} L_N \quad (4.14)$$

$$C = \frac{1}{2\pi f R} C_N \quad (4.15)$$

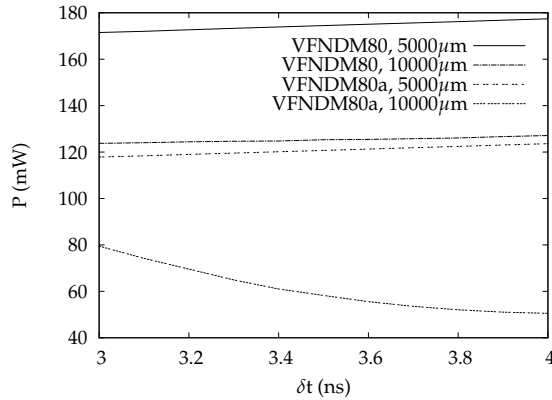
The value of the termination resistance  $R$  is known, since the circuit is expected to work at a 25V power supply and a transformer with a 1:2 turns ratio, so  $R = 12.5\Omega$ . Also note these components are external, so the exact value of the filter cut-off frequency can be changed freely afterwards, depending on the measured limit cycle frequency and the desired signal bandwidth, without affecting the dimensions or layout of any other system component.

Table 4.10: Normalized values for a third order Chebychev low pass filter with 1dB ripple

Component	Normalized value
$R_N$	1
$L_N$	2.2160
$C_N$	1.0883

As for the output stage itself, according to table 4.1, only a choice of the low side switch is required. Preliminary simulations on the output stage lead to a preference for the analogue VFNDM80a transistor, due to its lower dissipation. The results of this simulation are illustrated in Fig. 4.16.

These simulations however lead to enormous dimensions of the DMOS transistors to deliver the peak voltages, so the question rises if this requirement can be



**Figure 4.16:** Comparison of power dissipation between the VFNDM80 and VFNDM80a DMOS as a function of the time delay, for different widths

relaxed. As a result, simulations were performed with largely reduced widths for both the NDMOS and PDMOS output transistors, while using the increased output impedance as part of the matching resistance. The limit on the transistor size now is determined by the process corners, since even under worst case processing corners, the output impedance should not exceed the nominal matching impedance. This finally leads to the dimensions in table 4.11, giving the total width of all devices and the number of devices placed in parallel for reasons of simulation accuracy. The nominal resistance of each DMOS is approximately  $7\Omega$ .

**Table 4.11:** Dimensions of the output transistors

Device	Width	Parallel
VFNDM80a	3200 $\mu\text{m}$	16
LFPDM80	6400 $\mu\text{m}$	16

Using these dimensions, a simulation is performed, sweeping the duty cycle of the DMOS input signal to mimic the behaviour of this stage in a closed loop. This situation is not exactly how the closed loop system will behave, although the oscillating frequency is adjusted according to [10] for DC input signals with normalized voltage  $V$

$$f_k = (1 - V^2)f_0 \tag{4.16}$$

but this certainly gives an estimate of system performance. Figure 4.17 gives the simulated output voltage as a function of duty cycle, while Fig. 4.18 shows the input power.

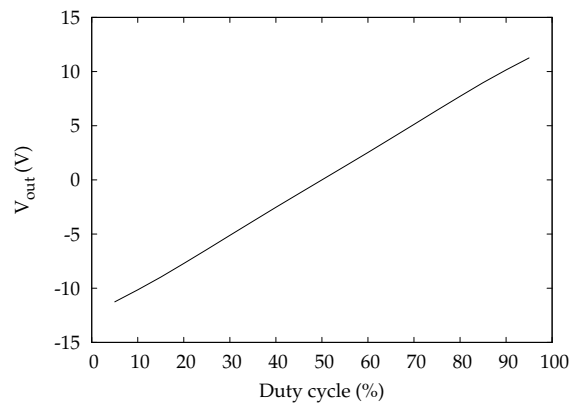


Figure 4.17: Output voltage as a function of duty cycle

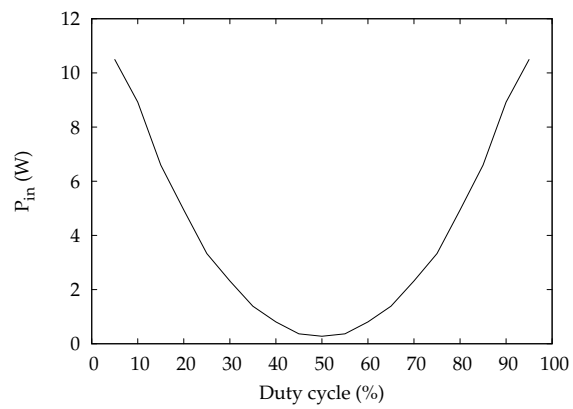


Figure 4.18: Input power as a function of duty cycle



Table 4.12: Transistor dimensions of the delay circuit

Device	Width	Length
$N_{1,2,N}$	$0.8\mu\text{m}$	$0.35\mu\text{m}$
$N_{1,2,P}$	$8.0\mu\text{m}$	$0.35\mu\text{m}$
$I_{2,3,N}$	$0.8\mu\text{m}$	$0.35\mu\text{m}$
$I_{2,3,P}$	$2.0\mu\text{m}$	$0.35\mu\text{m}$
$I_{4,5,6,7,N}$	$0.8\mu\text{m}$	$1.20\mu\text{m}$
$I_{4,5,6,7,P}$	$2.0\mu\text{m}$	$1.20\mu\text{m}$

When assuming a linear relation between input voltage and duty cycle, the technique from section 2.4.1 can be used to estimate the efficiency of the system with a xDSL signal, leading to an efficiency estimate of about 20%.

#### 4.3.4 Time delay, level shifter and buffers

The schematic of the delay circuit, again, is the simple circuit from Fig. 2.9, but since the output of the comparator is balanced, there is no need for the inverter  $I_1$ . The optimized dimensions of the transistors, taking into account the slight unbalance between rising and falling edge of the comparator output, are given in table 4.12.

The level shifter was changed significantly compared to the one in Fig. 2.6 and is given in Fig. 4.19.

The low side of the level shifter again is a NMOS switch with a cascode NDMOS. The high side now is formed by a flip-flop, increasing the level shifter speed compared to the basic version used throughout chapter 2 and ensuring both PMOS transistors are steered in counterphase. Additionally, this also means the high side contains a bi-stable memory cell, so the level shifter can be turned off to reduce power consumption. Therefore, a basic level shifter as in Fig. 4.20 is inserted at both outputs, switching off the level shifter transistors  $M_1$  and  $M_2$  with the NOR gates formed by  $M_{17}$  to  $M_{24}$ . This ensures the proper functioning of the low to high level shifter, while the dimensions on the high to low level shifter are not determined based on speed but power and can thus be reduced. As a result, the lower mobility  $\mu_0$  of the PMOS will be beneficial to this end.

The optimized transistor dimensions are given in tables 4.13 and 4.14 for the low to high and high to low level shifter respectively. The delay times are 0.78ns for the falling edge and 1.57ns for the rising edge, as illustrated in Fig. 4.21. The power consumption is 2.2mW, so the circuit is both more efficient and faster than the level shifters from chapter 2.

Due to the large size of the DMOS output transistors, the signals from the delay circuits need to be buffered. In [8] and [11] a simple formula is given to properly

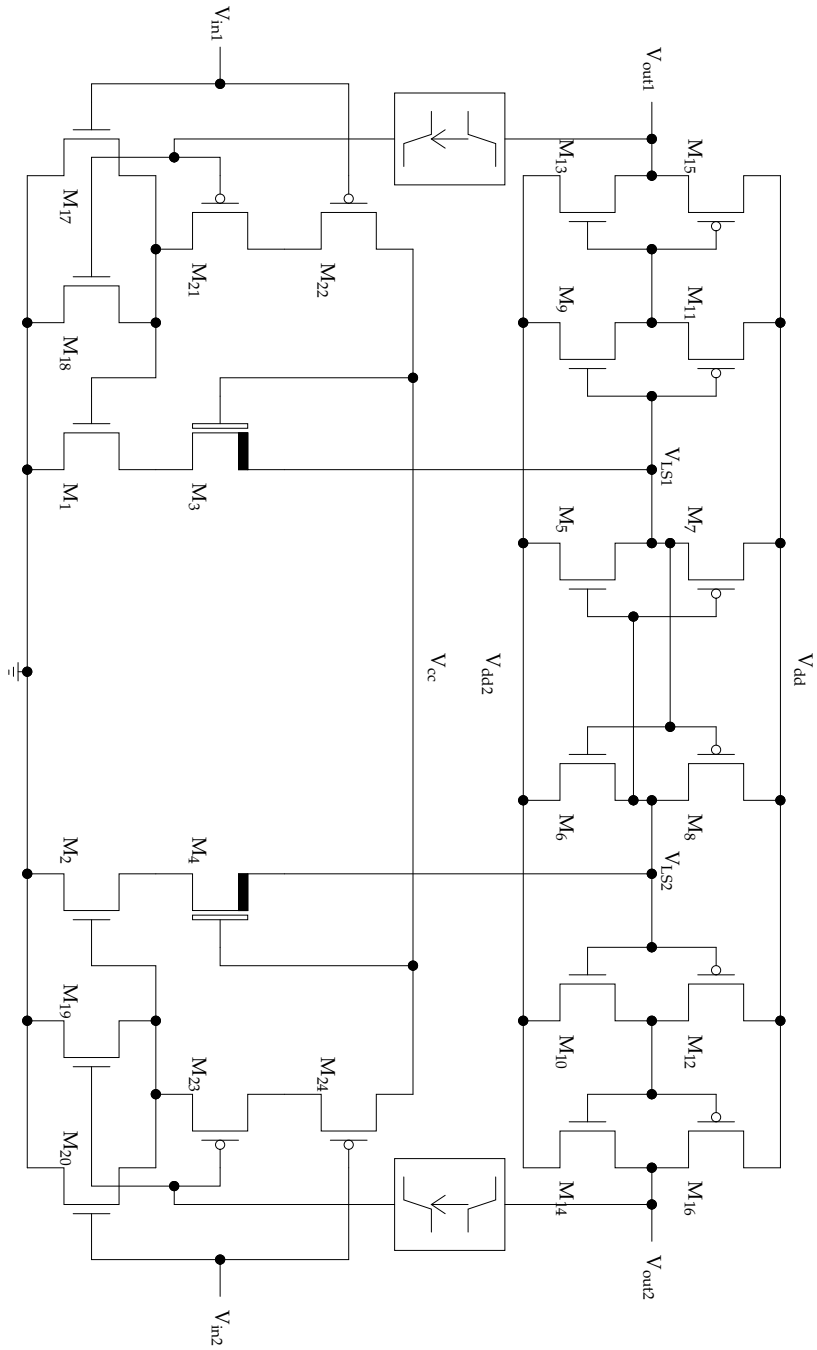


Figure 4.19: Schematic of the level shifter

### 4.3 Building blocks

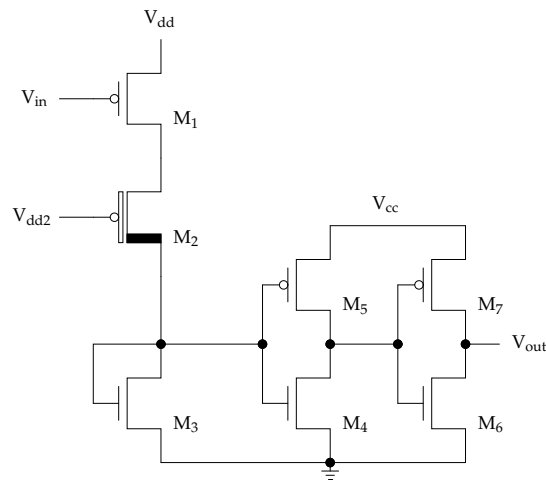


Figure 4.20: Schematic of the high to low level shifter

Table 4.13: Transistor dimensions of the low to high level shifter

Device	Width	Length
M <sub>1,2</sub>	20.0μm	0.35μm
M <sub>3,4</sub>	10.0μm	fixed
M <sub>5,6</sub>	20.0μm	0.35μm
M <sub>7,8</sub>	10.0μm	0.35μm
M <sub>9,10</sub>	1.0μm	1.00μm
M <sub>11,12</sub>	10.0μm	0.35μm
M <sub>13,14</sub>	10.0μm	0.35μm
M <sub>15,16</sub>	2.0μm	0.35μm
M <sub>17,18,19,20</sub>	4.0μm	0.35μm
M <sub>21,22,23,24</sub>	20.0μm	0.35μm

Table 4.14: Transistor dimensions of the high to low level shifter

Device	Width	Length
M <sub>1</sub>	1.0μm	1.00μm
M <sub>2</sub>	5.0μm	fixed
M <sub>3</sub>	1.0μm	4.50μm
M <sub>4</sub>	0.8μm	0.35μm
M <sub>5</sub>	1.0μm	0.35μm
M <sub>6</sub>	3.0μm	0.35μm
M <sub>7</sub>	6.0μm	0.35μm

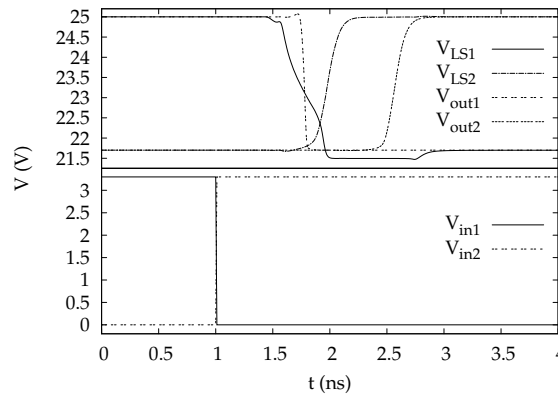


Figure 4.21: Simulation of the level shifter

size these buffers, depending on the input capacitance  $C_{G,1}$  of the first inverter and the load  $C_L$ :

$$N = \ln \frac{C_L}{C_{G,1}} \quad (4.17)$$

with  $N$  the number of inverter stages, sized by a factor  $e = 2.718$ . When using an input capacitance of 6.6fF, a NDMOS load capacitance of 60pF and a PDMOS load of 30pF, this leads to 9 stages for the NDMOS and 8 stages for the PDMOS.

Further optimizations lead to a sizing factor of 3, with the PMOS width chosen double that of the corresponding NMOS transistor and the calculated number of stages. The simulation results of the buffer stages are given in Fig. 4.22, leading to a total delay time of 2.17ns for the NDMOS buffer and 0.9ns for the PDMOS buffer.

### 4.3.5 Passive filter-divider

The schematic of the passive filter-divider is shown in Fig. 4.23. For simplicity, the second order filter is implemented as two RC-filters with the same component values in series. As opposed to the previous designs, the actual divider is placed after the filter, so the filter gets its input signal directly from the amplifier, while being minimally loaded, allowing for a highly impedant divider. This finally leads to following set of conditions

$$R_2 = R_1 \quad (4.18)$$

$$C_2 = C_1 \quad (4.19)$$

$$\frac{R_4}{R_1 + R_2 + R_3 + R_4} = \frac{3.3}{25} \quad (4.20)$$

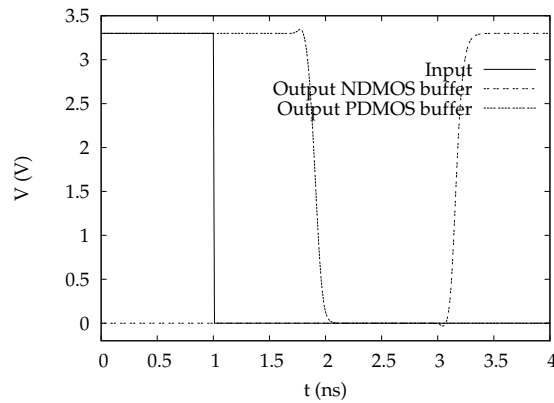


Figure 4.22: Simulation of the buffers

where the last equation serves the conversion of the output from a 25V supply to the 3.3V circuitry.

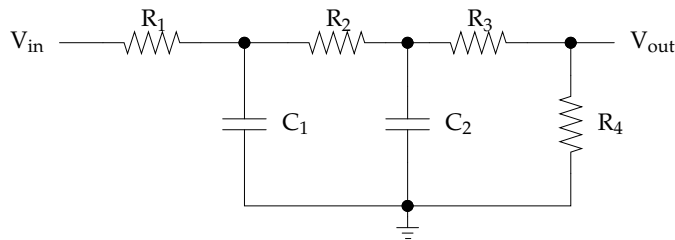


Figure 4.23: Schematic of the filter-divider

Another difference with both I<sup>2</sup>T100 designs is the better modelling of parasitic capacitances in the resistors, meaning every single resistor in the filter or divider will contribute to the final filter transfer. As a result, initial values for  $R_1$  and  $C_1$  were chosen, but had to be optimized in the closed loop system. A side effect of this closed loop optimization is that the additional time delays in the system can be compensated as well by the filter.

**First order loop**

The time constant of the second order low pass filter for the 6MHz first order loop was calculated as

$$\tau_g = \frac{1}{2\pi \cdot 6 \cdot 10^6 \text{Hz}} \tag{4.21}$$

**Table 4.15:** Dimensions of the first order loop filter components

Device	Value
R <sub>1</sub>	11.70kΩ
R <sub>2</sub>	11.70kΩ
R <sub>3</sub>	245.7kΩ
R <sub>4</sub>	40.95kΩ
C <sub>1</sub>	470fF
C <sub>2</sub>	470fF

**Table 4.16:** Dimensions of the 10MHz second order loop filter components

Device	Value
R <sub>1</sub>	9.75kΩ
R <sub>2</sub>	9.75kΩ
R <sub>3</sub>	204.75kΩ
R <sub>4</sub>	34.125kΩ
C <sub>1</sub>	46.95fF
C <sub>2</sub>	46.95fF

Further simulations lead to a higher cut-off frequency of the filter, using the component values from table 4.15.

### 10MHz second order loop

For the 10MHz second order loop, the time constant calculated was

$$\tau_g = 0.0000000134s \approx \frac{1}{2\pi \cdot 11.88 \cdot 10^6 Hz} \quad (4.22)$$

Again, all calculated component values needed serious downscaling due to the significant contribution of the modelled parasitics. The final values are summarized in table 4.16.

### 30MHz second order loop

For the 30MHz loop, the parasitics contribution was so high, that in order to reach

$$\tau_g = \frac{1}{200 \cdot 10^6 Hz} \approx \frac{1}{2\pi \cdot 32 \cdot 10^6 Hz} \quad (4.23)$$

both capacitors had to be omitted. The final limit cycle frequency is about 17MHz, since 30MHz would require too small a value for all resistors, resulting in increased power dissipation. Table 4.17 gives an overview of the values chosen for this loop filter.

#### 4.4 First order system

133

**Table 4.17:** Dimensions of the 30MHz second order loop filter components

Device	Value
R <sub>1</sub>	5.85kΩ
R <sub>2</sub>	5.85kΩ
R <sub>3</sub>	122.85kΩ
R <sub>4</sub>	20.475kΩ
C <sub>1</sub>	omitted
C <sub>2</sub>	omitted

**Table 4.18:** Dimensions of the third order loop filter components

Device	Value
R <sub>1</sub>	9.75kΩ
R <sub>2</sub>	9.75kΩ
R <sub>3</sub>	204.75kΩ
R <sub>4</sub>	34.125kΩ
C <sub>1</sub>	omitted
C <sub>2</sub>	omitted

#### Third order loop

The time constant of the third order system suffers a similar problem as the high frequent second order loop, due to the smaller time constant to reach a similar limit cycle frequency:

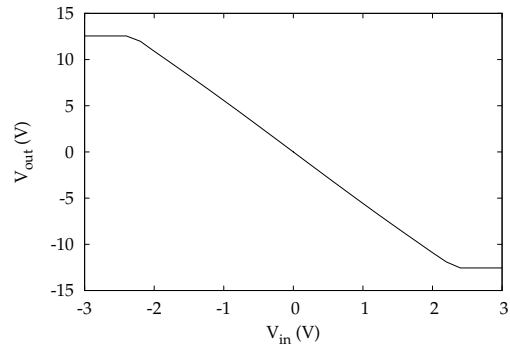
$$\tau_g = \frac{1}{109 \cdot 10^6 \text{ Hz}} \approx \frac{1}{2\pi \cdot 17.3 \cdot 10^6 \text{ Hz}} \quad (4.24)$$

Using the same resistor values as the 10MHz second order loop, but omitting the capacitors yields the desired limit cycle frequency. The values of all filter components are given in table 4.18 for reference.

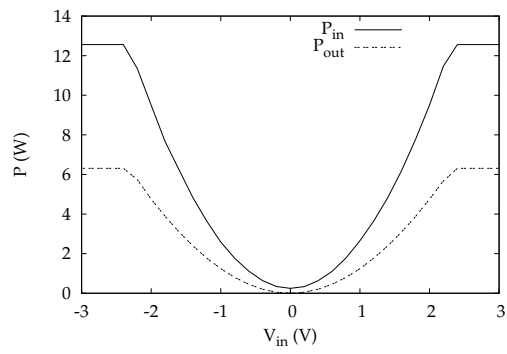
#### 4.4 First order system

In analogy with the simulations in chapter 2, DC simulations are performed on the full circuit, leading to the input output transfer from Fig. 4.24a and the power curves in Fig. 4.24b. This finally leads to the DC efficiency in Fig. 4.24c, showing the steep increase towards the maximum of 50%, before saturation kicks in. This figure of 50% is caused by the dissipation in the required matching resistors and DMOS output stage.

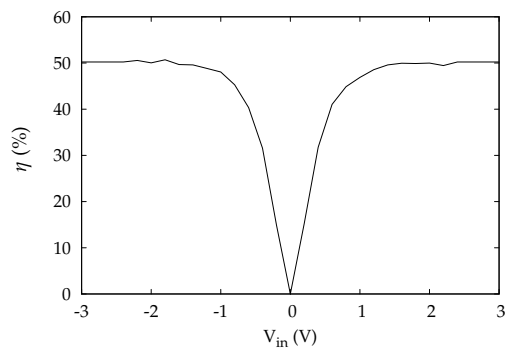
Using equation (2.27), this allows for calculation of the efficiency when amplifying a MTPR signal, resulting in an estimate of 22.98%.



(a) DC transfer



(b) Input and output power



(c) DC efficiency

Figure 4.24: DC simulation of the first order system



#### 4.5 10MHz second order system

135

In addition to the DC simulations, also the response to several sinewave inputs was generated to compare the simulations to the calculations from chapter 3. For comparison, frequencies of 200kHz, 500kHz and 1MHz were chosen, of which the resulting third order harmonic distortion is given in Fig. 4.25, together with the calculated, limit cycle compensated curve. The sinewave amplitudes are scaled according to the DC transfer from Fig. 4.24a to the corresponding relative amplitude, mapping the DC full scale to a nominal value of 1, as used throughout chapter 3.

For the 200kHz signal, the simulated curve coincides perfectly with the calculations, as for the 500kHz and 1MHz inputs, the simulated distortion is lower. It should however be noted that the calculations do not take the influence of any output filter whatsoever into account, so due to the 1.5MHz low pass filter, there is an additional reduction of 3dB and 25dB for the respective curves. After correction, this again leads to an excellent correspondence.

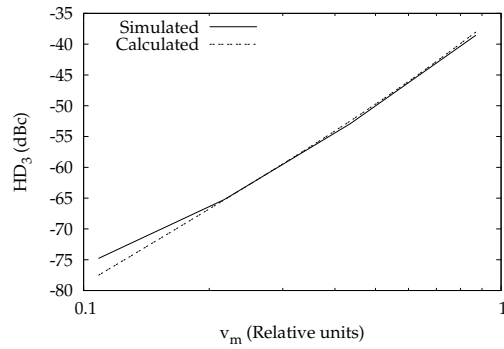
#### 4.5 10MHz second order system

The results of the DC simulations on the 10MHz second order amplifier are given in Fig. 4.26, showing similar behaviour as the first order system. In this case, the calculated MTPR efficiency is 23.18%.

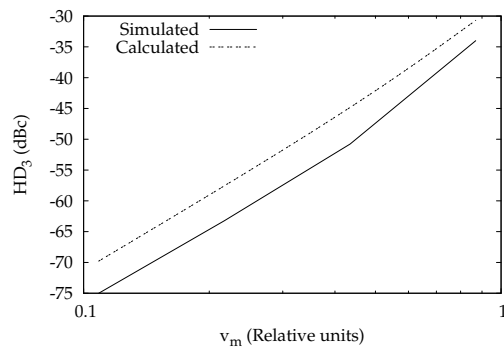
For the sinewave simulations, the cut-off frequency of the output filter is 2.5MHz, so only the result at 1MHz should be increased by 9dB, due to the filter contribution. The results are given in Fig. 4.27. For the 500kHz and the 1MHz, there is good correspondence between calculations and simulations, or an even better simulated result, whereas the 200kHz simulation is 10dB off.

It should however be noted that the curve at 200kHz starts at an already low value of -77dBc and due to the lower frequency, there will be less periods simulated, meaning reduced averaging by the Fourier transform. There will also be an additional contribution by the opamp circuits and the modelled non-linearities of the passive components, further increasing the simulated distortion.

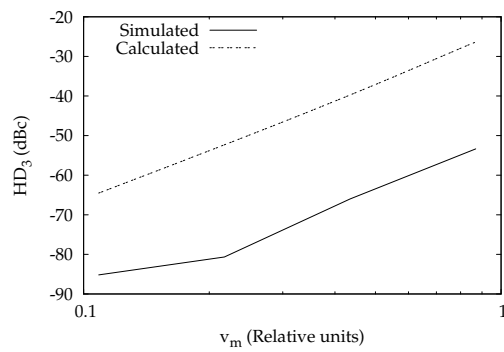
Furthermore, inclusion of a time delay into the model, while decreasing the filter time constants to maintain the same limit cycle frequency, is expected to increase distortion. Since the time delays of all five circuits are about equal, this effect will be more pronounced at higher limit cycle frequencies. As a result, the model for the first order system will be more accurate than those for the higher order loops compared to their respective implementations.



(a) 200kHz input sine wave



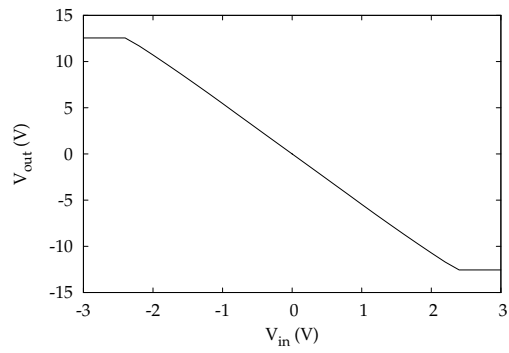
(b) 500kHz input sine wave



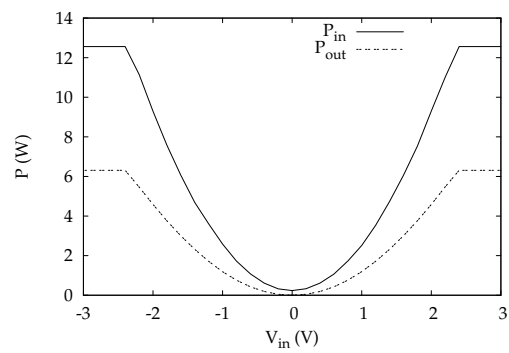
(c) 1MHz input sine wave

Figure 4.25: Third order harmonic distortion of the first order system

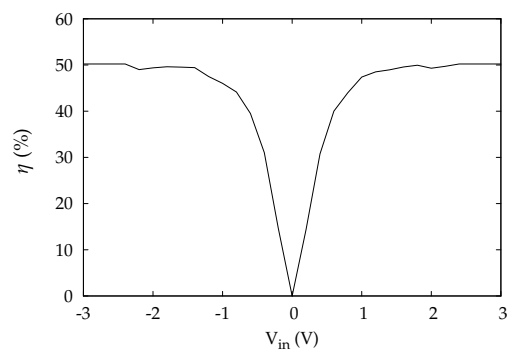
4.5 10MHz second order system



(a) DC transfer

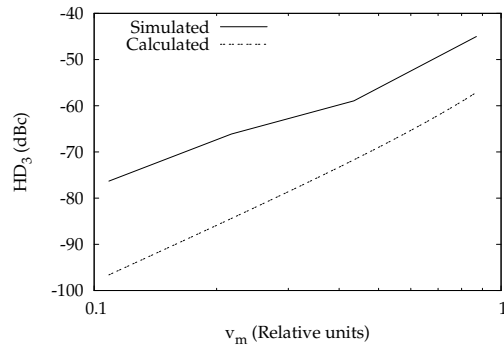


(b) Input and output power

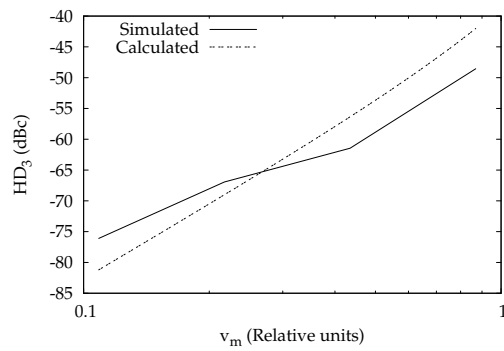


(c) DC efficiency

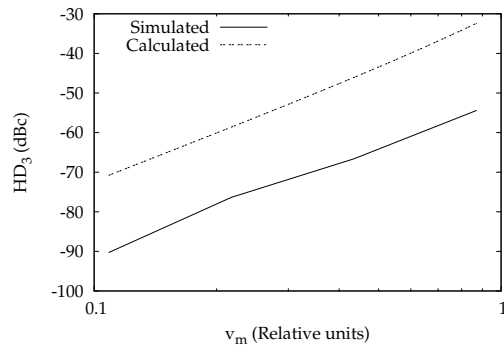
Figure 4.26: DC simulation of the 10MHz second order system



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 4.27: Third order harmonic distortion of the 10MHz second order system

## 4.6 30MHz second order system

Figure 4.28 shows the results of the DC simulations for the 30MHz second order loop, which again are similar to the transfers of the first order system. The resulting prediction of the MTPR efficiency is 21.00%.

The results for the sinewave simulations are given in Fig. 4.29, this time with a 4MHz output filter, which does not significantly attenuate the third harmonic of the input signals used.

The correspondence between simulations and calculations for this circuit is not so good, which can be explained by the much lower simulated limit cycle frequency of 17MHz compared to the calculated 30MHz, which in this case also means large differences between the time constants. The increased importance of all system time delays due to the high limit cycle frequency further deteriorates the results.

## 4.7 Third order system

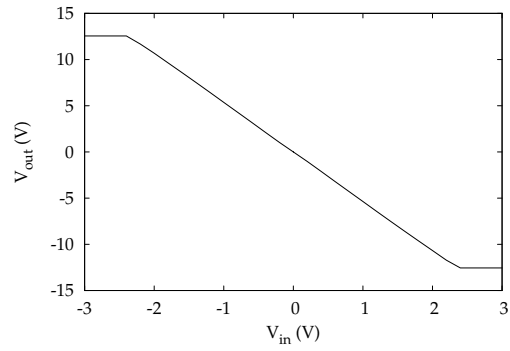
The results of the DC simulations on the third order system are presented in Fig. 4.30, leading to similar conclusions as before. The calculated efficiency of a MTPR signal is 21.28%.

The third order system again uses a 2.5MHz output filter, thus requiring the 9dB compensation at the 1MHz input. The results can be found in Fig. 4.31. As before, the correspondence at 200kHz is not good, but this improves at higher input frequencies, to be only slightly off at 1MHz, as with the 10MHz second order system. This also can be explained by the reasoning of the previous sections.

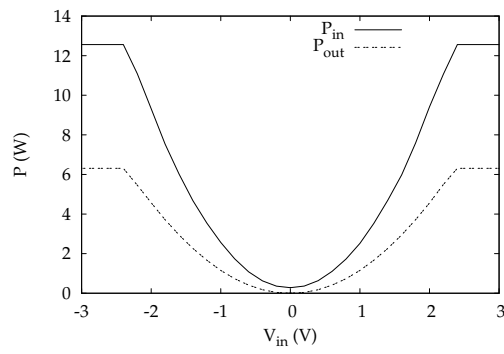
## 4.8 Second order system with independent loops

The final circuit is the special case of two independent, single ended second order systems, together acting as a balanced amplifier. The loops used are identical to that of the 10MHz second order system in section 4.5. Figure 4.32 shows the results of the DC simulations. The efficiency expected for a MTPR signal is 19.30%.

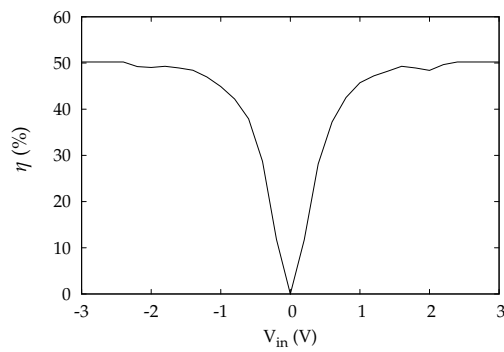
The results of the distortion simulations in Fig. 4.33 are almost equal to those for the corresponding single loop system, only slightly worse for low amplitudes at 200kHz input. The calculated and simulated distortion at 500kHz and 1MHz again are found to correspond well.



(a) DC transfer



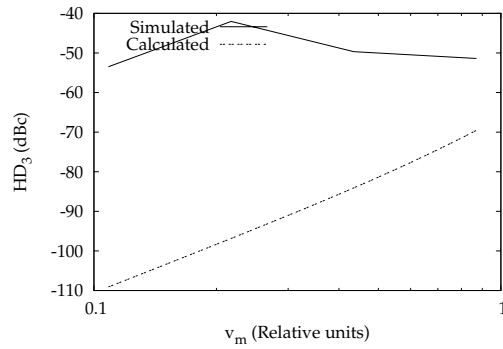
(b) Input and output power



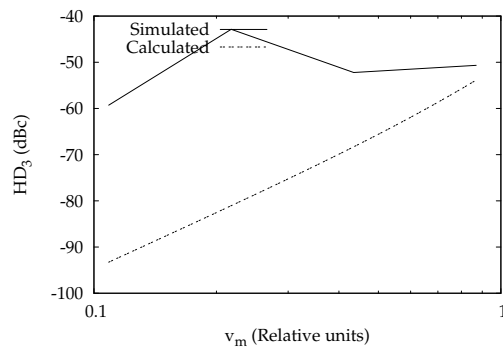
(c) DC efficiency

Figure 4.28: DC simulation of the 30MHz second order system

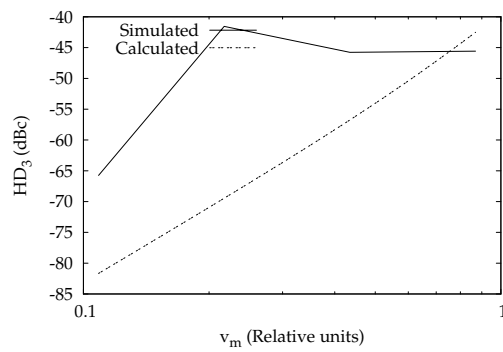
4.8 Second order system with independent loops



(a) 200kHz input sine wave

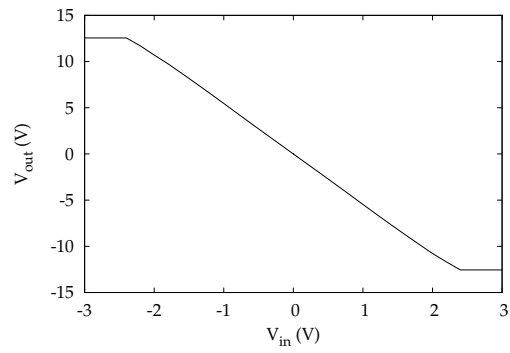


(b) 500kHz input sine wave

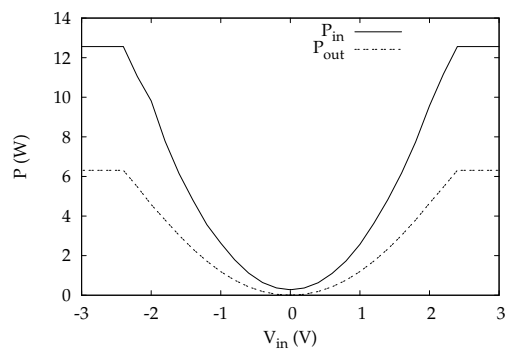


(c) 1MHz input sine wave

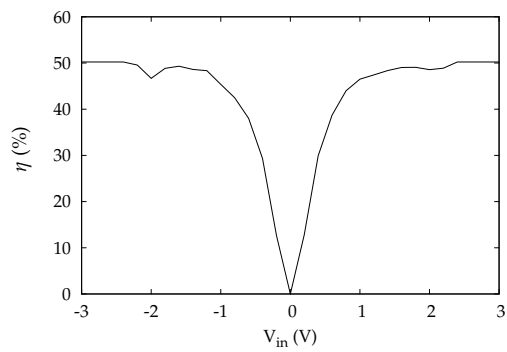
Figure 4.29: Third order harmonic distortion of the 30MHz second order system



(a) DC transfer



(b) Input and output power

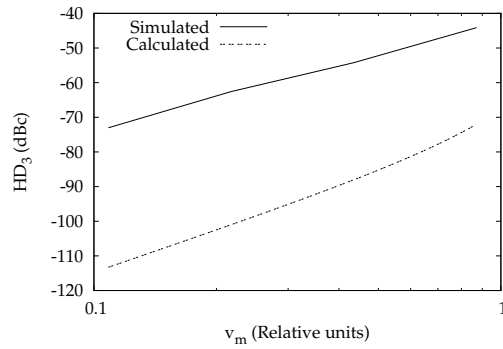


(c) DC efficiency

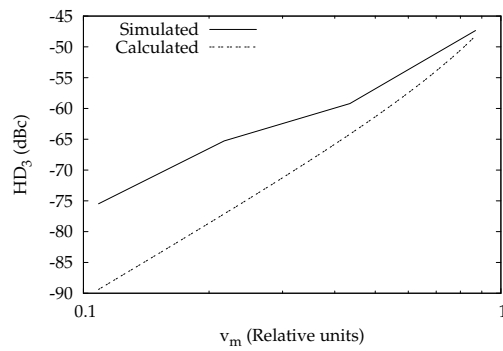
Figure 4.30: DC simulation of the third order system



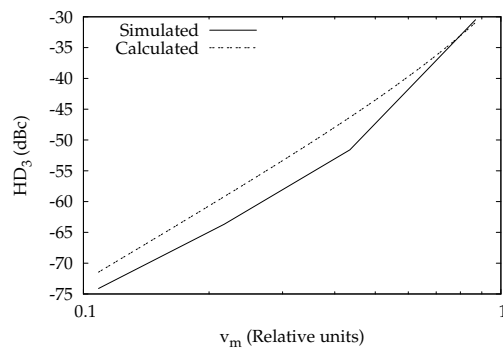
### 4.8 Second order system with independent loops



(a) 200kHz input sine wave

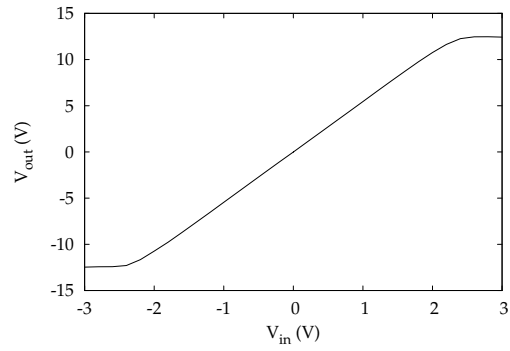


(b) 500kHz input sine wave

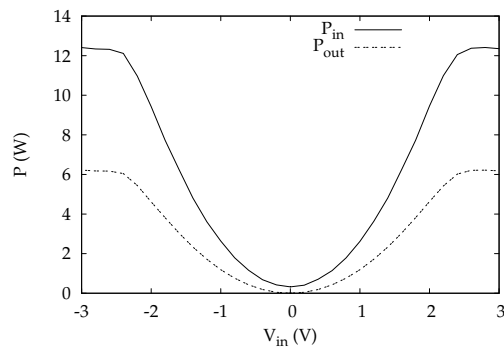


(c) 1MHz input sine wave

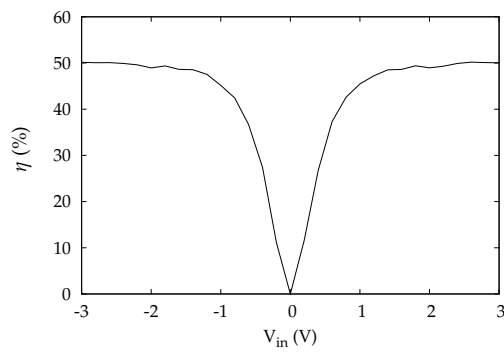
Figure 4.31: Third order harmonic distortion of the third order system



(a) DC transfer



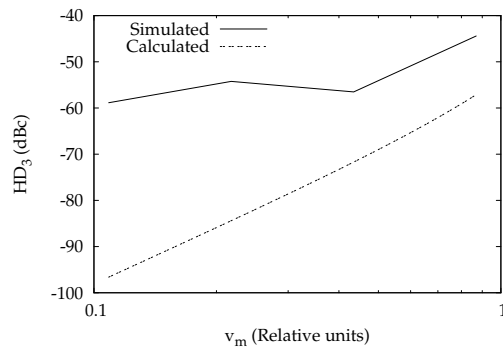
(b) Input and output power



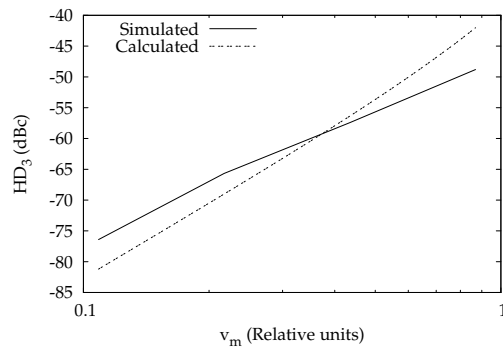
(c) DC efficiency

Figure 4.32: DC simulation of the second order system with independent loops

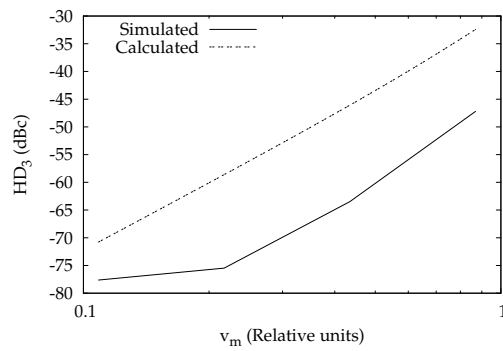
### 4.8 Second order system with independent loops



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

**Figure 4.33:** Third order harmonic distortion of the second order system with independent loops

## 4.9 Layout considerations

To finally verify the preliminary calculations and full circuit simulations, a silicon implementation is required. Due to the presence of quite sensitive analogue circuits in combination with both the high voltage and digital parts, special care must be taken to avoid or suppress their harmful contribution.

### 4.9.1 Interconnection

A first elementary option is the use of separate supply lines for analogue and digital circuits [12], [13]. The specificity of the I<sup>3</sup>T80 technology is of great importance in this regard, since all processing starts from a N-type epitaxial layer on top of a P-type substrate. On the one hand, this means there still is an ohmic contact between eventual separated ground supply lines, but on the other hand, the impedance is a lot higher than with a simple metallic connection. The technology also uses pockets with a N-type substrate, that are trivial to separate from each other by inserting a deep P-type implant in between, connecting to the P-type substrate.

This finally leads to two separate inputs for the 25V supply, being one for the switching output and one for the level shifter, an analogue and a digital 3.3V supply and three ground connections for analogue, low voltage digital and the high voltage output stage.

The one component falling between the cracks, is the comparator, which converts the analogously processed signals into digital form. The supply chosen for this component is the analogue one, with as big a decoupling capacitor as possible between the supply lines, close to the component.

This suggests a further optimization in the form of decoupling capacitances for all DC signals, such as the voltage references for the integrator common mode loop, the current reference input and the power supply lines. Since capacitors of significant value are expensive to implement, the metal tracks can be stacked to create additional capacitance and must be combined with off chip components.

Additionally, the resistance of the power tracks must be controlled, since putting all components in series will create a gradual voltage shift, such that the immediate power consumption of all components will influence all other components on the same branch. The solution to this problem is to create a wide, low ohmic base track and feed all components in parallel.

As for the reference input signals, the capacitive coupling of harmful signals can also be reduced by shielding the tracks with the analogue ground supply, placing tracks above, below and beside and interconnecting all with vias.

To improve the symmetry, the length of tracks with complementary signals should also be as equal as possible to reduce unbalance.

### 4.9.2 Components

Besides issues with electromagnetic compatibility, also the placement of the individual transistors relative to each other can play a significant role in system performance [2].

For the differential input stages, each transistor should be replaced by two transistors of half the original width. This allows for a centroid layout with both halves placed in the opposite corner, eliminating first order variations in the processing.

Current source devices related to the same mirror should be placed close to each other and be of the same size or multiple parallel devices of the same size, to reduce the relative importance of size dependent effects at the transistor edges. To further improve matching, dummy transistors can be placed at both ends, which will avoid asymmetry of the outer transistors due to their asymmetric environment. Placing the current mirror transistor in the middle of the row will also reduce the maximal mismatch.

Of course, the same holds for the resistors and capacitors used for opamp stabilization, integrators and loop filter with divider. For the capacitors and integrator resistors, a simple centroid as with the differential pair suffices. For the filter-divider, the situation is more complex, due to the unequal sizes of the resistors.

However, upon closer inspection of the values given in tables 4.15 to 4.18,  $R_1$  and  $R_2$  can be divided in two equal resistors and  $R_3$  and  $R_4$  in 42 and 7 identical resistors respectively. Due to the total size of these 106 smaller resistors, it will be advantageous to also use dummy resistors on all four edges of the centroid.

To further improve matching, the current flow in the devices should be the same as well, meaning the devices must be parallel to each other, with current flowing in the same direction and contacted in an identical way.

It should immediately be clear that the above partition of devices will have some influence on the system behaviour, due to slightly different component parameters. As a result, all simulations should be repeated for the adjusted schematic as well. For simplicity, all simulation results given in this chapter already take these changes into account and thus correspond to the final circuits as implemented.

## 4.10 Conclusion

The building blocks, required to implement the five different asynchronous oscillating amplifiers, are simulated. The results of DC simulations on the amplifiers are presented, showing no significant difference in efficiency. Table 4.19 summarizes the calculated efficiencies for a MTPR signal, based on these simulation results. The simulated efficiencies for the first order systems from section 2.4 are included for reference. The final result is a doubling of the efficiency compared to

**Table 4.19:** Summary of the calculated efficiencies

Amplifier	Efficiency
First order	22.98%
Second order 10MHz	23.18%
Second order 30MHz	21.00%
Second order, independent loops	19.30%
Third order	21.28%
Basic first order (I <sup>2</sup> T100)	9.67%
Cascode first order (I <sup>2</sup> T100)	9.94%
Reference [14] (measured)	14.3%
Reference [15] (measured)	13.5%

the previous designs and a significant increase compared to references [14] and [15].

Simulations using a sinewave input further serve to validate the calculations from chapter 3, showing good correspondence when additional time delays in the circuit are small compared to the limit cycle period. For lower input frequencies and amplitudes, the accuracy of the model also gets worse for numerical reasons and because the system performance also is limited by the linearity of the components in the loop, both active and passive.

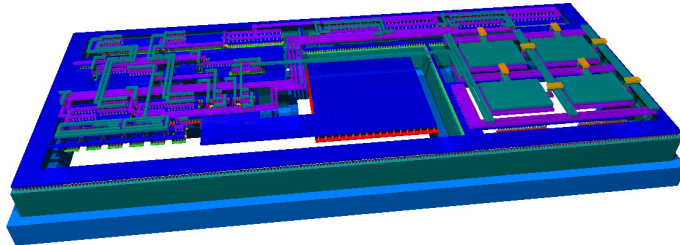
Hence, the formulæ for limit cycle determination and distortion prediction can be used to gain additional insight in the functioning of the circuit, depending on the nature of the loop components used and as a first guesstimate of the system parameters to reduce design time. This will not however obsolete the need for time consuming simulations on the device level for further optimization. It should also be noted that backannotation of the design parameters might lead to more accurate calculation results, although that should not be required anymore in an advanced design stage.

## References

- [1] Europractice IC service. (2007, Mar.) AMI Semiconductor I3T80 technology. [Online]. Available: [http://www.europractice-ic.com/docs/AMIS\\_datasheets/AMIS\\_I3T80U\\_V7.pdf](http://www.europractice-ic.com/docs/AMIS_datasheets/AMIS_I3T80U_V7.pdf)
- [2] K. R. Laker and W. M. C. Sansen, *Design of Analog Integrated Circuits and Systems*. McGraw-Hill, Inc., 1994.
- [3] J. Huijsing, *Operational Amplifiers, Theory and Design*. Kluwer Academic Publishers, 2001.
- [4] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. John Wiley & Sons, Inc., 2001.
- [5] R. Gregorian, *Introduction to CMOS OP-AMPs and Comparators*. John Wiley & Sons, Inc., 1999.
- [6] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*. Wiley-IEEE Press, 1998.
- [7] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. Oxford University Press, 2002.
- [8] J. M. Rabaey, A. Chandrakasan, and B. Nikolić, *Digital Integrated Circuits: a Design Perspective*, 2nd ed., C. G. Sodini, Ed. Prentice Hall, 2003.
- [9] A. B. Williams and F. J. Taylor, *Electronic Filter Design Handbook: LC, Active, and Digital Filters*, 2nd ed. McGraw-Hill, Inc., 1988.
- [10] E. Roza, "Analog-to-digital conversion via duty-cycle modulation," *IEEE Trans. Circuits Syst. II*, vol. 44, no. 11, pp. 907–914, Nov. 1997.
- [11] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, 3rd ed. McGraw-Hill, Inc., 2003.
- [12] J. J. Goedbloed, *Elektromagnetische Compatibiliteit: Analyse en Onderdrukking van Stoorproblemen*, 2nd ed. Ten Hagen Stam, 2000, in Dutch.

- [13] R. Morrison, *Grounding and Shielding Techniques in Instrumentation*. John Wiley & Sons, Inc., 1967.
- [14] A. Bicakci, C.-S. Kim, and S.-S. Lee, "A CMOS line driver for ADSL central office applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2201–2208, Dec. 2003.
- [15] F. Sabouri and R. Shariatdoust, "A 740mW ADSL line driver for central office with 75dB MTPR," in *ISSCC Digest of Technical Papers*, San Francisco, USA, Feb. 2002, pp. 322–323.





# 5

## Measurements

This chapter first describes some features of the chip layout and the test board to increase signal integrity. After these initial remarks, a first batch of measurement results is presented, together with the observed phenomena and the possible causes. In a next section, additional measurements are presented, resulting in some final recommendations.

### 5.1 Introduction

The circuit, as discussed in chapter 4, is processed in the I<sup>3</sup>T80 technology. Figure 5.1 gives the die photograph of this silicon implementation, where the five different implementations are easily distinguishable. The top circuit is the first order system, followed by the 10MHz second order amplifier, a highly symmetric second order system with independent loops, the 30MHz second order system and at the bottom the third order amplifier, each measuring approximately 2mm<sup>2</sup>.

Several blocks can be identified on the photograph. The rasterized structures at both sides are the DMOS output transistors, of which the widest on top is the PDMOS and the bottom one is the NDMOS. These are interconnected by wide metallic stripes with their respective bonding paths, being the 25V supply on top, the output in the middle and ground at the bottom. The interconnection is chosen that wide for electromigration reasons, since some measurements require large DC currents to flow through the output stage.

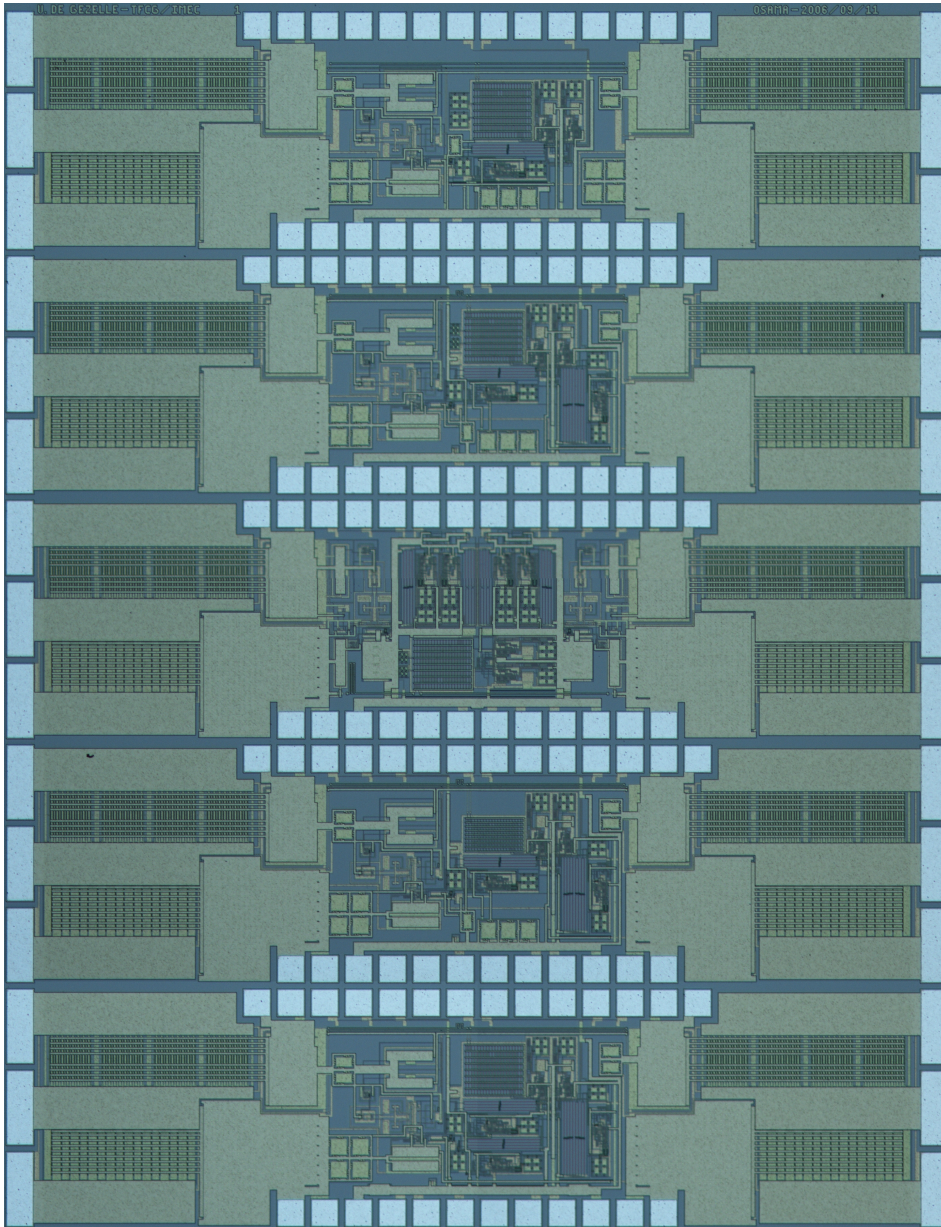


Figure 5.1: Die photograph of the amplifiers processed

The output transistors are controlled by large inverters, which are covered with overlapping power supply planes. Together with the power connections to the N-type epitaxial layer, forming the bulk of the low voltage buffer transistors and the ground connection to the P-type substrate around these structures, this creates a shield between the analogue and high power digital parts of the circuit.

On the bottom of each circuit, there also is a bar, formed by overlapping analogue power and ground tracks, creating a point of low impedance for distribution to the individual analogue building blocks.

To complete the measurements on the ASIC, a test board is designed, which is shown in Fig. 5.2. This board further implements the recommendations as given in section 4.9.

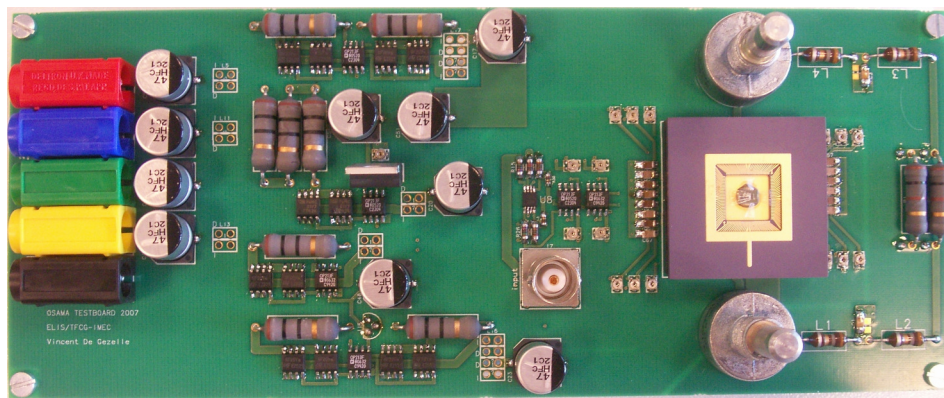


Figure 5.2: Photograph of the test board

Basically, the board is divided in three main parts. On the left side, there are the power connectors with decoupling capacitors, followed by a voltage reference circuit with current measuring capabilities and finally the ASIC socket with reference signals, output filter and input single ended to balanced converter.

In addition to the decoupling at the power input, additional large capacitors are placed at the voltage reference outputs and smaller capacitors at the supply lines of the analogue components and the DC voltage and current reference circuits of the chip, as close to the component of interest as possible.

Separate paths are provided for the analogue and digital supply lines, whereas a separate ground plane is used with cut outs to separate low voltage, high voltage, analogue and digital. These ground stripes closely follow the path of the corresponding supply line and are merged close to a common reference point of the power supply, or at the power connector otherwise. As such, capacitive interference, especially with analogue ground and power and current loops, caused by on-chip interaction between analogue and digital, can be reduced to a minimum.

The result is a design, where the components should not interfere significantly with each other or the environment in general. As an interesting side effect, this will automatically reduce the effect of environmental disturbances on the test circuit as well.

This chapter is further organized as follows. Section 5.2 gives the results of the first set of measurements performed on all five circuits. In section 5.3, the problems with the initial measurements are identified and explained and section 5.4 then presents the final measurements on the adjusted circuit.

## 5.2 Initial measurements

To characterize the circuits, several measurements need to be performed. Analogous to the simulations from chapter 4, the DC response will give a first impression of both linearity and power consumption. The next step are AC measurements, to compare the third order harmonic distortion with the predicted values from chapter 3 and the simulated values from chapter 4. The final step then is a full MTPR test, including measurement of the noise level without input signal.

### 5.2.1 First order system

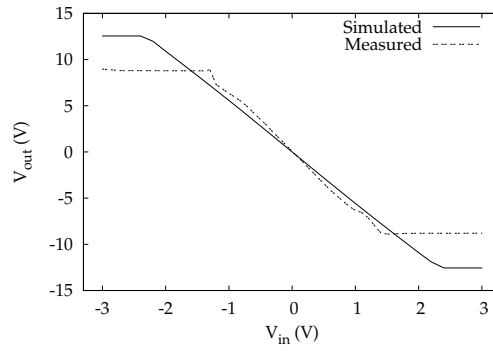
#### DC response

The simulated and measured response of the first order loop to a DC input voltage is given in Fig. 5.3. The transfer in Fig. 5.3a already shows reduced linearity compared to the simulations. Additionally, the output voltage saturates at  $\pm 9V$  instead of the simulated  $\pm 12.5V$ , even when the external matching resistor is completely shorted.

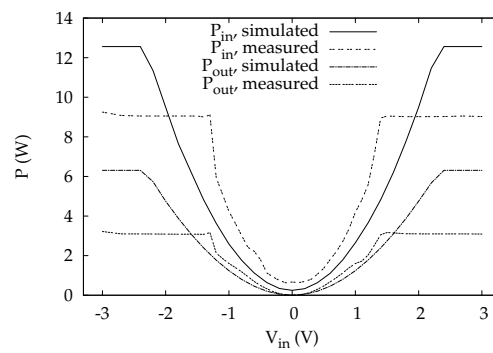
Due to the early saturation, the maximum output power is about half the simulated value. The minimum input power is found to be 670mW, which also is significantly higher than the 245mW simulated. Since xDSL signals have a Gaussian distribution (2.28), this elevated idle power will drastically reduce the overall efficiency. The final result is an amplifier with an estimated efficiency of 12.82% according to equation (2.27).

#### AC response

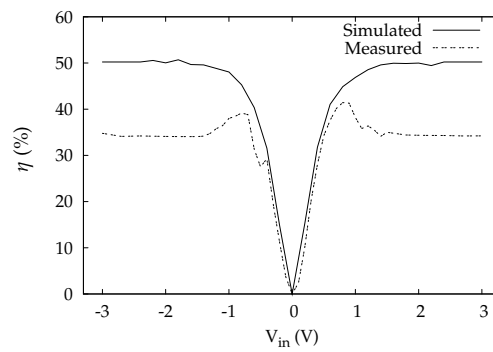
The results of the distortion measurements are shown in Fig. 5.4, again at 200kHz, 500kHz and 1MHz, together with the calculated and simulated results. As with the DC measurements, there is a significant difference between simulation and measurements, except at higher signal amplitudes.



(a) DC transfer

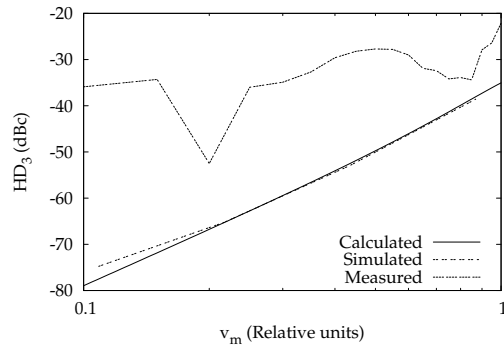


(b) Input and output power

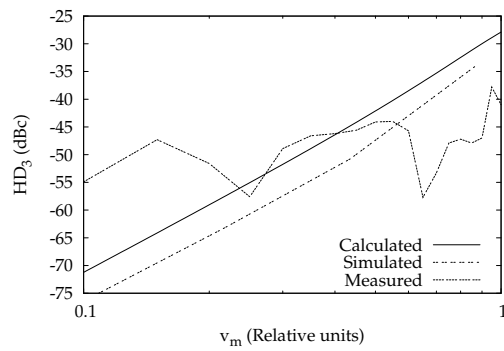


(c) DC efficiency

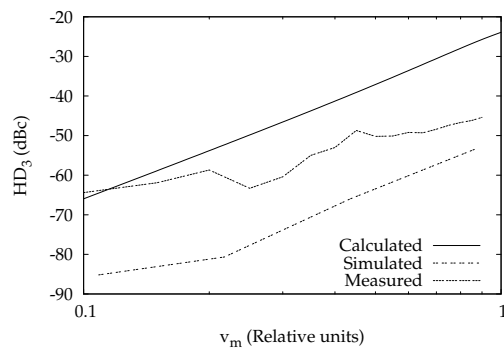
Figure 5.3: DC measurements on the first order system



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.4: Third order harmonic distortion of the first order system

## 5.2 Initial measurements

157

### MTPR response

The first set of measurements regarding the MTPR, is the noise floor of the idle amplifier, which should be below  $-100\text{dBm/Hz}$  in the band up to  $10\text{MHz}$  [1], [2], [3]. Fig. 5.5a shows the noise spectrum of the idle amplifier, Fig. 5.5b the noise spectrum of the spectrum analyzer and Fig. 5.5c the noise of the bias power supply unit (PSU) used.

From this last measurement, it becomes clear that the PSU will already cause some modulation of the amplifier, which is confirmed by the peak around the same frequency in Fig. 5.5a. Also the fundamental and second harmonic are clearly distinguishable at a frequency of  $4.2\text{MHz}$  instead of the simulated  $6\text{MHz}$ . Starting at about  $5\text{MHz}$ , the noise floor drops to that of the spectrum analyzer.

The global result of these measurements is that, apart from the PSU induced contribution and the limit cycle frequency, the system is expected to comply with the noise specifications.

The result of the MTPR measurements is given in Fig. 5.6, for a total signal power of  $0\text{dBm}$ ,  $11.5\text{dBm}$  and  $20\text{dBm}$ . For the two lowest transmit powers, the MTPR is approximately  $45\text{dB}$ , while at full power this decreases to about  $30\text{dB}$  with peaks down to  $25\text{dB}$ . This also is worse than outlined in table 3.3.

### 5.2.2 10MHz second order system

#### DC response

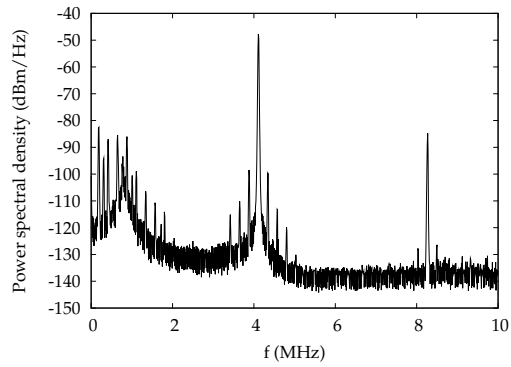
Figure 5.7 shows the results of the DC measurements on the  $10\text{MHz}$  second order amplifier, up to the verge of saturation. As with the first order system, the output range is more limited than simulated. The linearity also is worse, but already seems better than the first order system transfer from Fig. 5.3a. The efficiency from Fig. 5.7c also has the wider "valley" and a maximum value of about  $35\%$ . As for the minimum input power, the situation is even worse, with a minimum dissipation of  $787\text{mW}$ , leading to an estimated MTPR efficiency of  $10.50\%$ .

#### AC response

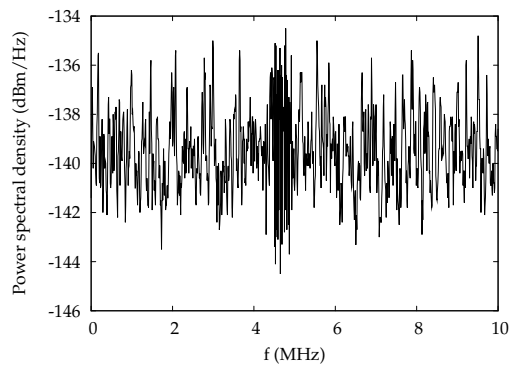
The distortion measurements are presented in Fig. 5.8. Although the simulations corresponded quite well with the calculations, there is a significant difference with the measurements.

#### MTPR response

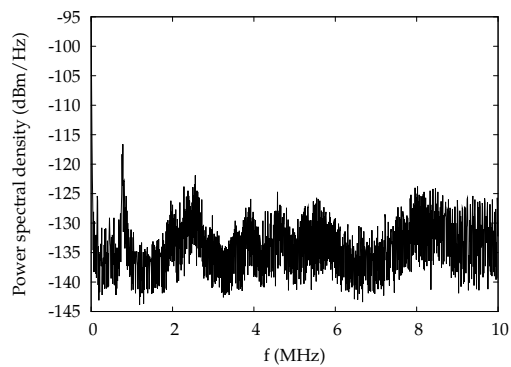
The noise measurement from Fig. 5.9 shows a small bump at approximately  $2\text{MHz}$ , in addition to the PSU contribution at  $800\text{kHz}$ . This small peak is at-



(a) Noise of the amplifier



(b) Noise floor of the spectrum analyzer



(c) Noise of the bias PSU

Figure 5.5: Noise measurements on the first order system



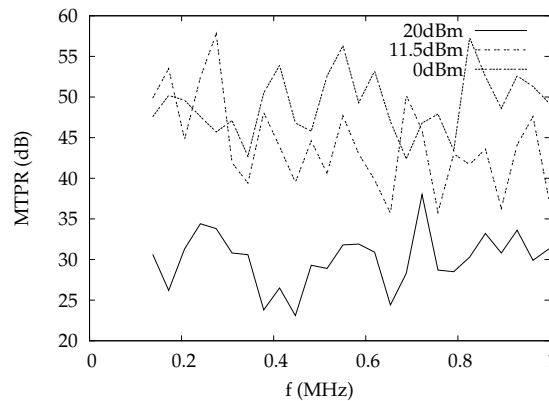


Figure 5.6: MTPR measurements on the first order system

tributed to the ripple in the transfer characteristic of the third order Chebychev output filter. This was not visible with the first order loop, due to the PSU contribution, being close to the lower filter cut-off frequency of 1.5MHz.

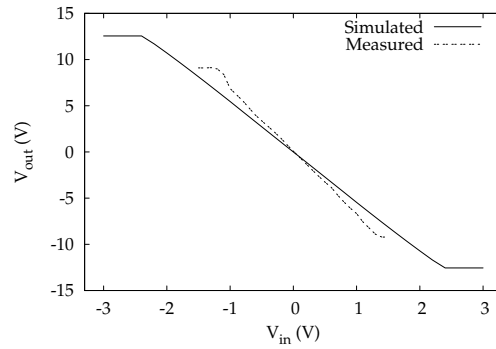
The limit cycle frequency is 5.8MHz instead of the simulated 10MHz. Starting at about 3MHz and making abstraction of the peak at the oscillating frequency, the noise contribution stays well below the specified -100dBm/Hz.

Due to the increased limit cycle frequency and cut-off frequency of the output filter, the MTPR measurements are performed with a full rate ADSL2+ input signal, spanning the band from 138kHz to 2.208MHz. The resulting MTPR figure is given in Fig. 5.10, showing 45dB for the 0dBm signal, decreasing to 25dB for the 11.5dBm signal and 20dB for the full power output. This again is not the expected value of 52dB from table 3.3.

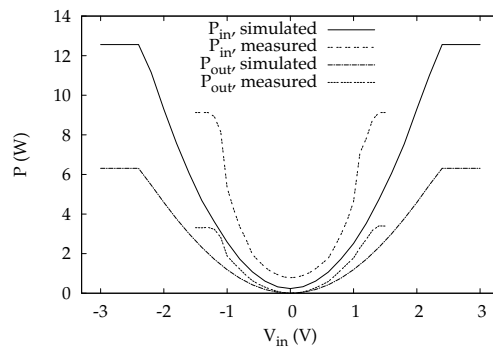
### 5.2.3 30MHz second order system

#### DC response

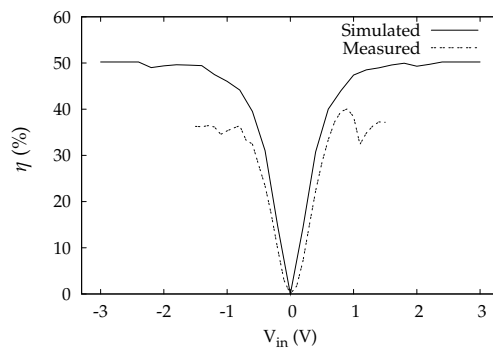
The DC response is shown in Fig. 5.11, again until saturation sets in. When comparing the linearity measurements from Fig. 5.11a with those for the 10MHz second order system in Fig. 5.7a, the distortion is expected to be worse due to the more pronounced non-linearity. The minimum output power, however, is slightly lower at 725mW, leading to an efficiency estimate of 10.38%. The maximum DC efficiency is limited to about 37%.



(a) DC transfer

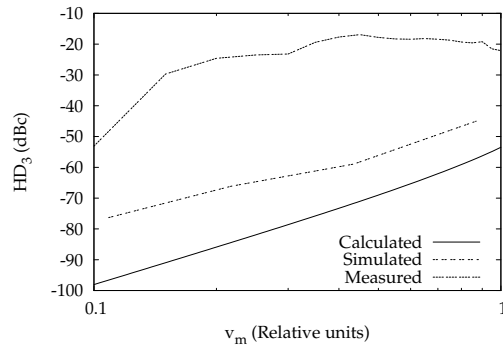


(b) Input and output power

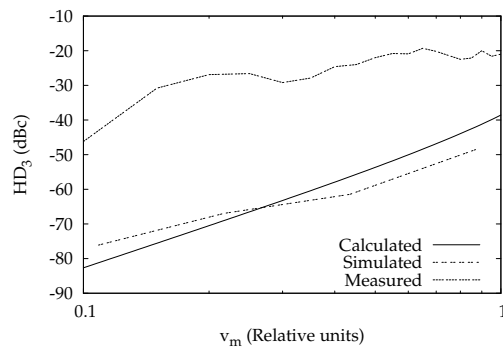


(c) DC efficiency

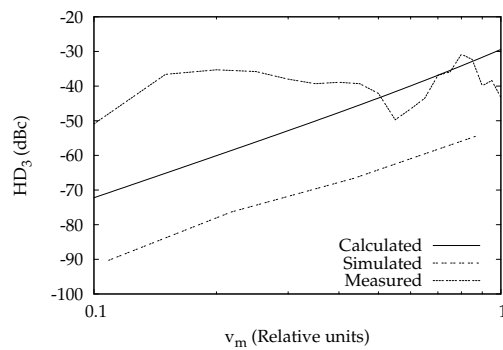
Figure 5.7: DC measurements on the 10MHz second order system



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.8: Third order harmonic distortion of the 10MHz second order system

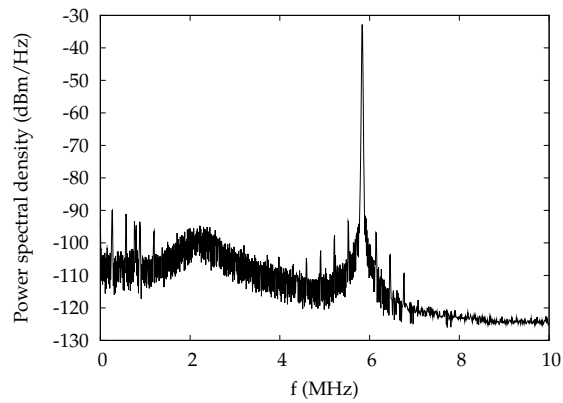


Figure 5.9: Noise measurement on the 10MHz second order system

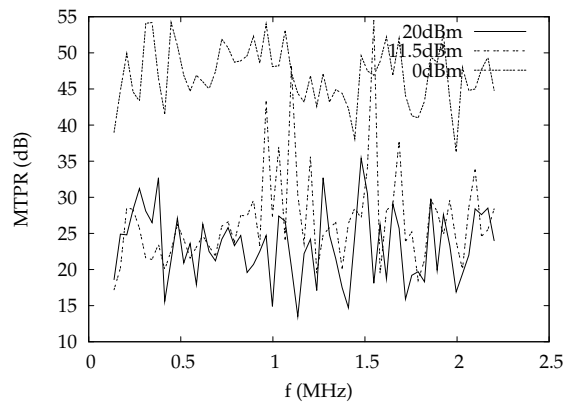
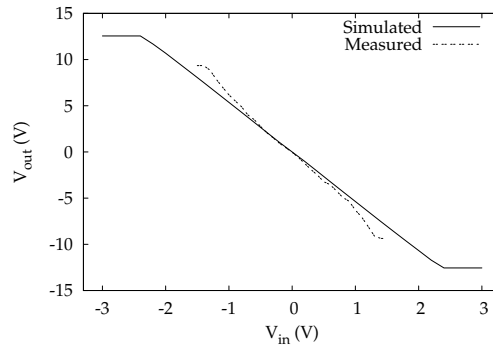
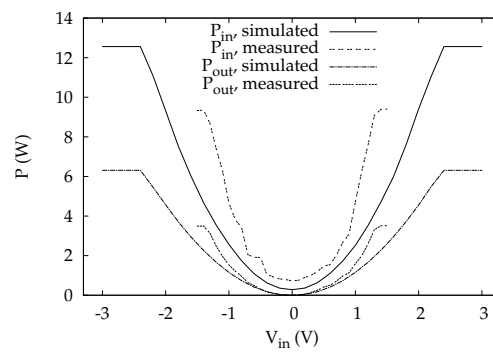


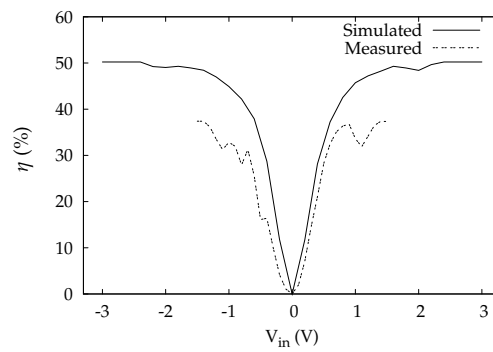
Figure 5.10: MTPR measurements on the 10MHz second order system



(a) DC transfer



(b) Input and output power



(c) DC efficiency

Figure 5.11: DC measurements on the 30MHz second order system

### AC response

The distortion, as illustrated in Fig. 5.12, in general is higher than simulated, as already deduced from the DC linearity measurements. The only correspondence with the simulations is at high input frequencies with a low amplitude.

### MTPR response

The noise measurement in Fig. 5.13 exhibits similar behaviour as before, showing the PSU contribution and the output filter transfer characteristic. The limit cycle frequency is about 9.6MHz instead of the simulated 17MHz.

The corresponding MTPR measurements are given in Fig. 5.14, leading to about 30dB overall, compared to the simulated 54dB.

## 5.2.4 Third order system

### DC response

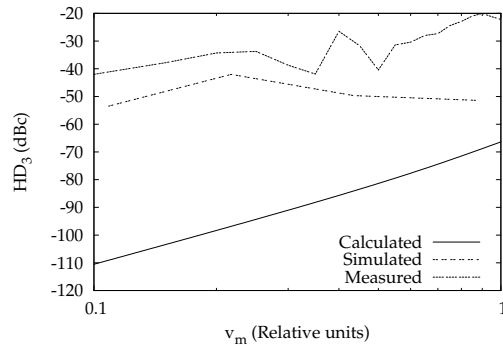
The results from the DC measurements, as given in Fig. 5.15, are not complete, due to destructive overheating of the output stage at higher output amplitudes. The minimum input power is 1.31W, which explains the overheating. Due to the limited measurement, only a rough estimate of the MTPR efficiency is made, leading to 6.75%.

### AC response

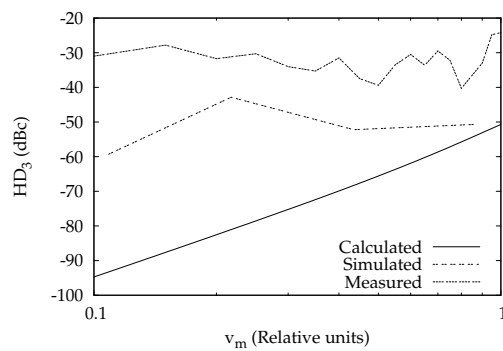
The linearity of the third order system is measured with the 1.5MHz output filter for reasons that will be explained in the next section. The results are given in Fig. 5.16, leading to a higher distortion at low frequencies, but converging to the simulation results at higher frequencies.

### MTPR response

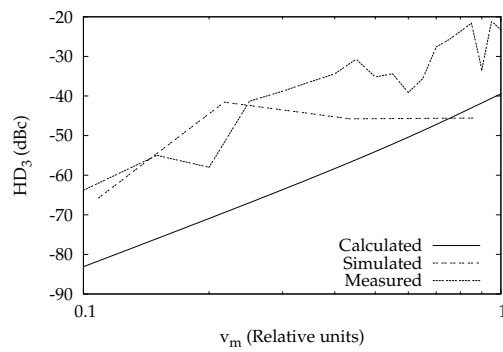
The noise measurements are presented in Fig. 5.17, for both a 2.5MHz and 1.5MHz output filter cut-off frequency. This clearly shows the existence of a subharmonic frequency of the 4.7MHz limit cycle frequency. Using the 1.5MHz output filter, the subharmonic is removed, but there still are a lot of spurious components around the 4.1MHz oscillating frequency. This change in limit cycle frequency is caused by the increased influence of the output transistors on the entire loop, due to their higher output impedance. Both values also are significantly lower than the simulated 10MHz.



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.12: Third order harmonic distortion of the 30MHz second order system

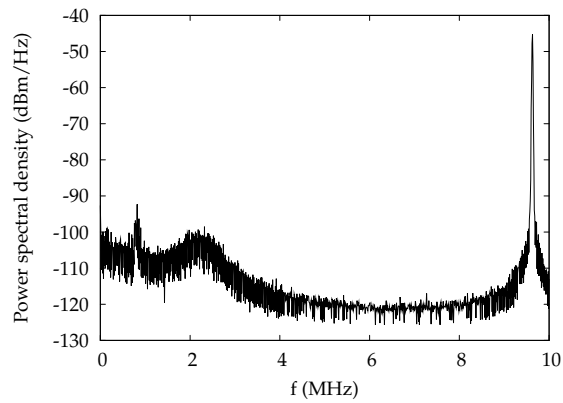


Figure 5.13: Noise measurement on the 30MHz second order system

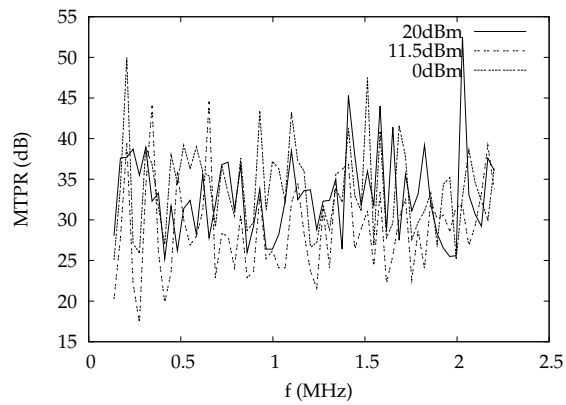
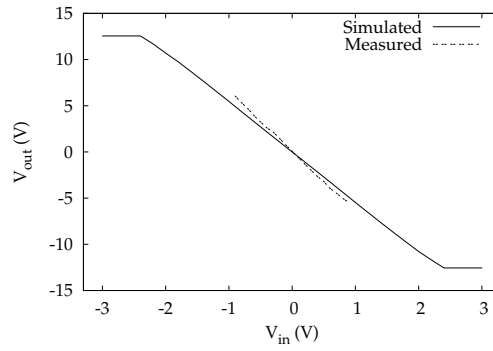
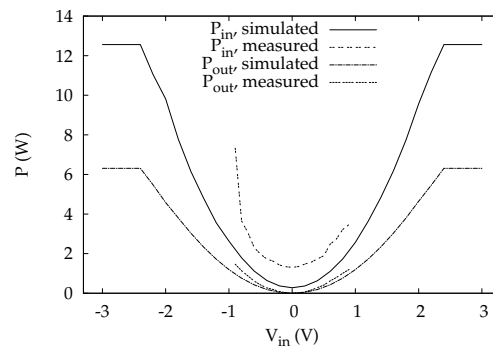


Figure 5.14: MTPR measurements on the 30MHz second order system

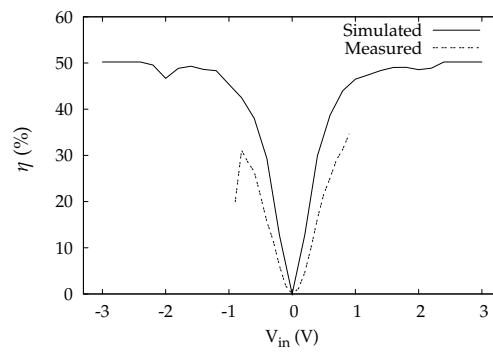




(a) DC transfer

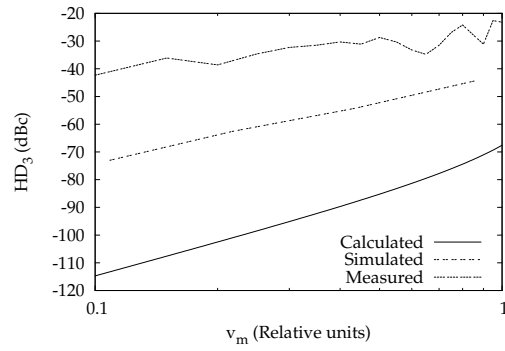


(b) Input and output power

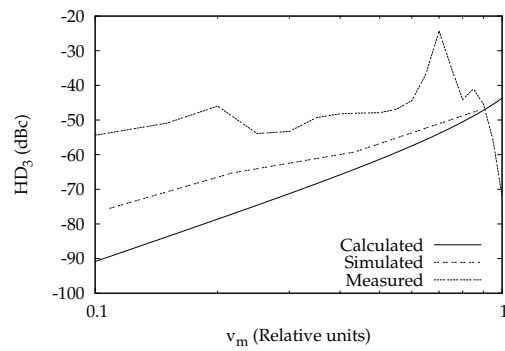


(c) DC efficiency

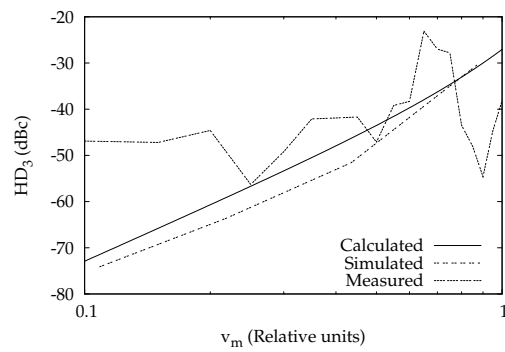
Figure 5.15: DC measurements on the third order system



(a) 200kHz input sine wave

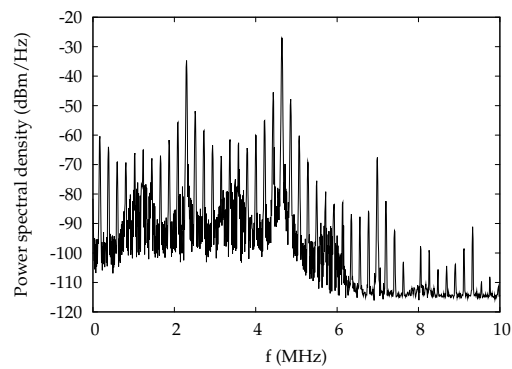


(b) 500kHz input sine wave

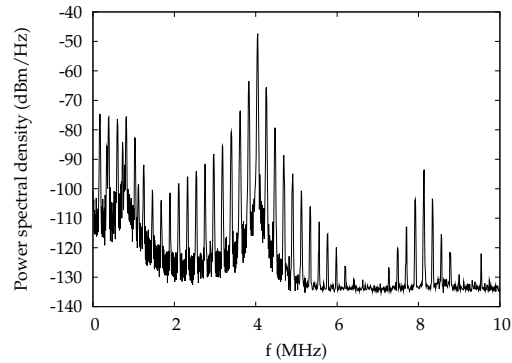


(c) 1MHz input sine wave

Figure 5.16: Third order harmonic distortion of the third order system



(a) Noise of the amplifier, 2.5MHz LPF



(b) Noise of the amplifier, 1.5MHz LPF

Figure 5.17: Noise measurements on the third order system

The results of the MTPR measurements are given in Fig. 5.18, ranging from 35dB for 0dBm output power down to 25dB for full power. The simulated value from table 3.3 was 57dB.

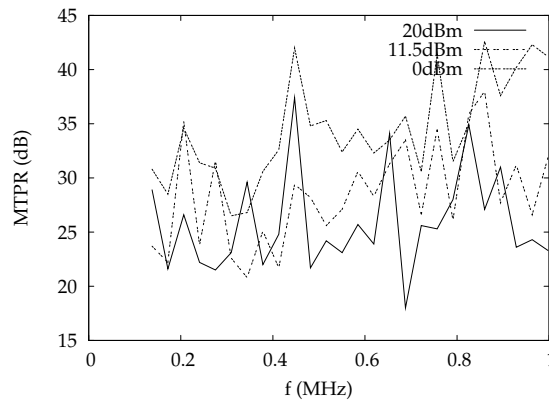


Figure 5.18: MTPR measurements on the third order system

## 5.2.5 Second order system with independent loops

### DC response

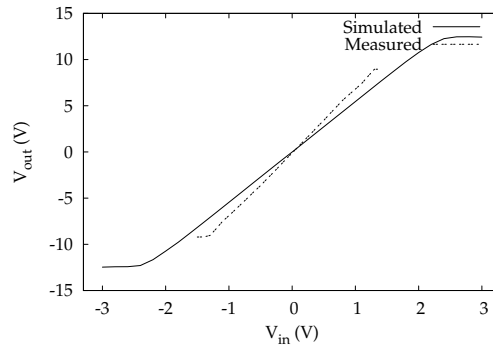
The last circuit is the 10MHz second order system with independent loops. The DC transfers are given in Fig. 5.19, again up to the verge of saturation. The results are comparable to those of the single loop 10MHz second order system, with a minimum of 720mW input power. This leads to an efficiency estimate of 11.35%.

### AC response

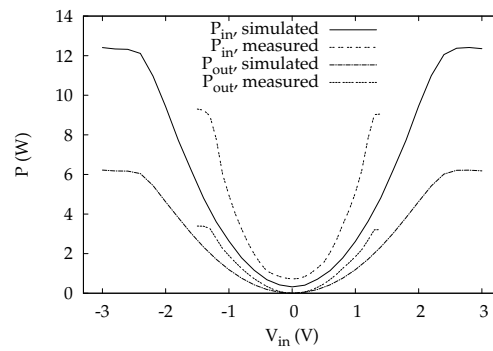
The third order harmonic distortion is illustrated in Fig. 5.20. Compared to the single loop 10MHz second order circuit, there is a slightly better correspondence between simulations and measurements.

### MTPR response

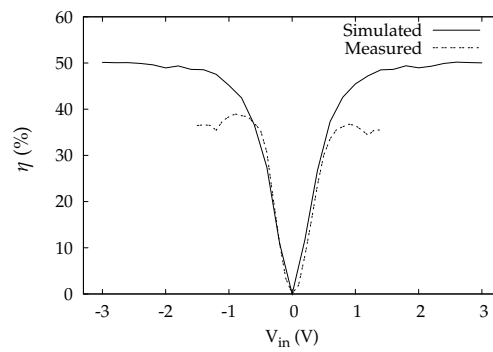
The noise floor of the amplifier is given in Fig. 5.21, again showing the PSU noise and the contribution of the output filter. The limit cycle frequency is 5.9MHz instead of the simulated 10MHz.



(a) DC transfer

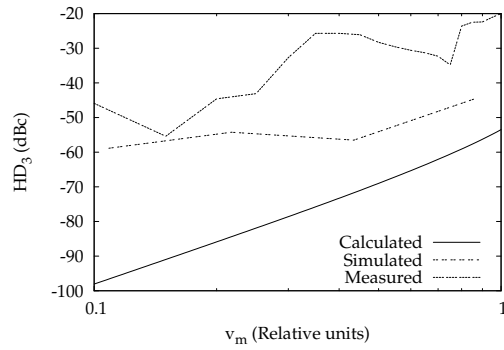


(b) Input and output power

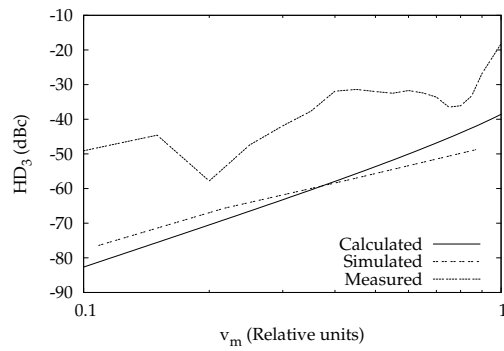


(c) DC efficiency

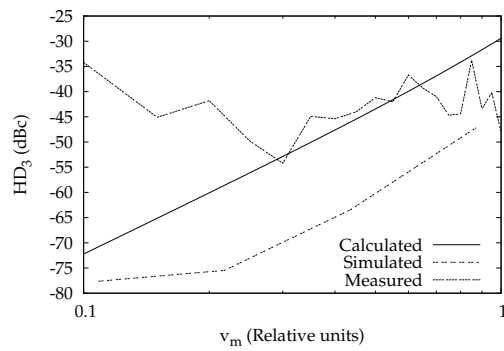
Figure 5.19: DC measurements on the second order system with independent loops



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

**Figure 5.20:** Third order harmonic distortion of the second order system with independent loops

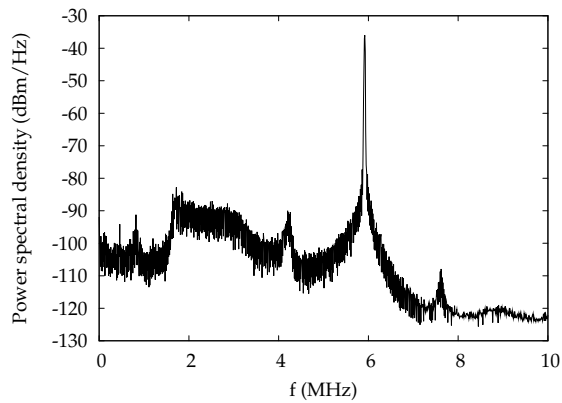


Figure 5.21: Noise measurement on the second order system with independent loops

The MTPR for low output powers, as illustrated in Fig. 5.22, is about 35dB, decreasing to 25dB at full power, which is comparable to the results of the other second order system.

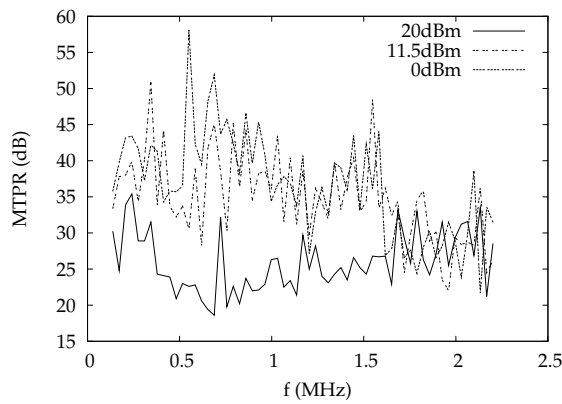


Figure 5.22: MTPR measurements on the second order system with independent loops

### 5.3 Troubleshooting

From the measurements in the previous section, it is clear there are some serious discrepancies between the simulated and processed circuits.

A first indication stems from the observation that correct start-up of the oscillator

**Table 5.1:** Maximum saturation voltage at process corners

Temperature	Minimum	Typical	Maximum
27°C	13.89V	15.27V	16.15V
125°C	11.30V	12.69V	13.97V

requires a very specific procedure, involving a specific input signal with a precise common mode voltage, applied at the correct moment, when ramping up the 25V supply voltage. To make matters worse, this procedure even depends on the device under test.

Secondly, the high idle power consumption suggests an overlap between the on times of the NDMOS and PDMOS output transistors. This can be caused by several factors, such as layout parasitics, difference in length of the signal paths, operating temperature and process corners. In addition, the low value of the turn-on delay, as simulated in Fig. 4.16, limits the acceptable tolerance.

Due to the complexity of the layout, simulations including the extracted parasitics were not possible. The increased dissipation of the circuit however implies an increase in operating temperature, resulting in a lower mobility and higher resistance of the active components, depending on the temperature gradient. The specs from the processing run also showed some of the parameters of the DMOS transistors being worst case, thus further increasing the signal delay.

Furthermore, in addition to the third order harmonic distortion, the amplifier also generates second order harmonic distortion, which is caused by the slightly different path length from comparator and level shifter to the corresponding output buffers.

The last observation is the significant difference between the maximum output voltage from the simulations, including some external matching resistance and the measurements without matching resistance. Using the circuit from Fig. 5.23a, the minimum saturation voltage over the load resistor can be determined, which can be reduced by inserting extra matching resistors if required. Table 5.1 gives an overview of these voltages at temperatures of 27°C and 125°C. This indicates the elevated temperature might cause the minimum saturation voltage to drop below the minimum requirement of 12.5V. There is, however, no indication of a drop below 9V as measured on all circuits.

Using a value of 9V for the maximum output voltage, the total resistance of the PDMOS and NDMOS output transistors together is 44.5Ω. To simulate the behaviour of the circuit with this increased output resistance, a 12.5Ω resistor is placed in series with the drain of the output transistors, which was the maximum value allowing for a converging simulation. Again using the circuit from Fig. 5.23a, the voltage over the "new" NDMOS is 7.54V and over the PDMOS 7.58V, resulting in a maximum output voltage of 9.88V at 27°C.



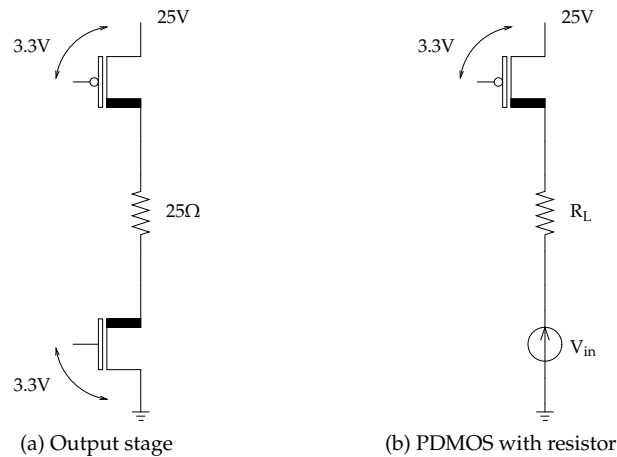


Figure 5.23: Schematics for worst case simulations and PDMOS transistor measurements

Distortion simulations on the 10MHz second order system using this series resistor also suggest this results in an increase of the third order harmonic distortion of about 20dB. As a result, at least part of the discrepancy between simulated and measured distortion levels can be attributed to the increased output resistance.

The primordial question now is the origin of this increased resistance. Using the circuit from Fig. 5.23b, this resistance can be simulated as a function of the drain-source voltage and temperature. The resistor  $R_L$  is included to limit this drain-source voltage to the maximum achievable in the full circuit when supposing an ideal, lossless NDMOS transistor.

Figures 5.24, 5.25 and 5.26 show the resulting curves for a typical and two worst case simulations at 27°C and 125°C for the full 6400μm wide PDMOS with 25Ω load and the 50μm wide reference transistor, which is to be repeated 128 times in parallel to form this full output PDMOS. To keep both simulations equivalent,  $R_L$  is scaled up according to the ratio of the total width of both devices. The resulting difference in resistance scale then again is compensated according to this ratio.

As could be expected from the previous simulations on the full output stage, the results of the 6400μm wide PDMOS do not suggest a significant difference in output resistance as compared with the 50μm reference PDMOS, except for the worst case corner in Fig. 5.25. However, the results in Fig. 5.27 of TCAD simulations on the device level under nominal processing conditions, using the 50μm device, already point in the direction of an underestimation of this resistance.

To finally confirm these simulations, the results of measurements on discrete transistors, processed in the same AMIS I<sup>3</sup>T80 0.35μm technology, are presented in Fig. 5.28 for a 80μm wide PDMOS and Fig. 5.29 for a 4818μm wide PDMOS. The

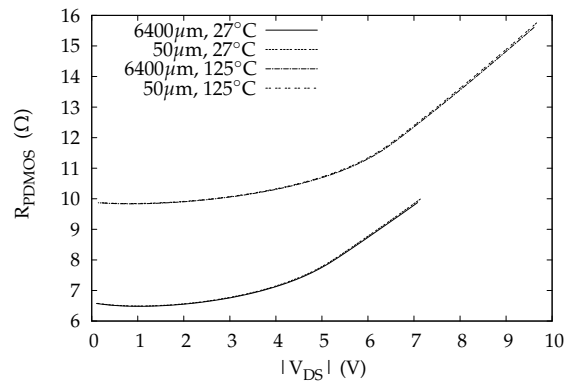


Figure 5.24: Resistance of the PDMOS, spice simulation, typical

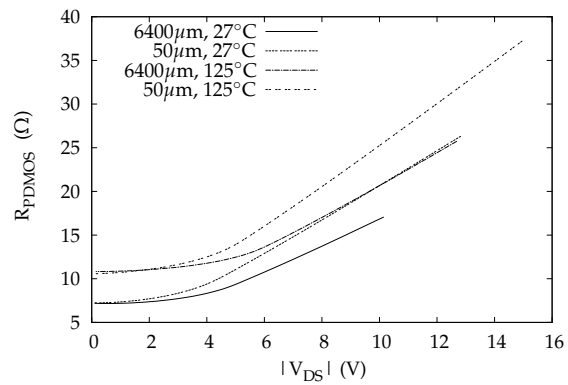


Figure 5.25: Resistance of the PDMOS, spice simulation, worst case 1

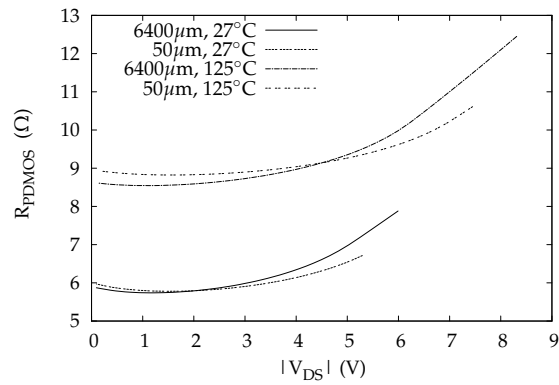


Figure 5.26: Resistance of the PDMOS, spice simulation, worst case 2

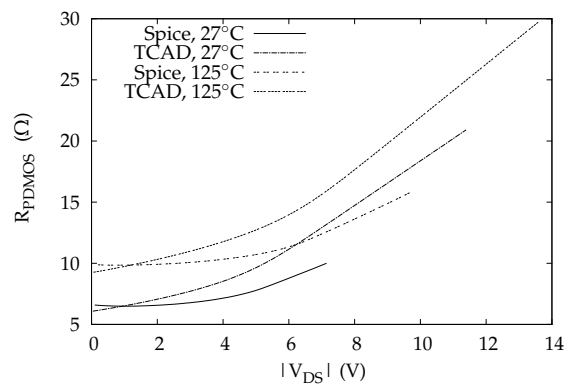


Figure 5.27: Resistance of the PDMOS, comparison of spice and TCAD simulations

resulting impedance, again, is compensated to reflect an estimate of the  $6400\mu\text{m}$  wide PDMOS from all circuits implemented and compared to the extremes, resulting from worst case Spice simulations on devices with exactly the same parameters.

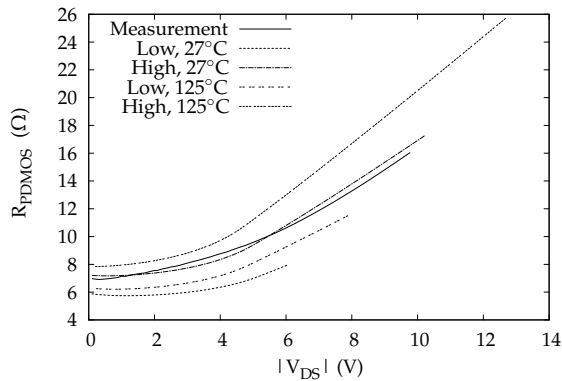


Figure 5.28: Measured resistance of a  $80\mu\text{m}$  PDMOS

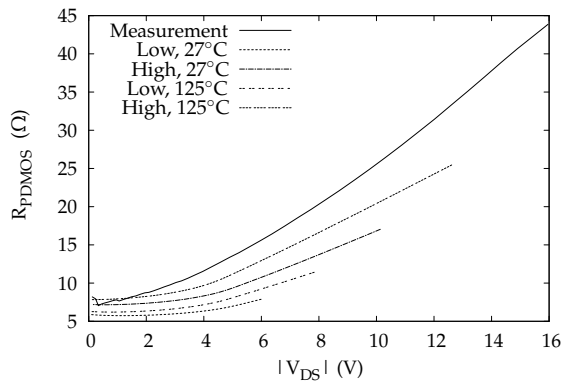


Figure 5.29: Measured resistance of a  $4818\mu\text{m}$  PDMOS

The measurements on the  $80\mu\text{m}$  PDMOS tend to comply with the most high impedance corner of the  $27^\circ\text{C}$  simulations. Due to the low power dissipation in this small device, only a slight local increase in temperature is expected, which can be dispersed immediately by the surrounding, unused, silicon and the contacting metal layers.

For the  $4818\mu\text{m}$  wide PDMOS however, the results in Fig. 5.29 speak for them-

### 5.3 Troubleshooting

179

selves. In this case, due to the large silicon area in use, the power dissipated in the device will not be drained as efficiently as with the  $80\mu\text{m}$  PDMOS, thus self heating will play an important role in device performance. The temperature, as measured at the metal sealing the device package, is given in Fig. 5.30. This clearly shows an increase in temperature with increasing drain-source voltage, due to this self heating. These temperature values however only illustrate the temperature tendency and not the exact temperature of the device itself, since this would require knowledge of the thermal resistance of the entire chip and package, the influence of heat convection at the package-air interface and radiated heat.

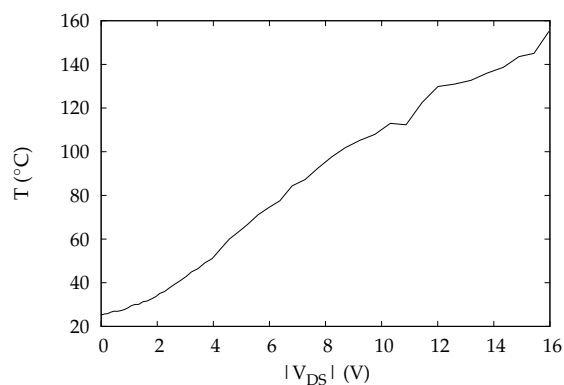


Figure 5.30: Temperature of the  $4818\mu\text{m}$  PDMOS package seal

Combination of Fig. 5.29 and 5.30 now leads to two conclusions.

First of all, it is remarkable that drain-source voltages of over  $1.5\text{V}$  already lead to a higher measured impedance than could be expected even from the worst simulated impedance at  $125^\circ\text{C}$ , while the package temperature is not indicating a significantly increased temperature yet.

Secondly, when looking at drain-source voltages of  $8\text{--}9\text{V}$ , which is the measured operating region of the amplifier output PDMOS transistors, the expected rescaled impedance is between  $20\Omega$  and  $25\Omega$ , which confirms the impedance estimation of  $44.5\Omega$  at page 174, when supposing similar impedance levels of both NDMOS and PDMOS transistors. The case temperature for this voltage region is around  $100^\circ\text{C}$ , indicating a silicon temperature that might even exceed  $125^\circ\text{C}$ .

The general conclusion to be drawn from these simulations and measurements, is the serious deterioration in performance of the output stage, which, due to self heating, will further impact the functioning of the control circuits. Since this self heating will also cause a temperature gradient depending on the oscillating frequency and the corresponding duty cycle and on time of the output transistors, the full extent of this effect can not readily be quantified by simulations.

To verify this conclusion in a definite way, new measurements can be performed, using a higher load impedance and modified output filter, according to this termination impedance. These results will be given in the next section.

## 5.4 Final measurements

A first important observation of the additional measurements with double load, is the much simpler procedure to start up all five systems. No special tricks with the input signal and high voltage supply are required, since the amplifiers were even verified to work correctly when the voltage supplies were switched on at nominal voltage directly, if applied in the correct order that is.

Additionally, a spectral measurement of the limit cycle peak gives an indication of a more stable oscillation. When comparing the peak with  $25\Omega$  load for the 30MHz second order loop from Fig. 5.31 with that in Fig. 5.32 for the  $50\Omega$  load, it is clear that the amount of phase noise already is much reduced.

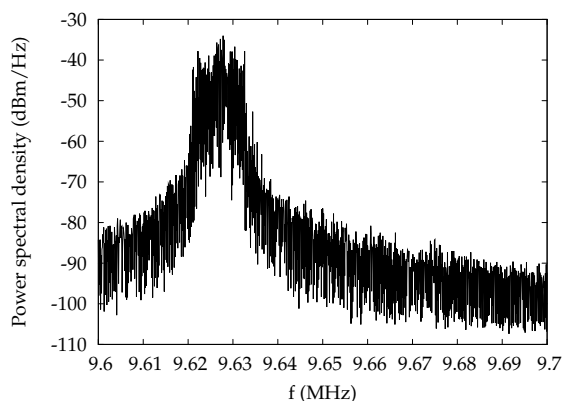


Figure 5.31: Oscillating frequency detail,  $25\Omega$  load, 30MHz second order loop

Further differences, depending on the implementation, will be discussed in the next sections.

The  $50\Omega$  measurements will still be compared with the  $25\Omega$  simulation results, as the load increase serves to more closely match the simulation conditions. This also means that the measured input and output power should be half that of the simulations, which are still included as such in the graphs, mainly to allow for comparison of shape and idle power.

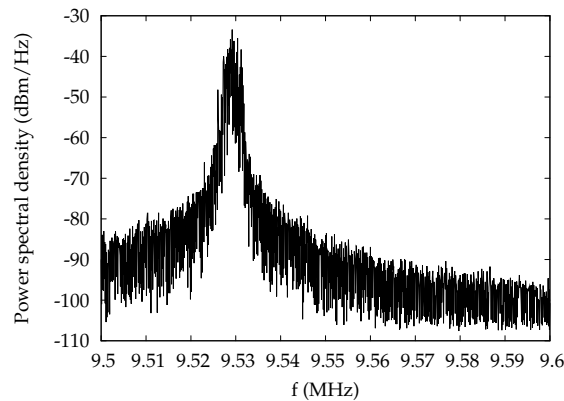


Figure 5.32: Oscillating frequency detail, 50Ω load, 30MHz second order loop

### 5.4.1 First order system

#### DC response

The DC transfer functions are given in Fig. 5.33, resulting in an improved output voltage range and a seemingly less distorted input output relation. Also, the maximum achievable efficiency is greatly improved and the minimum input power is reduced by over 100mW to 560mW. This results in an expected efficiency of 7.08%.

The main reason for this low value, is the reduced output power delivered into the double load impedance. Measurements, using a 50mW total output power, yield 7.69%, whereas a full power measurement, violating the crest factor requirement, leads to 13.28%.

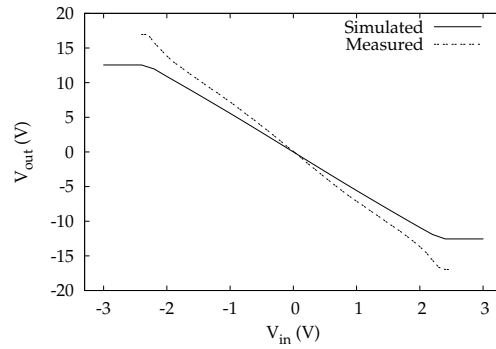
#### AC response

The results of the AC measurements are presented in Fig. 5.34. The main conclusion to be drawn, is a significant reduction in distortion, even down to the simulated level in the 500kHz case.

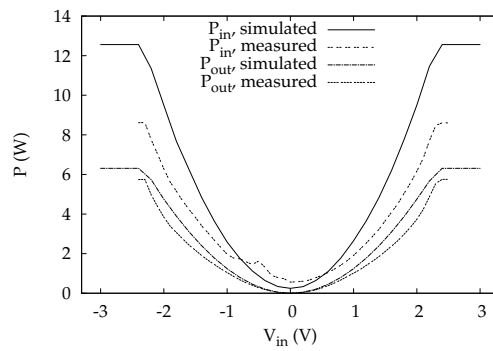
#### MTPR response

The noise measurement, as illustrated in Fig. 5.35, closely resembles that from Fig. 5.5, except for the reduced power dissipated in the side lobes of the limit cycle frequency.

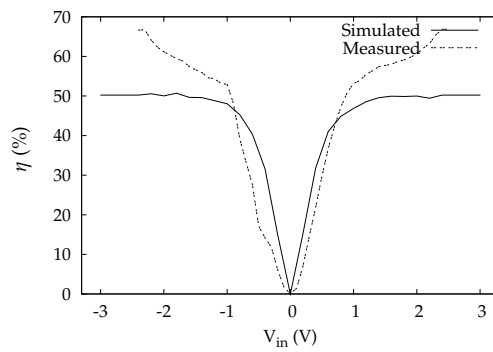
As could be expected from the distortion measurements, the MTPR also is in-



(a) DC transfer



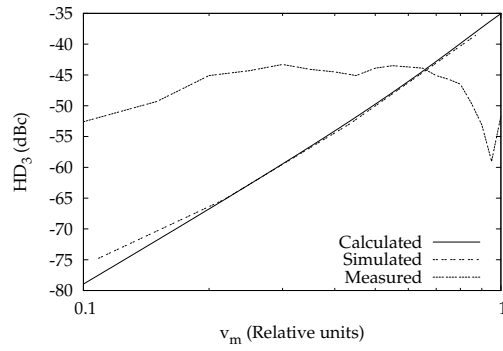
(b) Input and output power



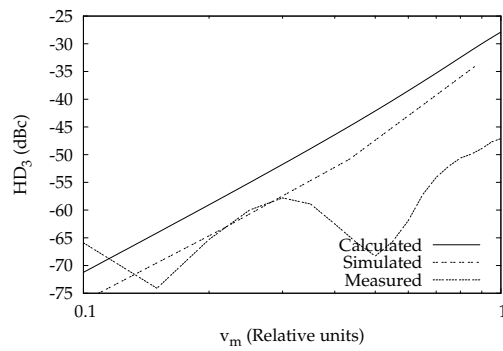
(c) DC efficiency

Figure 5.33: DC measurements on the first order system

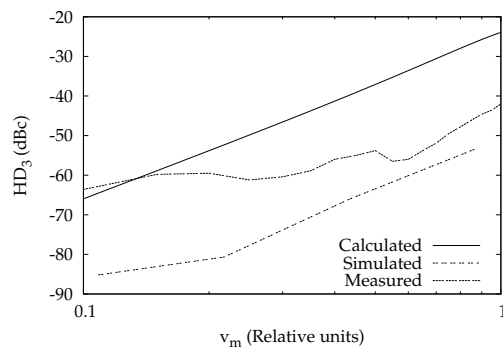




(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.34: Third order harmonic distortion of the first order system

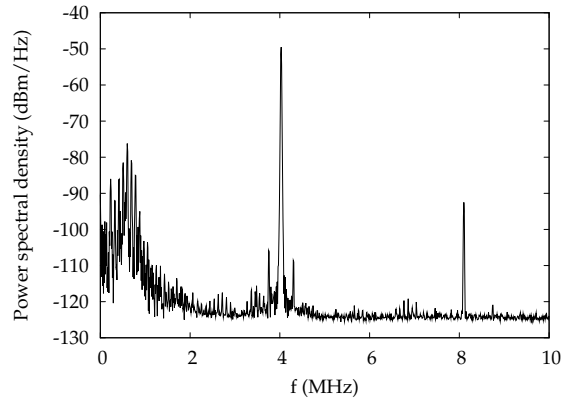


Figure 5.35: Noise measurement on the first order system

created. Fig. 5.36 shows the results for -3dBm, 8.5dBm and 17dBm, showing values of over 45dB at low power, to more than 30dB for the half power output, resulting in an increase of about 5dB.

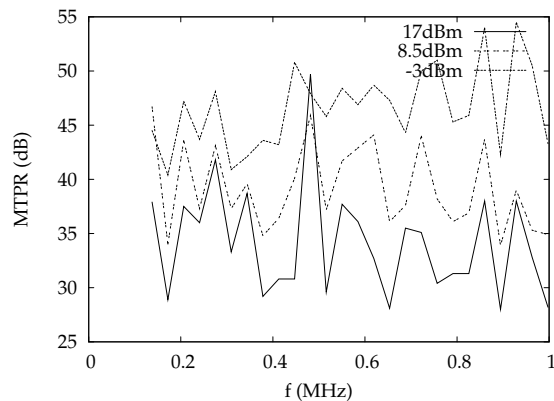


Figure 5.36: MTPR measurements on the first order system

## 5.4.2 10MHz second order system

### DC response

Also the 10MHz second order system shows a much improved linearity, as can be seen in Fig. 5.37a. This, again, is expected to result in a reduced third order harmonic distortion.

The minimum power dissipation, however, is increased to 900mW, resulting in an estimated 4.98% efficiency. This is verified by a measured 5.22% efficiency, increasing to 9.01% for a 20dBm output signal.

#### AC response

As with the first order system, the distortion is found to be 10 to 20dB lower than with the original full load circuit, although this is still higher than simulated. All results are shown in Fig. 5.38.

#### MTPR response

The noise, as given in Fig. 5.39, is comparable to the initial measurements, showing the PSU and filter contributions. The side lobes can be attributed to a low frequency disturbance, picked up at the input of the amplifier.

The results of the MTPR measurements are shown in Fig. 5.40. At -3dBm output power, this is comparable to the 0dBm curve from Fig. 5.10. However, at 8.5dBm and 17dBm, there is an increase of about 10dB.

### 5.4.3 30MHz second order system

#### DC response

Figure 5.41 gives the results of the DC measurements on the high frequent second order loop. Again, there is better correspondence with the simulated transfer, although this seems less linear in general.

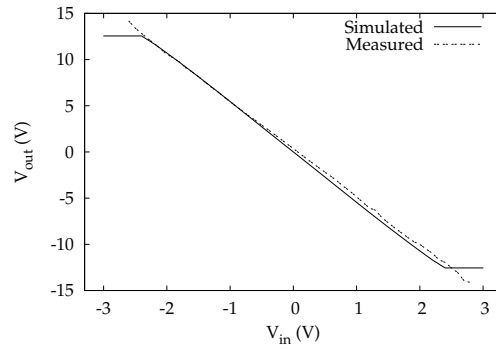
The minimum measured input power is 950mW, again an increase compared to the first set of measurements. This results in an estimated 4.16% efficiency, which is verified to be 4.08% at 17dBm output power. The full 20dBm leads to 7.62%.

#### AC response

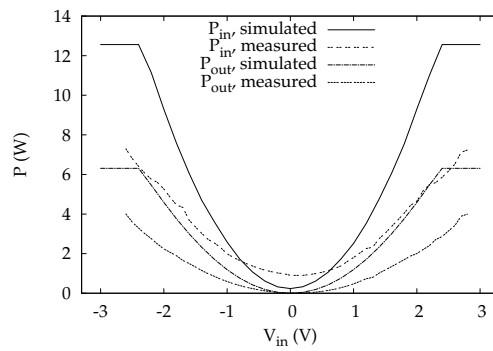
The third order harmonic distortion, as illustrated in Fig. 5.42, shows a slight increase of linearity of up to 10dB as compared to Fig. 5.12. Due to the “bumps”, visible in Fig. 5.41a, this confirms the expectations.

#### MTPR response

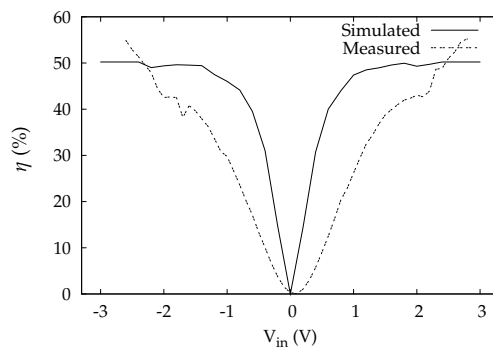
The noise floor from Fig. 5.43 again shows the PSU contribution and the output filter transfer and is otherwise equivalent to Fig. 5.13.



(a) DC transfer

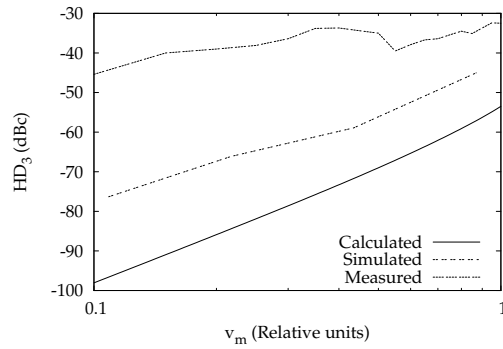


(b) Input and output power

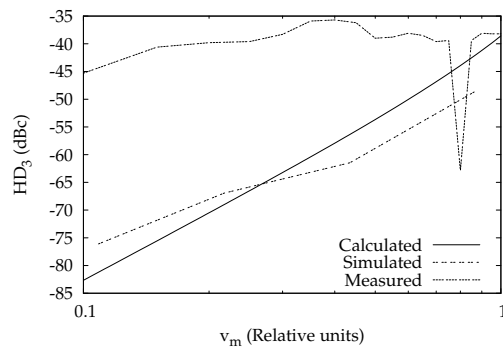


(c) DC efficiency

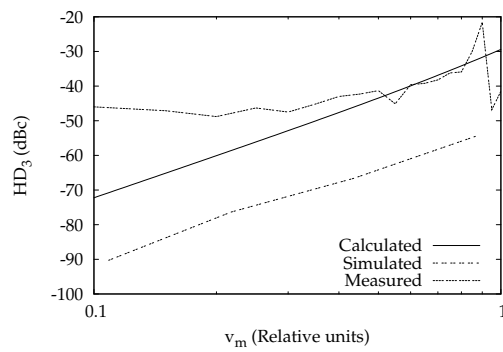
Figure 5.37: DC measurements on the 10MHz second order system



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.38: Third order harmonic distortion of the 10MHz second order system

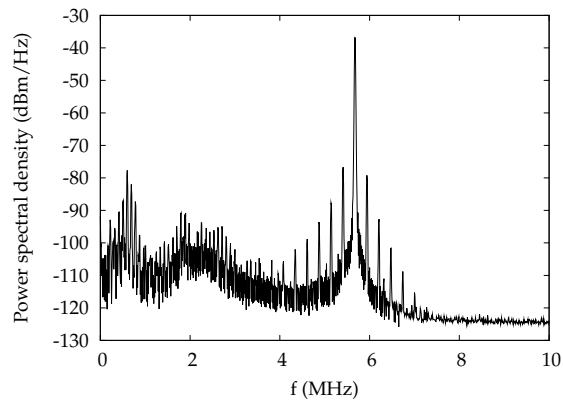


Figure 5.39: Noise measurement on the 10MHz second order system

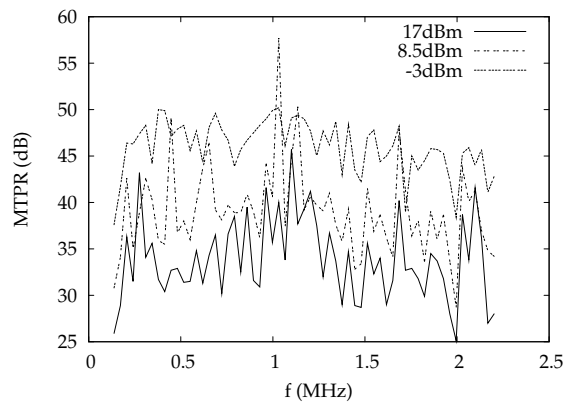
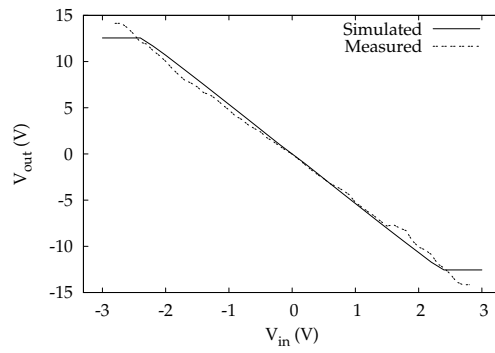
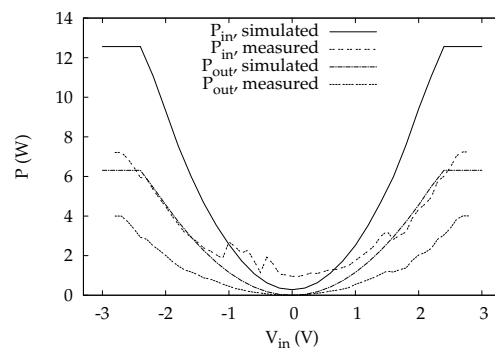


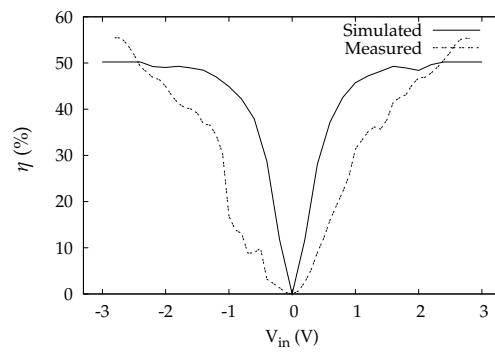
Figure 5.40: MTPR measurements on the 10MHz second order system



(a) DC transfer

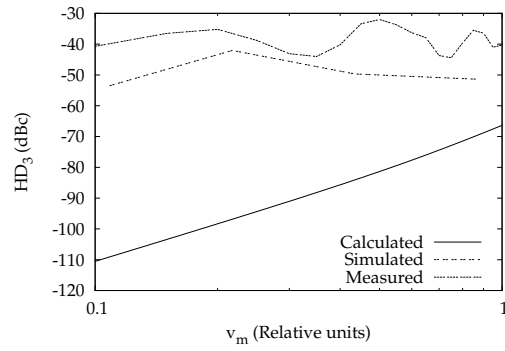


(b) Input and output power

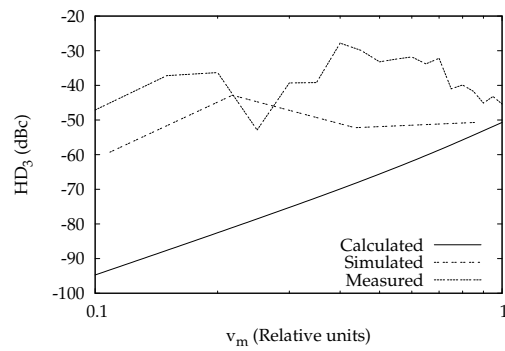


(c) DC efficiency

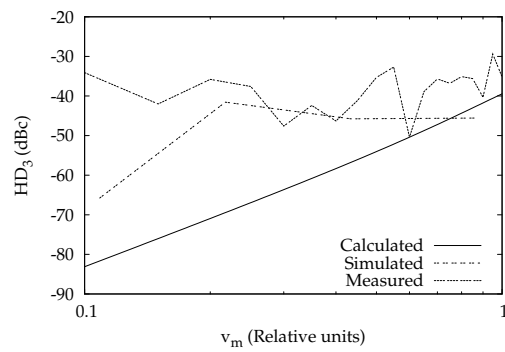
Figure 5.41: DC measurements on the 30MHz second order system



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.42: Third order harmonic distortion of the 30MHz second order system



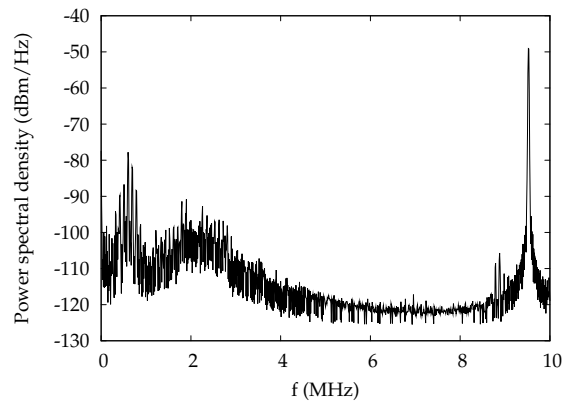


Figure 5.43: Noise measurement on the 30MHz second order system

The MTPR, as shown in Fig. 5.44, is more or less the same as Fig. 5.14, which also could be expected because of the similar DC transfer from Fig. 5.11a and 5.41a.

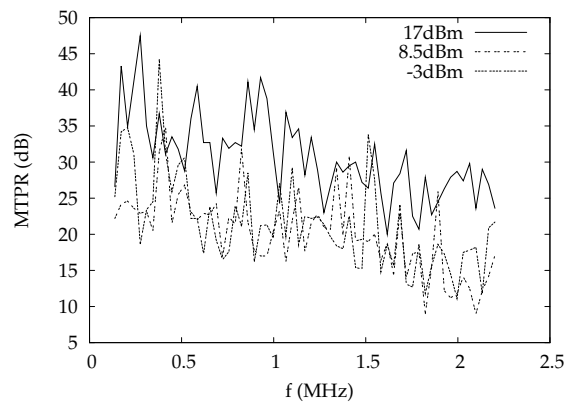


Figure 5.44: MTPR measurements on the 30MHz second order system

### 5.4.4 Third order system

#### DC response

With the load doubled, this time, the third order system could be measured completely. There is however a large offset and a strong non-linearity in the DC transfer from fig. 5.45a, which could not be removed by adjusting the external biasing.

As a consequence, the slight instability, which is still present in this set up, might be the culprit. The minimum input power is significantly lower at 665mW, resulting in a 7.30% efficiency estimate. The measurements lead to 7.20% for half the output power and 11.86% at 20dBm.

### AC response

Surprisingly, the third order harmonic distortion as shown in Fig. 5.46, is reduced by up to 10dB compared to Fig. 5.16. These results are even comparable to, or better than those for the second order system, whereas comparison of the DC transfer would have lead to the opposite conclusion.

### MTPR response

The noise measurement from Fig. 5.47 still demonstrates the instability of the implemented third order loop. For this reason, all measurements again were performed with a 1.5MHz output filter and the MTPR measurements from Fig. 5.48 range up to 1MHz. The result is an overall increase of about 10dB compared to Fig. 5.18.

## 5.4.5 Second order system with independent loops

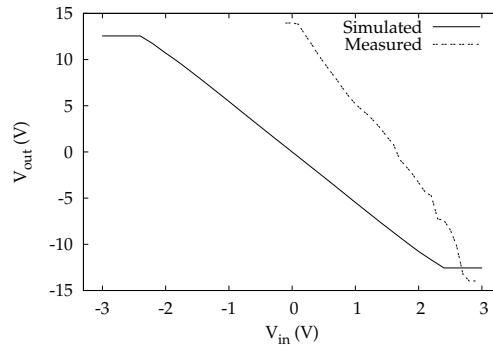
### DC response

Finally, the DC response of the second order system with independent loops is given in Fig. 5.49. As with the regular second order system, the DC transfer corresponds really well with the simulated curve.

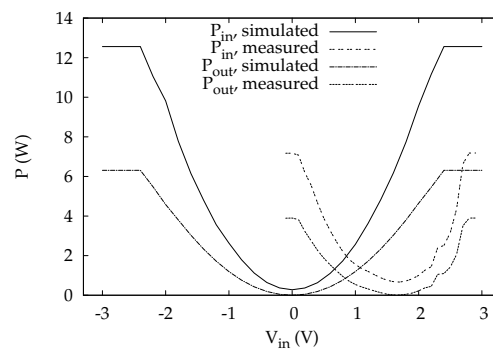
The minimum input power however is increased by almost 200mW, reaching 905mW, which is almost the same as in section 5.4.2. This result leads to a calculated efficiency of 4.91% and measured as 5.40% for 17dBm output power and 9.26% for the full power output.

### AC response

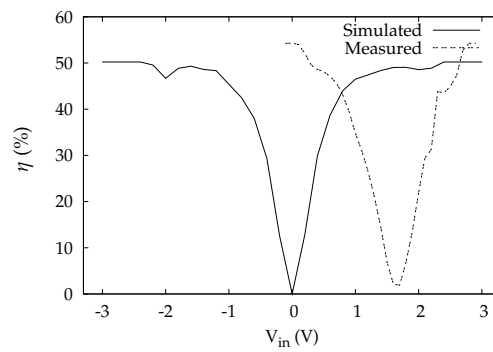
Figure 5.50 shows a slightly decreased third order harmonic content at 200kHz and 500kHz compared to Fig. 5.20, whereas the 1MHz result remains about the same.



(a) DC transfer

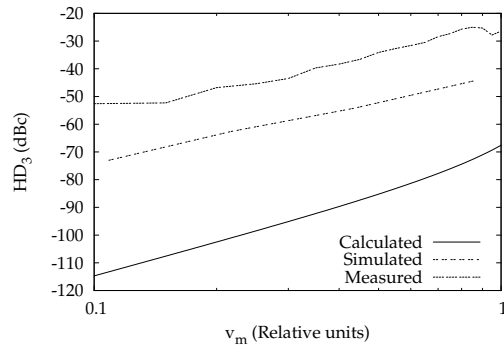


(b) Input and output power

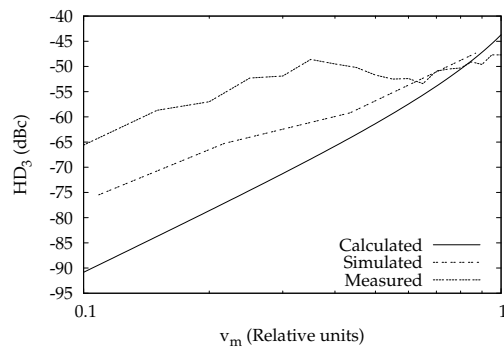


(c) DC efficiency

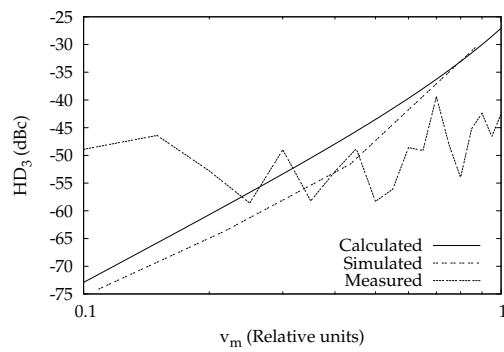
Figure 5.45: DC measurements on the third order system



(a) 200kHz input sine wave



(b) 500kHz input sine wave



(c) 1MHz input sine wave

Figure 5.46: Third order harmonic distortion of the third order system

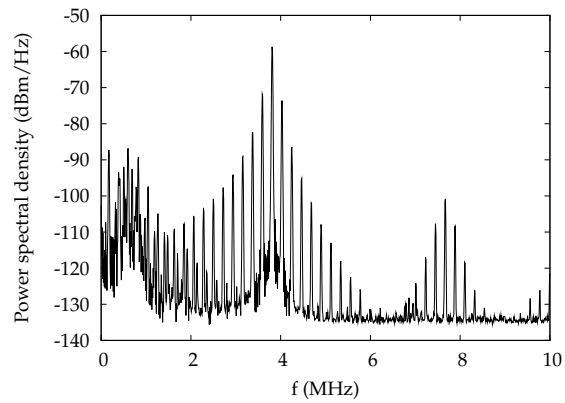


Figure 5.47: Noise measurement on the third order system

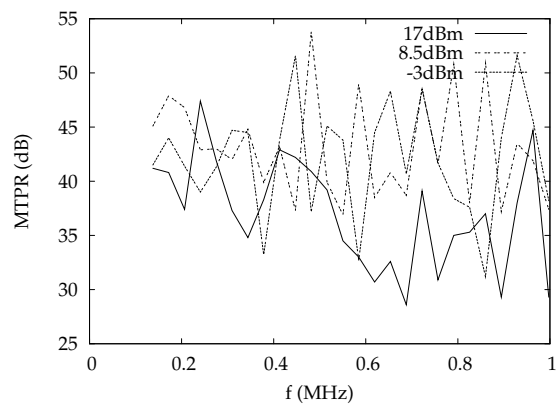
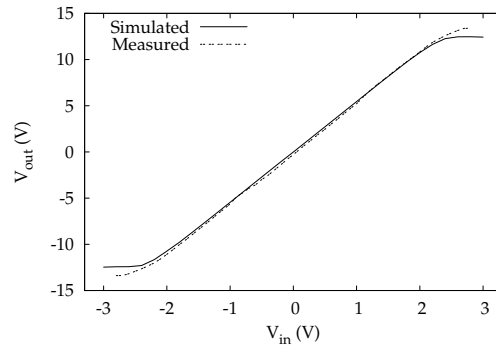
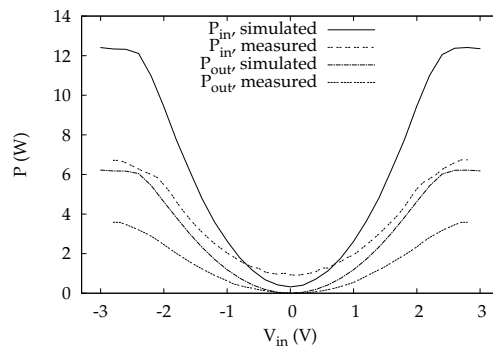


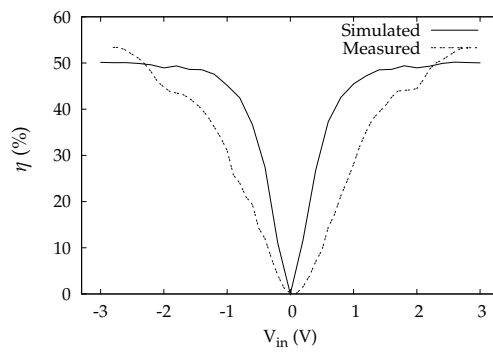
Figure 5.48: MTPR measurements on the third order system



(a) DC transfer

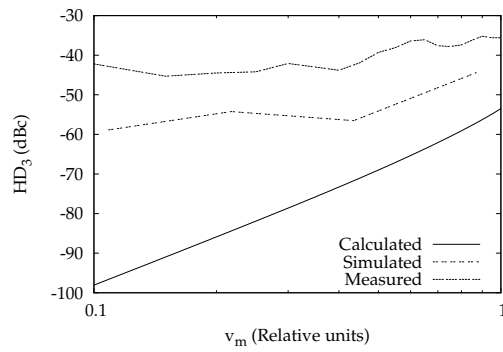


(b) Input and output power

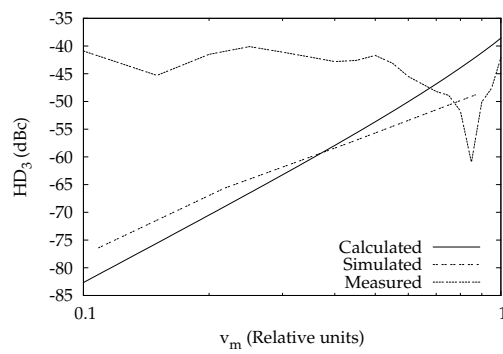


(c) DC efficiency

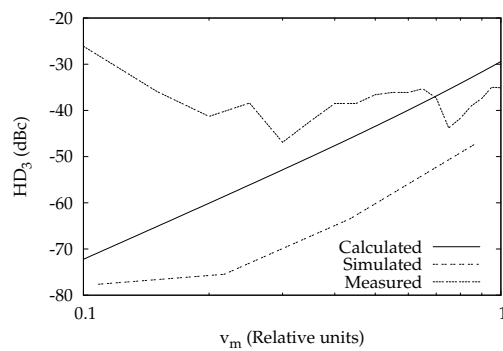
Figure 5.49: DC measurements on the second order system with independent loops



(a) 200kHz input sine wave



(b) 500kHz input sine wave

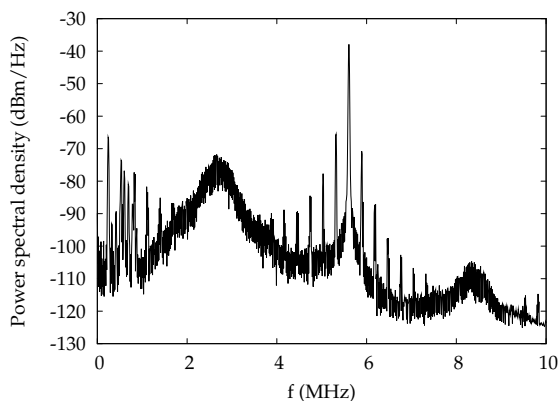


(c) 1MHz input sine wave

Figure 5.50: Third order harmonic distortion of the second order system with independent loops

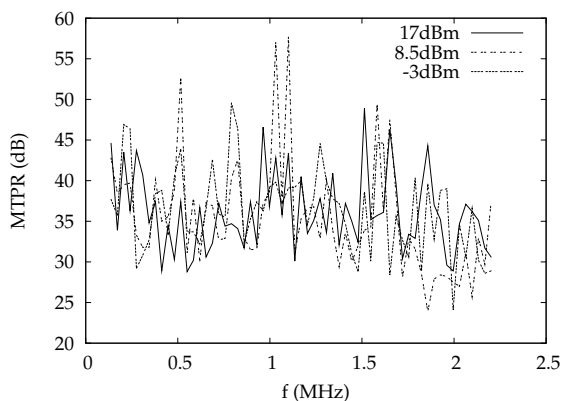
**MTPR response**

The noise measurement from Fig. 5.51 again shows the contribution by the PSU and the filter characteristic, in addition to side lobes caused by the asymmetric switching of the independent output stages.



**Figure 5.51:** Noise measurement on the second order system with independent loops

The results of the MTPR measurements are given in Fig. 5.52, showing comparable values for the low power measurements as in Fig. 5.22. For the maximum power output, the MTPR is increased with 10dB to 35dB.



**Figure 5.52:** MTPR measurements on the second order system with independent loops



## 5.5 Conclusion

The circuits simulated in chapter 4, using the system parameters from chapter 3, are implemented in silicon. A first set of measurements was performed on all circuits, showing a significant discrepancy between simulations and measurements.

The main reason for this difference is identified as the result of self-heating of the DMOS output stage, due to the inclusion of part of the matching resistance of the output filter in the devices. This self-heating further results in a largely increased output impedance as compared with the simulations, leading to an excessively high impedant output of the amplifier, directly influencing the feedback filter characteristics. The resulting time dependent temperature gradient also is expected to have a negative influence on the remainder of the circuits. The impedance and self-heating hypothesis is confirmed by measurements on discrete PDMOS transistors, processed in the same technology, suggesting additional measurements on the amplifiers with an increased load impedance.

The results of these measurements with double load impedance are also presented, already showing better linearity. Additionally, also the oscillating frequency is much more stable and system start up is much easier and reliable. The most important measurement results are summarized in table 5.2.

Additional causes of distortion equally comprise the non-linearity of integrated resistors, capacitors and the opamp circuits, which could not be verified as those signals remain internal to the circuit and their influence is masked by the output stage.

This all leads to the final conclusion that the output stage should be made as low impedant as possible to increase correspondence between simulations and measurements, as suggested by Fig. 5.29.

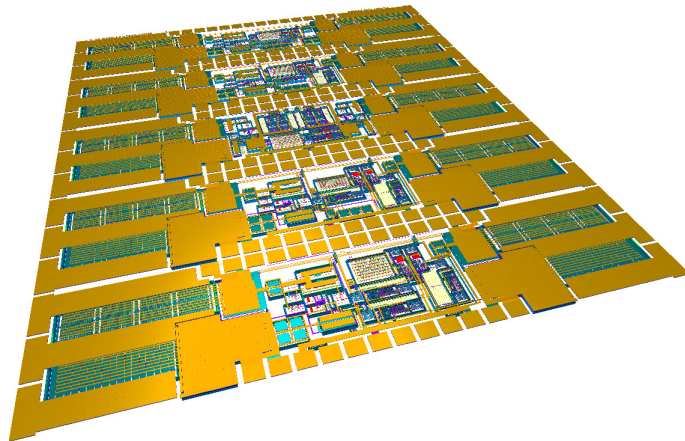
**Table 5.2:** Summary of both sets of measurements on all five circuits

Amplifier	25Ω load				50Ω load			
	$P_{in,min}$	Efficiency @20dBm (estimate)	MTPR	$P_{in,min}$	Efficiency @17dBm (estimate)	Efficiency @17dBm	Efficiency @20dBm	MTPR
First	670mW	12.82%	25-30dB	560mW	7.08%	7.69%	13.28%	30-35dB
10MHz second	787mW	10.50%	20dB	900mW	4.98%	5.22%	9.01%	30dB
30MHz second	725mW	10.38%	30dB	950mW	4.16%	4.08%	7.62%	30dB
Third	1.31W	6.75%	25dB	665mW	7.30%	7.20%	11.86%	35dB
10MHz second (independent loops)	720mW	11.35%	25dB	905mW	4.91%	5.40%	9.26%	35dB

## References

- [1] *Asymmetric digital subscriber line (ADSL) transceivers*, ITU-T Recommendation G.992.1, Jul. 1999.
- [2] *Asymmetric digital subscriber line transceivers 2 (ADSL2)*, ITU-T Recommendation G.992.3, Jan. 2005.
- [3] *Asymmetric Digital Subscriber Line (ADSL) transceivers - Extended bandwidth ADSL2 (ADSL2plus)*, ITU-T Recommendation G.992.5, Jan. 2005.





# 6

## Conclusions and outlook

### 6.1 Main achievements

In this work, an alternative architecture for a xDSL line driver is presented.

First of all, the feasibility of this concept is verified, leading to a successful silicon implementation. The efficiency of this amplifier is 13.1%, with a MTPR of 40dB.

To allow for a more systematic design path, a mathematical description of this non-linear system is presented, resulting in an estimate of the limit cycle frequency and the third order harmonic distortion. The resulting formulæ are then applied to determine the required system parameters of first, second and third order loops, which are further used as a basis for block level simulations and full circuit simulations.

The silicon implementation of all circuits, however, is not yet comparable to the circuit simulations, due to the inclusion of part of the matching impedance in the DMOS output transistors to reduce silicon area, buffer sizes and, as a result, also size imposed delay times. The power dissipation in the DMOS devices causes self-heating, resulting in a significant rise of the temperature. This in turn leads to a significantly increased impedance of the output stage and change in mobility, which is both place and time dependent. The solution will be to redesign the output stage to be much more low ohmic to reduce the influence of the DMOS devices, even though this results in higher delay times and increased area consumption.

This work resulted in several contributions to journals and conference proceedings [1], [2], [3], [4], [5], [6], [7]. Involvement in additional projects also led to [8], [9] and [10].

## 6.2 Future work

In addition to a version with a low ohmic output stage, there are several additional improvements possible.

A first improvement, limiting the number of power supplies required, would be to change the architecture of the level shifter, such that only the high voltage supply is required as an input. Care must however be taken, that the gate signal for the PDMOS output transistors still is strong enough to maintain the required speed, without a disproportional increase of the power consumption of the level shifter.

An additional architectural change to increase the efficiency, would be a similar approach as in [11], where multiple supply voltages are used, allowing the amplifier to work at the smallest power supply capable of generating the instantaneous amplitude level. While a reduced supply voltage, sourcing an identical output current, would mean higher efficiency, this will also reduce the linearity, since the distortion increases and the oscillating frequency decreases with the relative amplitude as explained in chapter 3.

This, however, also makes it possible to take advantage of smaller output DMOS transistors due to the limited output currents for the smallest output voltage range, implying smaller sizes of buffer stages and faster operation at a higher limit cycle. As such, this requires an optimization of the additional voltage supply levels, transistor sizing and, possibly, loop filter dimensioning, to balance efficiency and linearity.

Furthermore, as active termination, which is used with linear line drivers, is not readily applicable, the need for impedance matching can be questioned, since this has no direct influence on the final performance of the system, except for halving the maximum achievable efficiency.

## 6.3 Feasibility and extensibility

The main question remaining now, is the feasibility of asynchronous switching amplifiers as a xDSL line driver, since no compliant system could be demonstrated, in part for the reasons given in the previous chapter.

Based on the results of the Matlab simulations in chapter 3, however, it should be possible to tune the filter order and parameters to reach the MTPR spec, at least

### 6.3 Feasibility and extensibility

205

for ADSL and ADSL2+ that is. For the more high frequent VDSL variants, this is much more questionable, since the requirement for high voltage devices with corresponding level shifters most probably will introduce too high a delay time in the loop to allow functioning at even more elevated limit cycles.

This last remark leads to following conclusion with regard to the extensibility of the technique used throughout this work. The three main parameters influencing the applicability of an asynchronous amplifier are

- Output voltage range
- Output power
- Limit cycle imposed by signal frequency band

which basically boils down to the classical frequency versus parasitics trade-off.

Additional applications thus could be found in the domain of low frequent, high power audio amplifiers, as briefly mentioned in chapter 1 and the area of PWM applications such as power conversion. Since the amplifier architecture is very similar to that of synchronous  $\Sigma\Delta$  converters, it can also be used to that extent at higher operating frequencies.





## References

- [1] V. De Gezelle, J. Doutreloigne, and A. Van Calster, "A 765 mW high-voltage switching ADSL line-driver," *Solid-State Electronics*, vol. 49, no. 12, pp. 1947–1950, Dec. 2005.
- [2] J. Doutreloigne, J. Buyle, and V. De Gezelle, "A multi-level switching amplifier with improved power efficiency for analog signals with high crest factor," in *Proceedings of the 8th WSEAS International Conference on Microelectronics, Nanoelectronics, and Optoelectronics*, Istanbul, Turkey, May 2009, pp. 47–52.
- [3] J. Buyle, V. De Gezelle, B. Bakeroot, and J. Doutreloigne, "A new type of level-shifter for n-type high side switches used in high-voltage switching ADSL line-drivers," in *Proceedings of the 15th IEEE International Conference On Electronics, Circuits and Systems*, Malta, Sep. 2008, pp. 954–957.
- [4] J. Buyle, V. De Gezelle, B. Bakeroot, and J. Doutreloigne, "A high-voltage switching ADSL line-driver, with an n-type output stage," in *Proceedings of the 12th WSEAS International Conference on CIRCUITS*, Rodos, Greece, Jul. 2008, pp. 60–64.
- [5] V. De Gezelle, J. Buyle, and J. Doutreloigne, "Distortion calculation of an asynchronous switching xDSL line-driver," in *Proceedings of the International Symposium on Circuits and Systems*, Seattle, USA, May 2008, pp. 2386–2389.
- [6] V. De Gezelle, "On the design of a switching xDSL line-driver," in *Proceedings of the 8th FirW PhD Symposium*, Ghent, Belgium, Dec. 2007.
- [7] V. De Gezelle, J. Doutreloigne, and A. Van Calster, "A high-voltage, 765mW switching ADSL line-driver," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, Dec. 2005, pp. 213–217.
- [8] H. De Pauw, V. De Gezelle, J. Doutreloigne, A. Van Calster, E. Op de Beeck, R. Van Bolderik, and J. Content, "Development of the area-reducing active 'coil enhancement' principle, practised onto an adsl-pots splitter," *IEEE Trans. Circuits Syst. I*, accepted for publication.

- [9] H. De Pauw, V. De Gezelle, J. Doutreloigne, E. Op de Beeck, R. Van Bolderik, and J. Content, "Active-tunable inductor effected by a novel impedance synthesis circuit," in *Proceedings of the 8th WSEAS International Conference on Instrumentation, Measurement, Circuits and Systems*, Hangzhou, China, May 2009, pp. 95–100.
- [10] T. Bert, V. De Gezelle, G. Van Steenberge, S. Van Put, P. Geerinck, and H. De Smet, "Model for the properties and behavior of electronic paper," in *Abstracts of the SID-MEC Spring 2006 Meeting*, H. De Smet and P. Van Daele, Eds., Mar. 2006.
- [11] F. H. Raab, "Average efficiency of class-G power amplifiers," *IEEE Trans. Consum. Electron.*, vol. CE-32, no. 2, pp. 145–150, May 1986.