Integratie van PWM gebaseerde optische regeling voor emissieve beeldschermen

Integrated PWM based optical feedback for emissive displays

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Promotor: Prof. dr. ir. J. Doutreloigne

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This is my answer to the gap between ideas
and action - I will write it out.
HORTENSE CALISHER

Dankwoord

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Nederlandse Samenvatting –Summary in Dutch–

Beeldschermen zijn alom vertegenwoordigd in ons dagelijkse handelen en dit over heel diverse toepassingsgebieden. Van het kleine draagbare in onze mobiele telefoon over TV en computerschermen tot in tal van professionele applicaties. Deze enorme vraag is de laatste 20 jaar een drijfveer gebleken voor de zoektocht naar steeds goedkopere, kleinere en meer geavanceerdere technologien. Een belangrijk deel van het onderzoek spitst zich toe op emissieve technologien waarbij elk beeldpunt afzonderlijk licht opwekt. Technologien zoals OLED of FED blijken excellente eigenschappen te bezitten doch worstelen met een aantal technologische beperkingen. Vooral uniformiteit blijkt voor de meeste ontluikende emissieve technologien een struikelblok. Immers elk beeldpunt produceert afzonderlijk licht en dit proces is afhankelijk van fysische parameters die varieren van beeldpunt tot beeldpunt. Technologische vooruitgang biedt vaak na vele jaren een oplossing voor de initiele tekortkomingen, doch in dit werk wordt een alternatieve piste vooropgesteld: aangezien elk beeldpunt elektronisch moet worden aangestuurd kan gepoogd worden deze aansturing intelligenter te maken en een meetsysteem in te voeren dat de technologische variaties compenseert.

In dit werk wordt in eerste instantie een korte vergelijking gemaakt tussen de verschillende wijzen waarop een dergelijk meetsysteem kan worden geconcipieerd. We tonen aan dat een optische meting intrinsiek de beste garantie biedt op een goede regeling en bespreken mogelijke pistes om een optisch meetsysteem in de aanstuurelektronica te integreren. Hierbij worden de verschillende

aanstuurmechanismen voor emissieve beeldschermen in de eerste plaats vergeleken met het menselijke gezichtvermogen. Dit is in sterke mate niet lineair waardoor in dit werk een grondige analyse wordt gemaakt van de implicaties van een eventuele lineaire aansturing van een beeldscherm. Theoretische berekeningen worden vergeleken met recente meetgegevens omtrent het menselijke zichtsvermogen en numeriek wordt resolutie van een lineaire aansturing berekend, nodig om een perceptueel equidistante grijswaardenschaal te implementeren. Het menselijke gezichtsvermogen blijkt zeer kundig en kan tot 0.5% variaties detecteren. Hieruit blijkt dat resoluties van meer dan 14bit nodig zijn om de het menselijk zichtvermogen te evenaren. In een tweede fase wordt de integratie van een optische regelsysteem bekeken. We concluderen dat pulsbreedte gemoduleerde aansturing de beste garantie biedt voor een praktische implementatie van een optisch regelsysteem.

Aangezien het optische regelsysteem als functie heeft de uniformiteit voor een beeldscherm te bewerkstelligen en te behouden, wordt gekeken naar theoretische modellen voor de veroudering van bestaande beeldscherm technologien. Aan de hand van modellen wordt een analytische beschrijving gegeven van de invloed van de implementatie van een optische regelkring. Monte Carlo analyse levert echter verassende resultaten op: elke regelkring die veroudering tegengaat blijkt een veel beperktere invloed te hebben dan intuitief verwacht.

In de hoofdstukken die volgen wordt een analyse gemaakt van de integratie van een optische regelkring in de aanstuurelektronica. Hierbij wordt een totale integratie vooropgesteld waarbij in eenzelfde IC alle componenten van het meetsysteem zijn opgenomen: intelligentie, aansturing en optische detectie. De noodzaak tot ijking van het systeem wordt besproken: de meetwaarde voor elk beeldpunt zal immers niet enkel afhankelijk zijn van de emissieve eigenschappen van het beeldpunt, doch ook van de karakterisatie van zijn meetsysteem. Bestaande, toegepaste optische regelkringen blijken zeer eenvoudig en houden hiermee geen rekening. Bovendien wordt aangetoond dat zij ontoereikend te zijn voor een fysieke implementatie van het ijkingsmechanisme. Daarom worden systematisch de vereisten voor een complex optisch regelsysteem bespro-

ken. Er wordt aan de lezer aangetoond dat een volledig geintegreerd meetsysteem enkel werkbaar kan worden gemaakt mits deze ijking wordt losgekoppeld van de eigenlijke aansturing van het beeldpunt. De keuze tot volledige integratie in een enkel fysiek punt brengt een groeiende complexiteit van de regelkring met zich mee. Om ooit commercieel en dus praktisch relevant te zijn moeten verschillende beeldpunten onafhankelijk kunnen worden geregeld. We stellen in dit werk een modulair beeldscherm voor waarbij groepen van beeldpunten door eenzelfde IC worden aangestuurd. Hierdoor ontstaan echter verschillende problemen naar de optische regeling toe: verschillende beeldpunten moeten door hetzelfde regelsysteem worden aangestuurd en invloeden van omgevingslicht worden belangrijker. Finaal wordt een schakeling aan de lezer voorgesteld met mogelijkheid tot ijking en aansturing van verschillende beeldpunten waarbij invloed van omgevingslicht op het meetsysteem wordt gecompenseerd. Gebaseerd op de data omtrent het menselijke gezichtsvermogen wordt een analyse gemaakt van de belangrijkste parameters in het ontwerp. Numerieke resultaten worden gepresenteerd in Tabel **??**.

Ten slotte handelen de laatste hoofdstukken over de fysieke implementatie van dit meetsysteem op een test IC. In dit werk werden optische detectoren ontwikkeld in een bestaand BCD proces. We tonen aan hoe optisch gevoelige diodes en transistoren kunnen worden geoptimaliseerd met de mogelijkheden die de technologie biedt. Metingen bevestigen de initiele simulaties doch tonen aan dat vooral voor fotodiode structuren het omliggend silicium een meer dan significante bijdrage levert aan de fotostroom. Aangezien deze bijdrage kan worden vervormd door andere signalen is een goede afscherming nodig. We tonen aan dat bipolaire transistoren kunnen worden geoptimaliseerd voor fotowerking door gebruik te maken van de proces stappen van een CMOS technologie doch concluderen dat deze behept zijn met een lage bandbreedte.

De uiteindelijke IC integratie van de meetkring wordt grondig besproken en relevante ontwerpsparameters worden toegelicht. Concreet wordt een capaciteit ontladen door de fotostroom en de tijd die hiervoor nodig is bemonsterd. Om het meetsysteem te kunnen ijken kan de spanning over deze capaciteit nauwkeurig worden

geregeld. De optimale strategie om deze spanning op te wekken blijkt een exponentiele DAC. Een analytische uitwerking toont aan dat hierdoor 2 tot 3 bit kan gewonnen worden ten opzichte van een lineaire DAC wat de nodige chip oppervlakte reduceert. Indien ijking over een groter gebied nodig is blijkt een exponentiele DAC de enige praktisch haalbare piste. De correctie voor omgevingslicht gebeurt door de fotostroom te meten over een weerstand en via een analoge regellus een tegengestelde stroom te injecteren.

De nood tot uiterst lage foutbijdrage leidt tot een uitdagend ontwerpstraject. We eisen een foutbijdrage $< 0.1\%$ op het totale systeem, wat met de analyse van de optredende quantisatiefouten moet leiden tot $< 0.5\%$ regeling. Uiteindelijke metingen tonen een werkende regelkring, doch deze slaagt er niet in de nodige precisie te behalen. Het ontwerp naar $\approx 0.5\%$ precisie blijkt in praktijk slechts $\approx 2\%$ precisie op te leveren. Mogelijke oorzaken zijn de onderschatting van lekstromen, de invloed van het invallende licht op het circuit en het ontwerp van de meetopstelling.

English Summary

Monitors are pervasive in our daily actions and this across various applications. Of the small portable screen in our mobile phone, over TV and computer and in many professional applications. This huge demand has been the driving force in the past 20 years for the search for ever cheaper, smaller and more advanced technologies. An important part of the research focuses on emissive technologies where each pixel separately generates light. Technologies such as OLED or FED have shown to possess excellent qualities but are struggling with a number of technological limitations. Especially display uniformity appears for most emerging emissive technologies a stumbling block. Indeed, every single pixel produces light yet this process depends on physical parameters that vary from pixel to pixel. Technological progress often only yields a solution to the initial shortcomings after many years, but in this work an alternative approach is suggested: since each pixel should be driven electronically we attempt to introduce in this driver a feedbacksystem and the needed intelligence to compensate for the technological variations.

In this work, initially a brief comparison is given between the different ways in which such a system can be conceived. We show that an optical measurement intrinsically gives the best guarantee of good feedback and discuss possible ways to integrate an optical measurement system in the control electronics. The different driving mechanisms for emissive displays are in the first place compared to the human eyesight. This is highly non-linear and therefore in this work a thorough analysis is made of the implications on a possible linear driving of a display. Theoretical calculations are compared with recent measurements on human eyesight and numerical we

find the required resolution of a linear driving mechanism capable of producing a perceptually equidistant gray scale implementation. The human vision appears very capable and can detect variations up to 0.5 %. This shows that resolutions ¿14bit are necessary to match the human eyesight. In a second phase, the integration of an optical feedback in the driver electronics is discussed. We conclude that pulse width modulated control offers the best garanitie for a practical implementation of an optical system.

Since the goal of the optical feedback is to achieve and maintain the uniformity of a display, theoretical models for the aging of existing display technologies are examined. Using analytical models, the impact of the implementation of an optical control circuit on the display's lifetime is discussed. Monte Carlo analysis provides surprising results: a feedback mechanisme has a much smaller influence than intuitively expected.

In the chapters that follow, an analysis is made of the integration of an optical feedback loop in the driving electronics. We aim for a total integration all components of the measurement system into a single IC: intelligence, control and optical detection. The need for calibration of the system is discussed: the measurement for each pixel will not only depend on the emissive properties of the pixel, but also the characterization of its measurement system. Currently applied optical control loops appear to be very simple and never take this into account. Moreover we demonstrate that they are not fit for a physical implementation of a calibration mechanism. Therefore, systematicly the requirements for a more complex optical feedback system are discussed. It is shown that a fully integrated measuring system can be made workable only if the calibration is separated from the actual driving of the pixel. The choice for full integration of the feedback into a single physical point does require a growing complexity of the control loop. To have a solution that should be practically (commercially) relevant, it becomes clear that different pixels should be driven from the same IC. We propose in this work a modular display where groups of pixels can be controlled by the same IC. This creates several problems to the optical feedback: different pixels should to be controlled by the same optical detector and the influence of ambient light becomes important. Finally

the reader is presented a circuit with the possibility of calibration and optical control of various pixels where the influence of ambient light on the measuring system is compensated. Based on the data about the human vision an analysis of key parameters in the design is made. Numerical results are presented in Table ref (H3tab: ValuesALRRandNOBS).

Finally the last chapters deal with the physical implementation of the optical feedback system on an IC test. In this work optical detectors are developed in an existing BCD process. We show how light sensitive diodes and transistors can be optimized with the possibilities that technology offers. Measurements confirm the initial simulations, but mainly for photodiode structures the surrounding silicon adds a significant contribution to the photocurrent. Since this contribution can be distorted by other signals a good shielding is needed. We show that bipolar transistors can be optimized to a phototransistor by using the process steps of a CMOS technology. However simulations show that they are posessed with very bandwidth.

The actual IC integration of the measuring circuit is thoroughly discussed and relevant design parameters are explained. Practical implementation is done as following: a capacitor is discharged by the photocurrent and the time required is sampled. To calibrate the optical feedback system, the voltage across this capacitor can be precisely regulated. The optimal strategy to regulate this charging voltage is proven to be an exponential DAC. An analytical analysis shows that this 2 to 3 bits can be won against a linear DAC, which reduces the necessary IC area. If calibration is required over a larger range an exponential DAC shows to be the only viable option. The ambient light rejection is done by sensing the photocurrent through a resistor and injecting an opposite current.

The need for extremely low error contribution results in a challenging design. We demand an error contribution $< 0.1\%$ to the feedback circuits. With the analysis of the other quantisation errors this should lead a precision $< 0.5\%$ for the entire system. Final measurements show a functional system, but fail to achieve the necessary precision. The design for $\approx 0.5\%$ precision, only delivers $\approx 2\%$ precision. Possible causes are the underestimation of leakage cur-

rents and noise, the influence of the incident light on the circuit and the design of the measurement setup.

1 Grayscaling and Uniformity

1.1 The Human Visual System (HVS)

The way humans "see" is a very complex thing. Our visual system is not so much a measuring system that generates the exact measurement signals it needs. The brain will use all available signals in a very non linear way, combine it with memories and non-visual stimuli to create what we call vison. In fact one could say we do not see... we percieve. When trying to display an image on a display, it is clear the human vision system (HVS) of the observer should always be taken into account.

For example colours shown on a display are not an absolute property of light. A light stimulus will generate a certain physical stimulus but the percieved colour will depend on physical and psychological inputs. However, the percieved colour will be related to the spectral content of the light stimulus. In the human eye, rods and cones will absorb photons but in a very wavelength dependent way. Taking this spectral sensitivity of the HVS into account, an arbitrary

photometric quantity can be defined:

$$X_v = K_m \int_{\lambda} V(\lambda)\, X_{e,\lambda} d\lambda \tag{1.1}$$

where $K_m = 683\ lm/W$ and $V(\lambda)$ is the spectral photopic[1] sensitivity of the eye and $X_{e,\lambda}$ the corresponding radiometric quantity, based solely on the electromagnetic radiation characteristics of the light.

The luminance $L_v\ [cd/m^2]$ is such a photometric quantity, being a measure of the luminous power per unit area of light travelling in a given direction. Typically the luminance of displays is defined for 2°. However, the HVS reacts very non-linearly on percieved luminance. We all experience that the brighter the lighting source, the harder it is to see small differences in brightness. However, in badly lit situations we can detect very small differences in brightness. To introduce grayscaling in a display it is obvious that we need a better understanding of the HVS' reaction to luminance.

1.1.1 Weber's law

One of the oldest approximations of HVS was given by Ernst Heinrich Weber (1795-1878). Weber introduced the "Just Noticable Difference" of perception and found that if a luminance is just noticable different from it's surrounding luminance, their ratio is given by:

$$\frac{\Delta L}{L} = 0.02 \tag{1.2}$$

This means that the relation between the luminance L and JND's j can be written as:

$$\begin{aligned} L(j) &= (1.02)^j \cdot L_{\min} \\ \Rightarrow \qquad j(L) &= \frac{\ln\left(\frac{L}{L_{\min}}\right)}{\ln(1.02)} \end{aligned} \tag{1.3}$$

[1] photopic sensitivity: sensitivity of the eye under well-lit conditions which allow color perception. In contrast to scotopic and mesiotopic sensitivity being the sensitivity of the eye under low-light and intermediate conditions respectively.

However, [2] and [3] mention a general power law as presented by Stevens' law and the CIELUV model (see below) gives a better approximation of the HVS. We mention Weber's law however because of the JND's. Equation (1.2) states the HVS can only determine variations of 2% and presents a minimum uniformity condition for displays. Many publications still use this "2% rule" as a uniformity condition.

1.1.2 Stevens' law

In the CRT/TV world however, Stevens' power law is often used. This law dating from 1957 is considered more accurate than Weber's law and states that a perceptual magnitude $\psi(\mathrm{Y})$ of an external stimulus Y is given by:

$$\psi(\mathrm{Y}) \sim \mathrm{Y}^{\alpha} \tag{1.4}$$

Stevens' law is a relatively good approximation for most stimuli (sound, vision, smell, ...) and for percieved brightness $\alpha \approx 0.33 \rightarrow 1$ is found depending on the background, viewing angle, type of light source, ...

By coincidence, the I-V characteristic of a CRT follows a same curve where the excitant electron current depends on the driving voltage as follows:

$$\mathrm{Y} = V^{\gamma} \tag{1.5}$$

with typical gamma values of 1.5 to 2.5. As the luminant output of a CRT is proportional to the excitant current it follows:

$$\psi(\mathrm{Y}) \sim V^{\alpha \cdot \gamma} \sim V \tag{1.6}$$

This means the percieved brightness of the display is proportional to variations in the CRT driving voltage, which is handy from an electrical point of view.

Note that a display is used to display recorded images. By linearly varying the CRT driving voltage V, the output luminance will increase according to Eqn. (1.5). When recording images this

means the opposite conversion is necessary, mapping exponentially (Stevens' law) varying luminance values to equidistant voltages:

$$V_{rec} \sim (Y_{\text{real}})^{\alpha} \quad \Rightarrow \quad \psi(Y_{\text{real}}) \sim (Y_{\text{real}})^{\alpha\cdot\gamma\cdot\alpha} \tag{1.7}$$

$$\overset{\alpha=1/\gamma}{\Rightarrow} \quad \psi(Y_{\text{real}}) \sim (Y_{\text{real}})^{\alpha} \tag{1.8}$$

$\psi(Y)$ is now once again given by Eqn. (1.4). That is why recording devices will incorporate the transfer function of the HVS as shown in Eqn. (1.8). This means they will make optimal use of the perceptual channel, reserving more bits for the lower range of luminances and fewer for the higher end. Mark that $\alpha = 1/\gamma$ isn't always true. γ is different for different kind of CRT's and α is observer dependent. Therefore often a correction on the incoming signal is possible: $V' = V^c$. This gives

$$\psi(Y_{\text{real}}) \sim (Y_{\text{real}})^{(\alpha\cdot\gamma\cdot c)\cdot\alpha} \tag{1.9}$$

By adjusting c to the observer's taste a better HVS matching is possible ($\alpha \cdot \gamma \cdot c = 1$).

1.1.3 CIELUV model

Similarly to the photometric quantities, the popular RGB colour representation was defined by the CIE in 1931. The sensitivity towards monochromatic primary colours with wavelengths of 700nm (R), 546.1nm (G) and 435.8nm (B) were defined (so called colour matching functions). For example with $r(\lambda)$ being the red colour matching function the R-value of a spectrum $S(\lambda)$ is then defined as:

$$R = \int_{\lambda} r(\lambda)\, S(\lambda)\, d\lambda \tag{1.10}$$

This (r,g,b) standard can be linearly transformed to the (x,y,Y) representation which has only positive color coordinates and where Y is chosen to represent the luminance L_v. Though the (x, y, Y) coordinates can represent each percieved colour, they only take into account the absorption properties of the HVS. However as mentioned

the brain works with the eyes input in a very non-linear way and colour / brightness perception is dependent on the luminance value. Therefore these coordinates are not yet perceptually uniform. In other words, the distance between two colours which are just noticeably different varies across the surface of the (x,y) diagram. In 1976 the CIE presented the CIELUV model, a more perceptually uniform colour model, being a non-linear projection of the (x,y,Y) model.

In order to account for the non-linear perception of luminance, Y is replaced by L^*.

$$L^* = \begin{cases} 116\left(\frac{Y}{Y_w}\right)^{\frac{1}{3}} - 16 & \frac{Y}{Y_w} > \left(\frac{24}{116}\right)^3 \\ \frac{29^3}{27}\frac{Y}{Y_w} & \frac{Y}{Y_w} \leq \left(\frac{24}{116}\right)^3 \end{cases} \tag{1.11}$$

The colour coordinates (x,y) are transformed to (u',v'):

$$u' = \frac{4x}{-2x+12y+3} \qquad v' = \frac{9y}{-2x+12y+3} \tag{1.12}$$

These coordinates are then coupled to the luminance L^*:

$$u^* = 13L^*\left(u'-u'_w\right) \qquad v^* = 13L^*\left(v'-v'_w\right) \tag{1.13}$$

with Y_w,u'_w and v'_w the coordinates of standard D65 white.

For perceptually equidistant grayscale implementation, brightness function L^* is important. It allows to translate a measurable photometric luminance Y (referred to the brightness of the reference white light) to a measure of percieved brightness L^*. The CIELUV model only defines the perceptual distance between two colors to be

$$\Delta E = \sqrt{\left(L_2^*-L_1^*\right)^2 + \left(u_2^*-u_1^*\right)^2 + \left(v_2^*-v_1^*\right)^2} \tag{1.14}$$

where two stimuli are just noticable different (JND) if $\Delta E = 1$. Note that L^* is only defined up to $Y = Y_w$ with $L^* = 100$ in that case. Thus when u^* and v^* remain constant, only 100 equidistant grayscales are defined in this model.

1.1.4 DICOM model

More recently, for high accuracy medical display devices, DICOM presented a thorough study of the HVS for grayscaling. A standardized display function for display of grayscale images (GSDF) based on Barten's model [4] was presented. As this model is based on more recent experiments, we will use the GSDF in this work. The GSDF was derived by measuring luminance modulation which is just noticeably different (JND) for an average human observer. Figure 1.1 shows the GSDF where the Y-axis shows the JND's which are perceptual equidistant. The X-axis shows the corresponding luminance in cd/m^2. The analytic representation of the GSDF is given by Eqn.

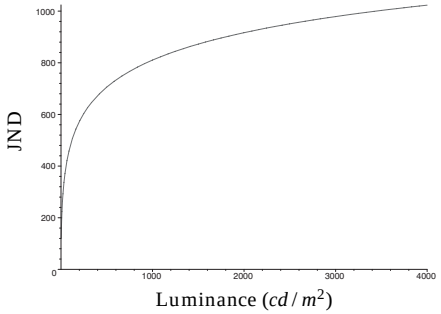


Figure 1.1: DICOM GSDF representing 1024 (10 bit) perceptually equidistant luminances. It's analytic representation is given by Eqn. (1.15) or (1.16).

(1.15) and (1.16). This is a fit of a 10 bit measurement, listed in [4].

$$\begin{aligned} j(L) &= A + B\log_{10}(L) + C\left(\log_{10}(L)\right)^2 + D\left(\log_{10}(L)\right)^3 \\ &\quad + E\left(\log_{10}(L)\right)^4 + F\left(\log_{10}(L)\right)^5 + G\left(\log_{10}(L)\right)^6 \\ &\quad + H\left(\log_{10}(L)\right)^7 + I\left(\log_{10}(L)\right)^8 \end{aligned} \tag{1.15}$$

with A = 71.498068, B = 94.593053, C = 41.912053, D = 9.8247004, E = 0.28175407, F = -1.1878455, G = -0.18014349, H = 0.14710899 and I = -0.017046845.

$$\log_{10}(L(j)) = \frac{a + c\ln(j) + e(\ln(j))^2 + g(\ln(j))^3 + m(\ln(j))^4}{1 + b\ln(j) + d(\ln(j))^2 + f(\ln(j))^3 + h(\ln(j))^4 + k(\ln(j))^5}$$

(1.16)

with a = -1.3011877, b = -2.5840191E-2, c = 8.0242636E-2, d = -1.0320229E-1, e = 1.3646699E-1, f = 2.8745620E-2, g = -2.5468404E-2, h = -3.1978977E-3, k = 1.2992634E-4, m = 1.3635334E-3.

For a standard emissive display 1000 cd/m^2 can be taken as $L_{\max}$ and 1cd/m^2 as $L_{\min}$ due to reflection from ambient light. ([4] suggests 0.305 cd/m^2 for a CRT display and [5] reports 1.15 cd/m^2 for an LCD display). Equation (1.15) teaches that $j(1000) - j(1) = 810.48 - 71.5 \approx 739$. This means there are 739 JND's that can be produced with a display with maximum luminance of 1000 cd/m^2, which corresponds to 9.53 bit perceptual grayscaling. In order to have a display that is as good as or better than the HVS, 10 bit perceptual grayscaling is required and more than 10 bit is not usefull. For example for medical applications this is important, but most commercial displays only incorporate 8 bit grayscaling.

The existence of JND's has two main consequenses:

1. The necessary uniformity of a display is determined by 1 JND. This means the uniformity of a grayvalue should always be within 1 JND of it's luminance value. Weber's law formulates a very easy rule: non-uniformity should be smaller than 2% (see Eqn. (1.2)). However, the DICOM model presents a more complex curve. Figure 1.2(b) shows the relative error $\Delta L/L$ corresponding with 1 JND that is allowed for the DICOM model. It is clear that the 2% rule is too stringent for very small luminance values, but in general not restrictive enough. Probably due to the ease of Weber's law, some publications however still use the 2% rule as a target for display uniformity [6, 7, 8]. However if any, Fig. 1.2(b) indicates 0.65% would be a better uniformity boundry.

2. As each display has a maximum luminance and a minimum luminance, the number of preceptually equidistant grayscales that can be detected by the human eye is limited. Consider for example a display with contrast ratio $L_{\max}/L_{\min} = 1000$. Figure 1.2(a) shows the corresponding JND's for Weber's law

and the DICOM model. Weber's law predicts the HVS can only determine 348.8 preceptually equidistant graylevels. This corresponds with 8.45 bit grayscaling. In the DICOM model the absolute luminance is also important. As previously mentioned, working with $L_{\min} = 1\ cd/m^2$ and the same contrast ratio, gives 739 equidistant graylevels or 9.53 bit.

1.1.5 Other models

In literature there are numerous grayscale models available, each better suited for a certain situation. The DICOM GSDF for example is only defined for levels of gray, but not for colour displaying. Moreover it is defined for uniform and static gray level displaying. Much more complex spatial and temporal dependent tone reproduction models exist. [9], [2] and [3] give good reviews. As it is the most recent and best documented, we will use the DICOM model in this work for our calculations, unless noted otherwise.

1.2 Perceptual grayscaling

Previous section explained the HVS' sensitivity towards brightness. To achieve a perceptual grayscaling the corresponding output luminances are found by applying one of the described models. We will use the DICOM model in the rest of this work. For a display with n-bit perceptual grayscaling the corresponding perceptually equidistant luminances are created by the driver electronics who apply a driving signal to the display technology. A required output luminance value can be mapped to the correct driver signal which generates this value. This mapping process is very dependent on both driver architecture and display technology. Figure 1.3 shows this mapping procedure for an amplitude modulated (AM) driven CRT and OLED display and a linearly driven display (in casu a pulse width modulated (PWM) driven display). It is clear that the better the display's characteristic resembles the HVS, the more efficient this mapping will be. For a CRT the resemblance is very good (see Sect. 1.1.2) and n bit perceptual grayscaling will almost need n bit

equidistant V_{CRT} values. The driving circuit for an OLED display is shown in Fig. 1.7 (p. 24) and results in a square dependency of the OLED output luminance on the driving voltage. Figure 1.3 illustrates that a larger range for the driving signals is necessary. As PWM is inherently linear, the conversion is even worse. The resolution of a linear PWM driver will therefore be much higher than n.

Driver/Display Characteristic The dependency of the output luminance on the driving signal for a field emission display (FED), OLED and linearly driven display can be written as:

$$L_{out}(k) = (L_{\max} - L_{\min}) \cdot \left(\frac{k}{2^n - 1}\right)^{\gamma} + L_{\min} \tag{1.17}$$

L_{out} represents the output luminance of the display pixel. $L_{\max}$ is the maximum luminance for the pixel which is dependent on the display technology. $L_{\min}$ is the minimal luminance that remains when the pixel is "black", e.g. due to reflectance of ambient light. The display and its driver only have a limited resolution n, meaning that only n equidistant driving signal values can be made by the driver. Each display-driver combination will transfer these equidistant driving signals to some output luminances by means of 1.17. For a FED γ is dependent on the type of emittor. As mentioned a CRT has $1.5 < \gamma < 2.5$ but for example Spindt-emittor based FED's can have $\gamma \approx 3.5$. We will use $\gamma = 2.5$ as a FED characteristic in the following reasoning. Active matrix OLED displays (see Fig. 1.7 on p. 24) have a quadratic dependency, thus $\gamma = 2$. These are examples of non-linear display-driver combinations. A linearly driven display, whether it is AM or PWM, obviously has $\gamma = 1$.

Suppose we wish to display a certain perceptual graylevel j. The corresponding output luminance $L_{HVS}(j)$ for this perceptual graylevel j is then easily derived from the HVS model used (e.g. the DICOM model). For the display-driver combination, a certain value of k corresponds to this output luminance. As k has to be an integer

value, k is given by:

$$k = \text{round}\left[\sqrt[\gamma]{\frac{L_{HVS}(j) - L_{\min}}{L_{\max} - L_{\min}}} \cdot (2^n - 1)\right] \tag{1.18}$$

and the resulting lumination is $L_{out}(k,j)$. For every j, a k value can be derived for the display but an error in output luminance because of the limited resolution n will occur.

Grayscaling To have a meaningfull graytone representation we can say:

$$L_{out}(k,j) \geq L_{HVS}(j) \quad \Rightarrow \quad L_{out}(k,j) < L_{HVS}\left(j + \frac{1}{2}\right) \tag{1.19}$$

$$L_{out}(k,j) \leq L_{HVS}(j) \quad \Rightarrow \quad L_{out}(k,j) > L_{HVS}\left(j - \frac{1}{2}\right) \tag{1.20}$$

This means the error made by approximating the ideal output luminance should be smaller than a perceptual LSB/2 or it might be seen as "the wrong shade": the conditions above will guarantee monotonous grayscaling.

On the other hand, two adjacent grayscale levels should always be distinguishable from each other. As mentioned before, there is a just noticeable difference between two luminance values, so extra conditions can be written:

$$L_{out}(k',j-1) < L_{out}(k,j) - 1\ JND \tag{1.21}$$

$$L_{out}(k',j+1) > L_{out}(k,j) + 1\ JND \tag{1.22}$$

If for example $L_{out}(k',j-1)$ is an overestimate of $L_{HVS}(j-1)$ and $L_{out}(k,j)$ is an underestimate of $L_{HVS}(j)$, eqn. 1.21 says that these values should still be noticeably different.

Figure 1.4 shows the relative error made for the first 64 graytones of an 8 bit DICOM grayscaling accomplished by a 14, 12 and 10 bit linear PWM, with

$$\Delta L_{rel} = \frac{L_{PWM}(k,j) - L_{DICOM}(j)}{L_{DICOM}(j)} \tag{1.23}$$

$L_{\max}$ was chosen 1000 cd/m^2 and $L_{\min} = 1\ cd/m^2$. It is obvious that the relative error will be much larger for smaller grayscale values. Figure 1.4 shows the inefficiency of a linear PWM for preceptual linear grayscaling. To have a low relative error, the maximum stepsize is determined by the smallest graytones but for larger graytones such a small stepsize is not necessary: the relative error is very small. Figure 1.5 shows that 14 bit linear PWM is needed for a monotonic variation of the output necessary for a meaningfull 8 bit DICOM graytone representation. For 12 bit (middle graph) or 10 bit (right graph) precision, several graytones will be approximated by the PWM driver with the same PWM output code k and thus the same output luminance. This means we lose graytones or the representing number of bits (NOB) drops below 8. Note that the required PWM precision is dependent on $L_{\max}$ and $L_{\min}$.

Uniformity With the conditions used above the display can produce meaningfull perceptual grayscaling, meaning they will be monotonous and distinguishable (> 1 JND from each other). To accomplish this the driver signal is adjustable with n bit precision, also meaning a noise error of maximum LSB/2 can occur. When two pixels are driven with the same desired driving signal, this noise contribution will result in an output luminance variation from pixel to pixel. A human observer will experience these variations if they are larger than 1 JND. The output luminance is given by Eqn. (1.17) and a deviation of $1/2$ LSB means $k \pm 1/2$. Thus extra conditions can be defined for the display:

$$L_{PWM}\left(k-\frac{1}{2}\right) > L_{HVS}\left(j\left(L_{PWM}(k)\right)-1\right) \quad (1.24)$$

$$L_{PWM}\left(k+\frac{1}{2}\right) < L_{HVS}\left(j\left(L_{PWM}(k)\right)+1\right) \quad (1.25)$$

Note that these conditions will define a minimum NOB required for pixel to pixel uniformity, independent of the NOB perceptual grayscaling! However the maximum and minimum luminance values of the display and the driver/display characteristic do are important.

	100			500			1000			4000		
	2.5	2	1	2.5	2	1	2.5	2	1	2.5	2	1
6	8	8	10	8	8	12	8	9	13	9	9	14
7	9	9	12	9	9	13	9	10	14	10	10	16
8	11	11	14	11	11	15	10	11	15	11	11	17
9	-	-	-	13	14	17	13	13	17	12	13	18
10	-	-	-	-	-	-	-	-	-	13^*	13^*	19^*

Table 1.1: The required NOB for preceptually equidistant grayscaling. $L_{\min}$ was kept constant at 1 cd/m^2 and $L_{\max}$ was stepped (100, 500, 1000 and 4000 cd/m^2). Different driver / display characteristics are listed: FED ($\gamma = 2.5$), OLED ($\gamma = 2$) and a linear characteristic ($\gamma = 1$).

Discussion Tables 1.1 and 1.2 list the NOB precision required for different driver / display characteristics, different numbers of perceptual grayscaling and different contrast ratio's of the displays. Table 1.1 shows the required precision without the uniformity constraint, Table 1.2 lists the NOB for the uniformity constraint. Let us focus on a display with $L_{\max} = 1000$ cd/m^2 and $L_{\min} = 1$ cd/m^2. To achieve 6 bit grayscaling (=64 levels) a linear driver / display characteristic requires 12 bit precision. To achieve a uniform display however, 15 bit precision is required.

For 128 (= 7 bit) and 256 (= 8 bit) grayscale levels 15 bit precision will be enough for a uniform display. For 9 bit grayscales (= 512 levels) 16 bit precision is required, so the uniformity constraint is no longer the dominating condition. Note that high brightness displays up to 4000 cd/m^2 require 17 bit precision for a linear driver / display characteristic. Compared to this, a CRT with $\gamma = 2.5$ only needs 11 bit resolution. An OLED driver (shown in Fig. 1.7 p. 24) requires a substantially lower NOB to achieve the same uniformity than a linear driver.

In Table 1.1 it is clear that the display's contrast ratio determines the achievable number of graylevels. As the DICOM curve defines 10 bit JND's up to 4000 cd/m^2, only displays with $L_{\max} >$ 4000 cd/m^2 can achieve 10 bit perceptual grayscaling. For $L_{\max} =$

4000 cd/m^2 the grayscales would be the $L(j)$ values from the DICOM model. This means that Eqn. (1.21) and (1.22) can only be met if $n \to \infty$. Therefore we have omitted these conditions in that case.

A remark should be made concerning the listed NOB: the precisions listed are these of the driver signal before the output stage. For an OLED driver the mentioned required NOB is that of the gate voltage of the driving transistor. However, the noise constraint for the driving transistor itself, is this of the linear case and thus the output stage requires a much larger signal to noise ratio than the driving signal electronics! For a CRT/FED display with $\gamma > 2$ the dependency of the luminance on the driving signal is a display technology dependent characteristic. Therefore, the NOB of Table 1.1 and 1.2 do suffice for the driver electronics, unlike for the OLED driver. However a driver which satisfies the listed conditions is still useless when the display technology itself does not achieve the necessary uniformity and especially for new technologies, this is were the shoe pinches.

100			500			1000			4000		
2.5	2	1	2.5	2	1	2.5	2	1	2.5	2	1
9	9	11	9	10	14	10	10	15	11	11	17

Table 1.2: The minimum required NOB driver precision for a perceptually uniform display. $L_{\min}$ was kept constant at 1 cd/m^2 and $L_{\max}$ was stepped (100, 500, 1000 and 4000 cd/m^2). Different driver/display characteristics are listed: FED ($\gamma = 2.5$), OLED ($\gamma = 2$) and a linear characteristic ($\gamma = 1$).

1.3 A need for feedback

In this work we focus on emissive large area displays. These are displays often used for outdoor applications such as concerts, sports events, ...Typically LED displays are commercially available, but other technologies are showing great promises such as field emission displays (FED) and organic LED (OLED). Emissive technologies are display technologies where the emitted light is generated within

each pixel, differentiating it from backlighted or reflective displays as LCD, electrowetting, ...

Generally emissive displays are interesting because of their superior brightness and contrast ratio, however they have some problems of their own. As an emissive display consists of individual emitting pixels with individual characteristics, the uniformity of output is often a problem. When applying emissive technologies for display applications, a uniformity of 1 JND for the entire display is required during a lengthy lifetime. We showed in Sect. 1.2 that this leads to high precision requirements on the driver side. However, it is clear the display technology should at least be as good. In Sect. 1.1, Fig. 1.2(b) showed that for high luminance values the DICOM model demands output variations should be smaller than 0.65% and remain smaller during the proposed lifetime of the display. This is a major problem for most emissive display technologies!

It is clear that even with good initial uniformity, it is very hard to garanty uniformity over a certain lifetime. As each pixel will age over time, each pixel might age differently and thus non-uniformity will grow steadily in time. For some display types such as large area LED displays, the ageing curve of the pixels is well known and very steady and might be incorporated in the displays driving electronics. However, some other technologies such as CNT-based FED do not have this luxury.

Another problem is temperature dependency of the emissive output. As different image data might induce temperature differences from pixel to pixel, temporary non-uniformities can occur. Figure 1.3 shows the influence of operation time and temperature on the light output of an RGB LED system and illustrates the need for a solution.

To compensate for this unknown ageing characteristic and removing ageing and temporary non-uniformities we must somehow find out their magnitude by measuring a quantity which is related to the output luminance of the pixel. With this measurement we can change the driving signal of the pixel to achieve better uniformity. As each pixel emits it's own light, it is clear that this measurement should be done on a pixel level! Two possibilities exist:

- An external calibration measurement allowing to remap the driving signals for each pixel.
- An intelligent display approach where a (pixel based) measurement system is build in the display.

For a display without added intelligence, an external calibration would be required every now and then to remap the driving signals for each pixel. This means the display quality will still deteriorate up to the next calibration. Moreover every calibration is a time consuming, impractical process and not very customer (nor producer) friendly. Therefore a display with imbedded intelligence is technically a preferable choice. For example [11] reports a current feedback for OLED displays. Also numerous LED drivers were the LED current is measured (for example as a voltage over a small resistor) and controlled by a high frequency PWM feedback loop are commercially available. However, even as current through the pixel remains constant, current-to-light efficiency of the pixel might deteriorate over time or over temperature. Only optical feedback which measures the actual emitted output, can overcome such deviations. For this reason optical feedback is widely used in commercial laser drivers for telecom applications. For example the ADN2870 uses optical feedback to control the average laser output and the extiction ratio [12]. [10] reports optical feedback for LED backlight stabilisation. Therefore this research will investigate the introduction of optical feedback to correct ageing and non-uniformities in emissive displays: the pixel's optical output power will be measured and regulated to a desired value.

1.4 Display architecture

As mentioned above the optical measurement required to correct ageing and non-uniformities should be done for each pixel independently. For LED backlights this is easily done by using a single detector [10] as these LED's are ajdacent to the display, however for an intelligent (large area) display it is not possible to measure every pixel with the same measurement circuit. The optical measurement

should therefore be allocated more closely to the pixel and the display architecture should be taken into account. We will discuss two types of display architectures: fully active matrix LAD's and modular LAD's.

Active Matrix In an active matrix display, the display is divided in rows and coloms. Each pixel has a small TFT circuit that can drive the pixel. Figure 1.7 shows a typical TFT circuit for an active matrix (O)LED display. When the row select signal becomes high, capacitance C is charged with V_{data} and transistor T_3 will work as a current source for the (O)LED. When the row select signal becomes low again, capacitance C holds $V_{gs,T_2} = V_{dd} - V_{data}$ and the (O)LED remains driven with the same current. By changing V_{data} the emittance of the pixel is regulated.

For an active matrix display the main driver electronics, which will generate the correct voltages on the column line and the row select signals, are peripheral to the display. To measure each pixel optically, the photodetector should be located within the active matrix. This means the simple 2 transistor circuit of Fig. 1.7 will be extended with at least a photodetector and generally with a few transistors as well, thus reducing the aperture ratio of the pixel. This detected signal might then be read out by the display driver or can be used as a feedback signal for a feedback loop in the active matrix itself creating a "smart" pixel. In recent literature [7, 13, 6, 14, 8, 15] especially active matrix OLED displays have recieved a lot of attention towards solving non-uniformities with a "smart pixel" approach. Note that these active matrix displays have a (relatively simple) optical feedback mechanism in the active matrix which is driven from a pheripheral driver IC that produces the required timing signals and (high) driving voltages.

Modular Display Large area displays (LAD) with high brightness, such as LED walls often have a modular architecture. The display consists of seperate modules of smaller size that can be concatenated together, with each of these modules gifted with enough intelligence to work independently. In our research group, other research to-

wards fully modular displays is currently conducted [16, 17]. Modular displays have the obvious advantages of free form, scalablity and much loser production constraints. The critical dimension of the LAD is in fact reduced to that of a single module, allowing for less expensive production with possibly higher yield. For example [17] reports a passive matrix display with high contrast and large scale. Alt-Pleshko's law prohibits large passive matrixe displays with high contrast but in modular displays only the module size is limited by Alt-Pleshko's law. The adressing scheme for a single module on the other hand can be active matrix or direct adressing (a single connection from the driver to each pixel). In this work we will focus on such an modular display architecture where we will choose the module size small enough for integrated optical feedback within the driver IC, removing the need for any external circuits such as optical detector or feedback circuit. There are mainly two possibilities:

- A sigle pixel - single driver (SPSD) approach. Here the module size is actually 1 pixel. This approach was proposed in the FP6 IST Nanopage project. Each pixel recieves it's own dedicated driver IC with complete intelligence: optical feedback, configurability, grayscale reproduction, adressablility,...
- A multi pixel - single driver (MPSD) approach. A more standard modular display approach where the optical feedback circuits is integrated in the driver IC but the module is small enough so one driver IC can provide optical feedback for all module pixels. This approach allows bigger module size but requires a more complex feedback loop. Indeed, as one driver IC can measure different pixels two problems arise:

    1. As each pixel's optical signal must be measureable, the driver IC can not be shielded from ambient light as might be possible for a single pixel - single driver approach or an active matrix display. Ambient light will influence the measurement and therefore needs to be cancelled out.
    2. As all the pixels will generate a feedback signal, feedback can only be performed for a pixel while the other pixels on the module do not change their state (on or off). The

ambient light cancellation circuit should then be able to determine the usefull signal. This means no continuous feedback is possible and fast output variations will not be compensated.

1.5 Calibration

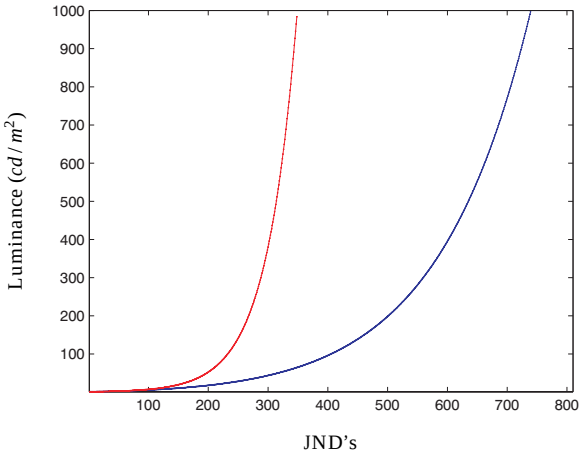
In previous section we stood up for an intelligent display with an integrated optical feedback in order not having to recalibrate the display over and over. However as mentioned, only by distributing the measurement system this can be established. In an active matrix display the photodetector will be allocated in the active matrix display on a pixel-level and for a modular display every driver IC preforms it's own measurement. Sadly each measurement system has it's own characteristics and errors which are not known in advance. In an active matrix TFT variations are always present ([7]) and for a driver integrated measurement IC parameters such as mobility, resistance, offset,... will be different for each IC. Every conversion from voltage to current or to time in an IC is always dependent on these physical parameters and resistor values, capacitance values are only 20% precise. These variations might however be cancelled out with a build in auto calibration as long as an absolute quantity is available to every measurement system (e.g. a clock frequency, a voltage,...).

However, as the coupling of light into the IC might be very dependent on IC placement and photodetector quantum efficiency variations occur [7], each measurement would still be incomparable to another. Actually by adding distributed optical feedback the non-uniformity problem is shifted from the display technology to the TFT backplane or driver technology. These technologies have the advantage that they are more stable over time and temperature. An active matrix measurement / feedback systems being more approximate to the emissive pixel, will still be influenced by the temperature of the emissive pixel. In this work we focus on a driver integrated measurement / feedback system. As the driver IC is often seperated from the actual emissive pixel, driver temperature issues are less important. Furthermore the driver electronics can be made rather

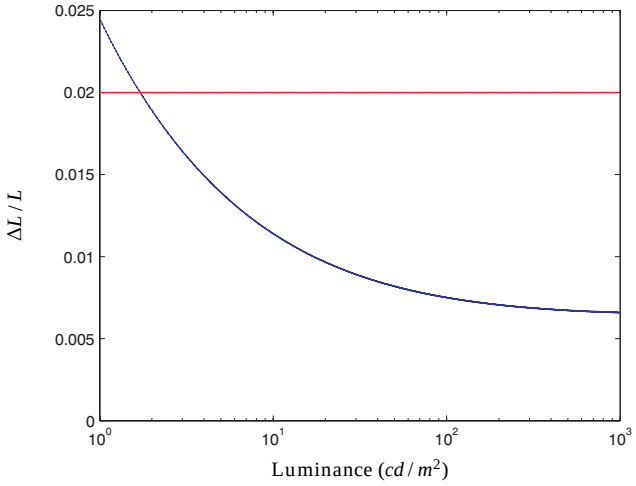
intelligent (and larger) to adress these issues, which is of course not possible for a display technology nor an active matrix circuit (as this would decrease the aperture ratio of the pixel). This work will however not focus on ageing or temperature related problems of the driver IC technology. But even then, in order to compare the different measurements to each other and adress non-uniformities, the different measurement systems (driver IC's in this work) or the whole "driving circuit - pixel" system should be calibrated. An initial calibration of the display remains necessary to remove initial non-uniformities in the display.

Once the display has been calibrated no initial non-uniformity remains and ageing and temporary non-uniformities can now be adressed pixel-based. As the initial calibration removes all deviations and errors between the different measurement systems, each driver IC or active matrix feedback loop can now work seperatly and adress output power changes (with corresponding measurement value change) differentially to the calibrated measurement value. Mark that this calibration measurement is not necessarily an absolute one, it simply must be equal for all pixels so the measurements values of different pixels are comparable to one another. Thus by an absolute measurement of only one pixel, all the others can be calibrated to a certain absolute power as well.

These considerations lead to an important consequence for the display driver: for a modular display with individual independent drivers to provide an optical (or other) feedback, each driver must be configurable to calibrate for initial differences. The possibility of driver calibration implies that the driver IC must have a tunable parameter in its feedback loop. As this calibrated value should remain known during the entire liftetime of the display, it should be stored (either on-driver or off-driver, see Sect. ???) and therefore a digitalisation is necessary. However, the way this calibration is implemented will depend on the chosen driver architecture or with other words: how is the display driven to implement correct grayscaling?



(a)



(b)

Figure 1.2: Comparison between Weber's law and the DICOM model. (a) gives the luminance as a function of the JND's for Weber's law and DICOM. Weber's law clearly underestimates the discriminating power of the HVS compared to the DICOM measurements. (b) shows $\Delta L/L$ as a measure for percievable non-uniformity for Weber's law and DICOM. The 2 % rule is clearly not sufficient according to the DICOM measurements.

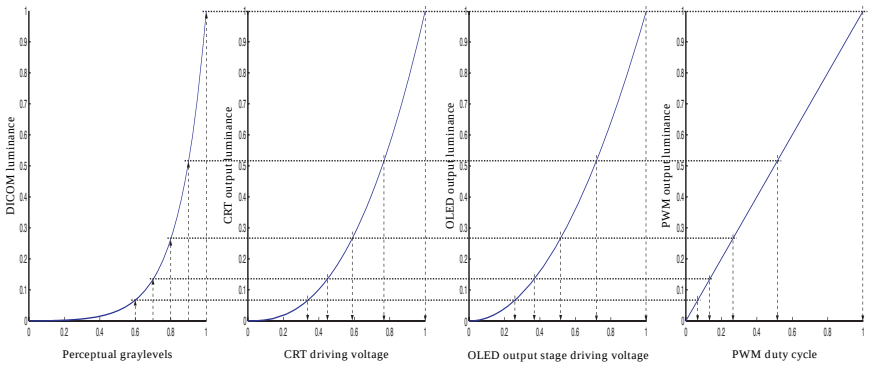


Figure 1.3: Mapping of the perceptual DICOM graylevels to the correct driving signals for a AM driven CRT, a AM driven LCD and a PWM driven display. All quantities are normalised.

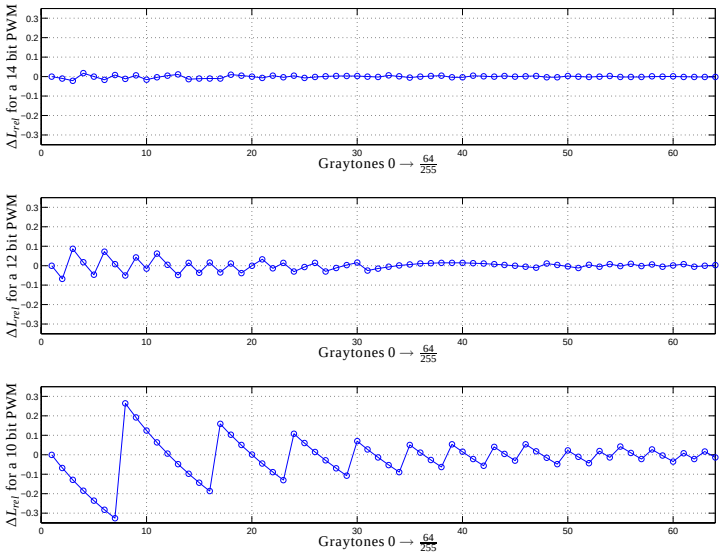


Figure 1.4: Relative Error ΔL_{rel} for linear PWM with different precision: 14, 12 and 10 bit. ΔL_{rel} increases sharply with decreasing precision of the PMW.

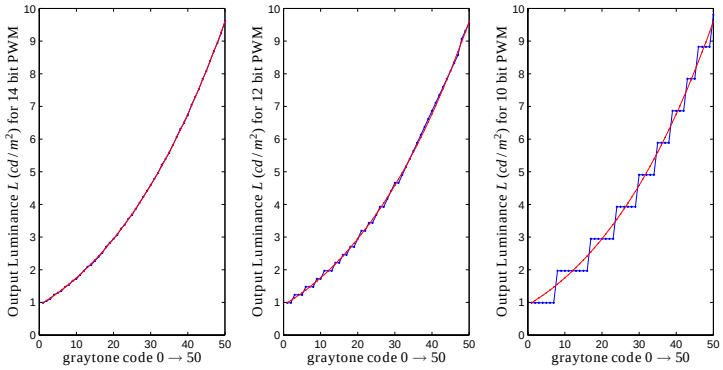
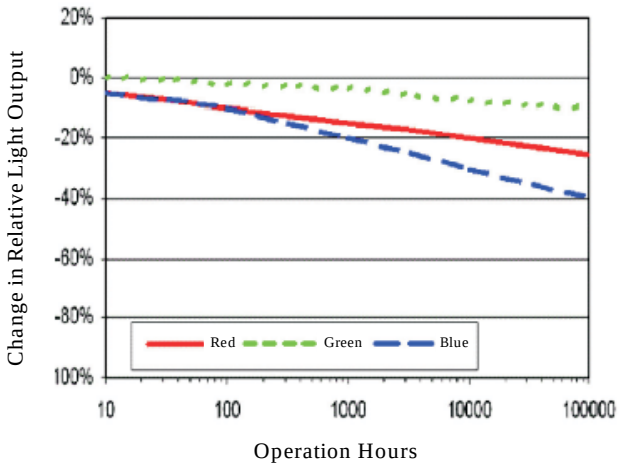
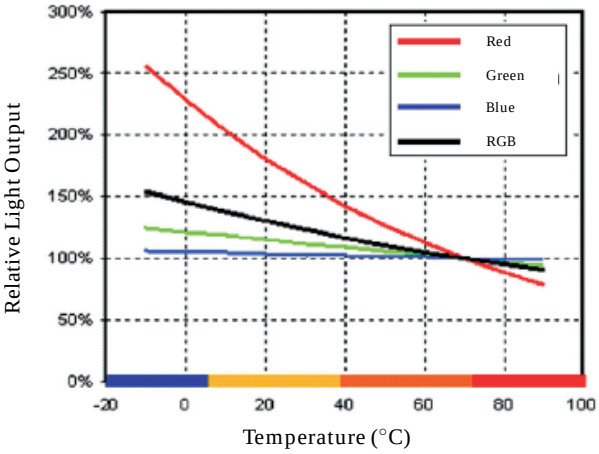


Figure 1.5: Output luminance L_{PWM} for different precisions of the linear PWM (14, 12 and 10 bit) for an 8 bit graytone reproduction. For less than 14 bit precision different graytones will generate the same PWM code and graytone reproduction precision is lost.



(a)



(b)

Figure 1.6: Influence of (a) operation time and (b) substrate temperature on RGB LED output [10]

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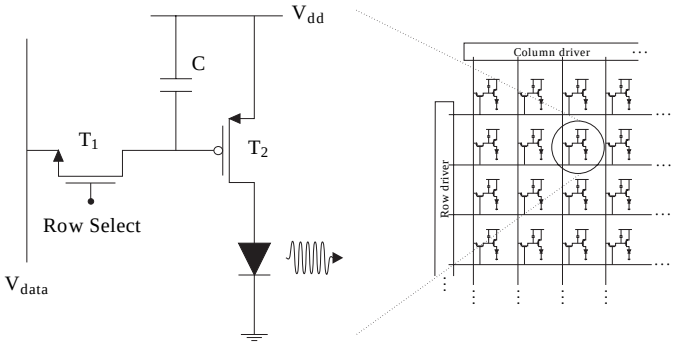


Figure 1.7: Active Matrix (O)LED current source circuit. Each pixel has a small circuit that provides a basic sample and hold function. When the "row select" signal is high, V_{data} will be stored on C and T_2 will be activated, sourcing the appropriate current through the (O)LED.

2

Driving Technique Considerations

To introduce grayscaling for displays, the two most common types of driving are Amplitude Modulation (AM) and Pulse Width Modulation (PWM). With AM the on-time of the pixel remains constant and grayscaling is obtained by making sure the pixel's output power is changing with the amplitude of the driving signal. For example the (O)LED current magnitude can be altered to obtain a different light output. In liquid cristal displays (LCD) the amplitude of the AC driving waveform will be altered. Basically, the output power of the pixel is an arbitrary function of the amplitude A of the driving signal and the emitted light energy is given by:

$$E = p(A) \cdot T_{on} \tag{2.1}$$

PWM keeps the magnitude of the output power constant, but changes the on-time T_{on} of the pixel to achieve the same goal. This chapter will give a few important considerations concerning the driving technique used. Furthermore we discussed in previous chapter the need for uniformity and the introduction of optical feedback. When chosing between AM and PWM driving, the influence

on uniformity and the compatibility with optical feedback should be taken into account.

2.1 HVS related considerations

A first consideration is wether there are constraints from a HVS point of view for any driving technique. A PWM display is driven by flashes with different length: the pixel is on or off for a longer time in order to generate grayscaling. This way the average emitted optical energy in a frame is the same as in a AM case. Bloch's law [18] states that light flashes with different duration or magnitude, but equal total energy, are indistinguishable below 30ms. This means PWM is a valid display driving method as long as the "refresh time" after which a new PWM period is started is smaller than 30ms. However, the HVS is very sensitive towards flashes of light, which is exactly what PWM does. In order not to percieve these successive periods as seperate flashes, the rate has to be above the critical flicker fusion frequency (CFF). [18] mentiones a 60Hz refresh rate is enough for normal illumination levels. [19] mentiones the CFF for a certain luminance L is given by:

$$CFF = 12.5 \cdot \log_{10}(L) + 37 \tag{2.2}$$

For a 1000 cd/m^2 display luminance we find $\approx$ 75Hz refresh rate. Commercial displays often use 50Hz or 60Hz refresh rates to avoid power-line interferences. In this work we will always consider a 60Hz refresh rate ($\approx$ 16.6ms frame) unless otherwise mentioned.

Another important issue for PWM driven displays are motion artefacts. The easiest way to implement PWM is by making binary weighted subframes. Figure 2.1 shows for 8 bit PWM precision how the duty cycle of the first subframe is $T_{fr}/255 = LSB$. The second subframe has a duty cycle of $2^1 \cdot LSB$, the third $2^2 \cdot LSB$, etc. With this approach a very simple bitwise graylevel code implementation is possible and is (was) used in PDP and DLP displays. Because of the subframes the display only needs to be adressed once for every subframe and a simple 1 or 0 is required. This makes this PWM

type ideally suited for active matrix displays. However, it generates dynamic false contouring.

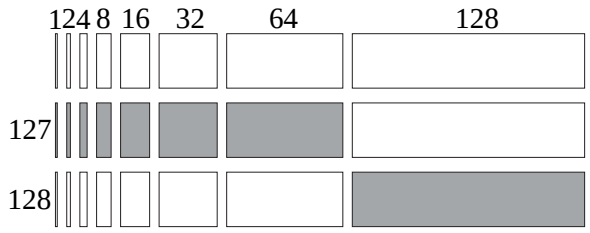


Figure 2.1: Binary weighted PWM used in active matrix displays such as PDP or DLP

Consider values 127 and 128 for an 8 bit PWM as represented in Fig. 2.1. One can see that a pixel with value 127 will emit light in the first half of the frame, a pixel with value 128 will emit in the second half of the frame. The problem arises when a moving image is displayed with these values next to each other. As the picture moves and the observer tracks this image with his eyes, the temporal discontinuity between the values 127 and 128 is transformed to a spacial discontinuity. If the image moves fast enough, this temporal gap will lead to a spacial gap (or overlap), meaning black (or bright) stripes will occur. Figure 2.2(a) shows a simple example where an image of 4 pixels is shifted to the right on the display at 1 pixel per frame ([20]). The line exists of two pixels which emit at the 128th level and two that emit at the 127th level. On Fig. 2.2(b) a space-time diagram fixed to the retina of the observer is shown. As the observer tracks the image, a gap occurs resulting in a dark disturbance shown in Fig. 2.2(c). Dynamic false contouring can be solved with special algoritms or pixel placement [20, 21]. In this work the constraints of an active matrix adressing do not apply as the whole driver is located at pixel level. Therefore using PWM which linearly adjusts the on-time of the pixel, in stead of bitwise implementation, is possible and will give fewer motion artefacts.

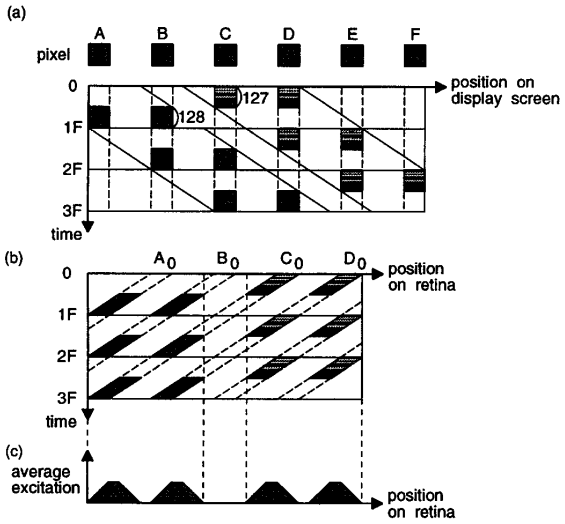


Figure 2.2: Dynamic false contouring for a binary weighted PWM driven display. Black stripes occur for a tracking observer due to temporal discontinuities.[20] Interpretation: the observer tracks the displayed "line" shown in (a) by following the diagonal lines in (a). This means a pixel value that scrolls over the display (in time) is projected on the same position on the retina (in time).

2.2 Driver IC

From a driver IC point of view, PWM is preferable to AM. If direct amplitude modulation is used to generate grayscaling, the driving signal (voltage or current) should be adjustable to the desired values. Some display technologies do not work at standard CMOS voltages: [22] reports 50V to 100V driving voltage for a carbon nanotube (CNT) based field emission display (FED) and OLED displays often use higher voltages up to 30V to set the OLED current [23]. The design of a complex analog high-voltage output stage increases IC size and cost drastically. PWM on the other hand is easily implemented in a digital form. Duty cycle or switching times can easily be derived from a clock with a simple digital counter. Thus we avoid a space consuming digital to analog converter (DAC) to scale the driving signal. Note that in Chapt. 1 we derived the NOB n for monotonous

and distinguishable grayscaling, listed in Table 1.1. A n bit counter would be sufficient. Table 1.2 listed the NOB required for uniformity, where we assumed an error of 1/2 LSB might be possible. However, for a digital implementation, it is clock skew, clock jitter,... that determines the error and the error will be much lower than half a clock periode. Therefore Table 1.2 is much too stringent for a digital implementation. We will discuss this further in Chapt. 4. Furthermore PWM requires a simplified output stage as only switching between the on- and the off-signal value is necessary. For example a simple switch or a push-pull output stage might be sufficient.

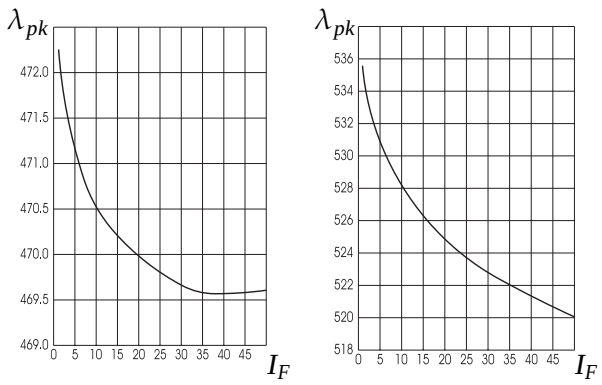
2.3 Uniformity

Also from a uniformity point of view PWM grayscaling is preferable. An advantage of PWM is the fixed working point of the pixel. As the driving signal is kept constant, no shift in emissive characteristics will occur. This is a major problem for InGaN LEDs. Figure 2.3 shows the shift in dominant wavelength λ_{pk} of a green and blue OSRAM LED as a function of forward LED current I_F [24]. With AM the LED current I_F is changed to generate grayscaling and thus the wavelength shift will occur. PWM on the other hand switches the LED on or off but always with the same I_F. Therefore, no working point induced color shift will occur. Other technologies might not have such a pronounced working point dependency, but generally a constant working point is always preferrable.

2.4 Adressing and response time

Often however, PWM grayscaling is not possible for a certain display technology. The line scanning approach of a CRT means only a short current burst can reach each pixel during a frame time. Therefore only the amplitude of this current can be used to dim the pixel.

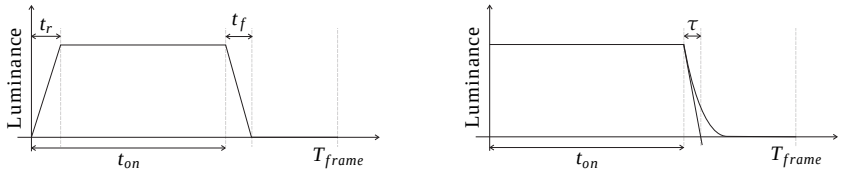
Also a display technologies response time should allow PWM's short pulse durations. For a display with 60 Hz refresh rate and a 10 bit PWM dimming, the shortest PWM pulse would be 16μs. For



(a) Blue InGaN LED (b) Green InGaN LED

Figure 2.3: Wavelength shift because of driving current for a (a) blue and a (b) green OSRAM LED. [24]

LEDs response times of 100ns are common [25], but for OLED typical response times of 10μs have been reported [26] and phosphor decay times of tens of μs exist [27, 28], but are often much larger. As the response time of the pixels becomes important to the PWM pulse duration, non-linearity occurs. For a display to remain perceptually uniform, this error should lead to an error smaller than 1 JND or its presence should be taken into account. Figure 2.4 shows two possible models for switching time errors: Fig. 2.4(a) deals with a simple model with linear rise and fall times, used for LEDs [25] and Fig.



(a) Linear switching edges for LED switching (b) Exponential decay for phosphors and OLED

Figure 2.4: Basic switching models for LED and phosphor / OLED based displays. The rise, fall and decay time will distort the average PWM output and should or be small enough, or be taken into account!

2.4(b) uses a typical OLED / phosphor exponential decay where the rise time is neglectable compared with the decay time. With Eqn. (1.17) for linear PWM ($\gamma = 1$), the average output power during a frame (T_{frame}) for a LED can be written as

$$L_{PWM}(k) = (L_{\max} - L_{\min}) \cdot \frac{\left(\frac{k}{2^n-1} T_{frame} + \frac{t_f - t_r}{2}\right)}{T_{frame}} + L_{\min} \quad (2.3)$$

Due to the rise and fall times of the LED an error is made which should be small enough to preserve monotonic, distinguishable and uniform grayscaling.

In Table 2.1 half of the maximum allowed difference between LED fall and rise times ($= \Delta t/2$) for different $L_{\max}$ with $L_{\min} = 1cd/m^2$ is listed. We chose the error $\Delta x/2 = 0$, meaning that Table 2.1 lists best case values. [25] mentiones measured values of $\Delta t = 200$ns for LEDs, which is sufficient. There is therefore no need to take the fall and rise times of LED's into account when calculating the appropriate k-values.

For a simple exponential decay model an upper boundry for the error can be written as:

$$\frac{(L_{\max} - L_{\min})}{T_{frame}} \cdot \int_{t_{on}}^{T_{frame}} e^{-\frac{(t-t_{on})}{\tau}} < \frac{(L_{\max} - L_{\min})}{T_{frame}} \cdot \tau \quad (2.4)$$

As this error should be smaller than 1 JND, Table 2.1 shows the maximum allowed τ for different $L_{\max}$. It is clear that these values are much lower than the achievable decay times found in literature.

In order for technologies with exponentially decaying output power to implement a meaningfull PWM driving scheme, the output contribution of the "decaying tail" should be included in the calculations when deriving the PWM value k that yields the correct output luminance. The possible error that occurs then is only the deviation on this "decaying tail", which is almost neglectible (see Sect. 3.2 for a thorough investigation including optical feedback). However in order to achieve the smallest luminance levels for the lower graylevels, the minimum output power of the display should

be small enough. The minimum output power will be:

$$L_{\min} \approx \frac{(L_{\max} - L_{\min})}{T_{frame}} \cdot \tau + \frac{(L_{\max} - L_{\min})}{2^n - 1} \tag{2.5}$$

Table 2.2 shows the maximum allowed decay constant when using the PWM precisions found in Tables 1.1 and 1.2. Once more we omitted the error $\Delta x/2$ and these are best case values. It is seen that for high end displays with high brightness and 8 bit perceptual grayscaling, too small decay times are necessary. However commercial displays (not LED!) for example only use 8 to 10 bit PWM, corresponding to only 6 bit perceptual grayscaling (see Table 1.1 on p. 12) and larger (and more important, feasible) decay times are allowed. Note however that PWM is not widely used for OLED or FED displays because of this exponential decay. As for AM driving the problem does not arise, it is preferred for slower display technologies.

100	500	1000	4000
4.1 μs	810 ns	400 ns	100 ns

Table 2.1: The maximum allowed decay constant for a PWM driven display so the error would not be noticable. NOB perceptual grayscaling and $L_{\max}$ are swept. It is clear these values are much too low. Therefore the decay contribution should be considered when calculating the appropriate k-value (see Eqn. (1.17)).

	100	500	1000	4000
6	27 μs	11 μs	6.7 μs	2.3 μs
7	12 μs	4.3 μs	2.6 μs	0.93 μs
8	2.5 μs	1.9 μs	0.92 μs	0.35 μs

Table 2.2: The maximum allowed decay constant so all graylevel luminances can be produced as a function of the maximum luminance and the desired NOB perceptual grayscaling. Higher end applications find it hard to implement PWM!

2.5 Ageing

An important question is wether the chosen driving scheme will influence the ageing process of a pixel. The impact of the driving scheme (PWM or AM) on the lifetime of a display technology is way beyond the scope of this research, but also in academic and technical literature almost no studies were found concerning this topic. Only for LED driving some studies concerning lifetime degradation under pulsed driving and DC driving were found [29, 30]. It was found that pulsed driving of the LED with duty cycles $< 50\%$ drastically reduces the LED lifetime compared to DC driving, *if equal average current was used.* For duty cycles $> 50\%$ however, prolonged lifetime was found. However this measurement implies that for small duty cycles high peak currents are applied, whom are damaging the device. For PWM grayscaling however this is not the case as the peak current is the same as the maximum AM current through the LED (full brightness). [29] mentiones no acceleration in performance degradation for PWM driven LEDs if the peak currents do not exceed the maximum recommended DC value.

2.6 Feedback and driver architecture

In previous section we found no evidence that favoured either technique considering the ageing speed, however PWM uses a constant working point and should result in a more uniform display. As mentioned in Sect. 1.3 regardless of the grayscaling driving technique (PWM or AM) optical feedback will be necessary. The driving technique used for grayscaling should therefore be suited to implement integrated optical feedback.

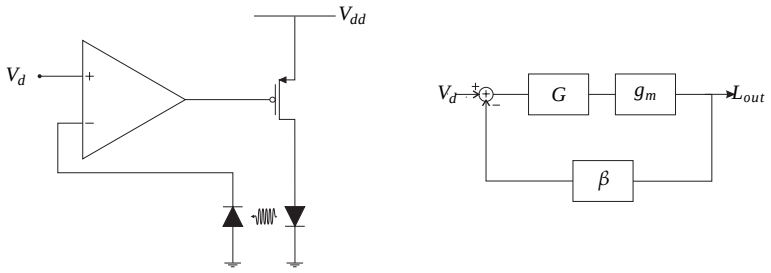
Figure 2.6 shows an implementation of a (O)LED AM driver with optical feedback and the equivalent model. The gain of the amplifier makes sure the feedback signal remains equal to the desired value V_d:

$$L_{out} = \frac{G \cdot g_m \cdot a}{1 + \beta \cdot G \cdot g_m \cdot a} V_d \overset{G \gg 1}{\approx} \frac{V_d}{\beta} \tag{2.6}$$

Note that the output stage was linearized around its working point $g_m \cdot a$. The ageing of the pixel is expressed in parameter $a \in [0,1]$, modeling a loss in conversion efficiency from electrical to optical power. The feedback path will generate an electrical signal from the optical output power. As mentioned in Sect. 1.4 for a modular display architecture, gain parameter $\beta \in [1, \beta_{\max}]$ models the variation due to coupling differences, IC characteristic deviations,... As given by Eqn. (2.6) the output luminance is proportional to the input signal V_d. Grayscaling can be implemented by changing V_d and thus V_d should have the resolution mentioned in Tables 1.1 and 1.2 on p. 12 in order to obtain display uniformity.

Using amplitude modulation for grayscaling means however the dynamic range of the optical feedback signal will be very high. For a modular display as in this work, this dynamic range is even extended by a factor $\beta_{\max}$. As we try to integrate the optical detector in the driver IC, the detector size should be as small as possible (e.g. only a few mm^2). Furthermore, only a small fraction of the emitted light will reach the detector, especially in a multi-pixel modular approach. Therefore even at maximum power with $\beta_{\max}$, small detector signals of a few μA are to be expected. For a display with $L_{\max} = 500$ and $\beta_{max} = 10$, this would mean the smallest feedback current would be only a few nA! In order to maintain display uniformity, the maximum allowed equivalent noise current from the driver electronics would be extremely small as will be shown later in this work.

With PWM grayscaling on the other hand, the pixel is always driven by a high driving signal. Therefore the feedback signal's magnitude will only vary over a factor $\beta_{\max} \cdot a$. For PWM grayscaling the ageing of the pixel will also determine the magnitude of the feedback signal, unlike with AM grayscaling. This range will however be much smaller than for AM grayscaling. Actually we exchanged dynamic range for bandwidth as with PWM grayscaling the feedback signal is larger but it's duration is shorter. As will be discussed in following chapters this is less of a problem compared to the necessity of a huge dynamic range.



(a) (b)

Figure 2.5: AM optical feedback for (O)LED. (a) shows a circuit implementation and (b) shows the corresponding model.

2.7 Feedback and ageing

Until now we only considered the grayscaling driving technique. As optical feedback adjusts the light output of the pixel, it can also adjust either the driving signal magnitude or the on-time of the pixel. Let us for example focus on AM optical feedback for a LED. As the LED ages, the magnitude of the LED current can be increased so the optical output power remains constant. However, higher current trough the LED will accelerate the aging process. As the LED ages faster, the LED current will increase faster and faster until either the driver's or the LED's limitation is reached. It is clear that all feedback mechanisms have only a limited ability to extend a display's lifetime. In this section we will try to determine this limitations for both PWM and AM feedback on the basis of two ageing models: exponential ageing for (mostly) OLED and Pfahln's metric for phosphor ageing.

2.7.1 Exponential ageing model

Figure 2.6 shows the ageing curves of an OLED pixel at constant current mode ([6]). A pixel which is driven with a higher current and thus higher output luminance ages much faster than a pixel with lower output luminance. In fact the output variation as a function

of the driving time t_{on} of the pixel can be written as [6, 1, 31]:

$$L(t) = L_0 \cdot e^{-\frac{t_{on}}{\tau}},\ with\ \tau \sim \frac{1}{L_0} \tag{2.7}$$

where $L_0 = L(0)$. The same characteristics are found for some FED and white LED phosphors [32, 33]. As we found no general models for high brightness color LED ageing [29], we will focus on exponential ageing given by Eqn. (2.7). In the above equations t_{on} represents the time the pixel is actually driven as the pixel will only age if it emits light. For amplitude modulated optical feedback, the pixel is driven constantly and the on-time is also the elapsed time. But for pulse width modulated feedback, this on-time is only a fraction of the frame-time and is gradually increased. Therefore there is no identity between the on-time and the actually elapsed time.

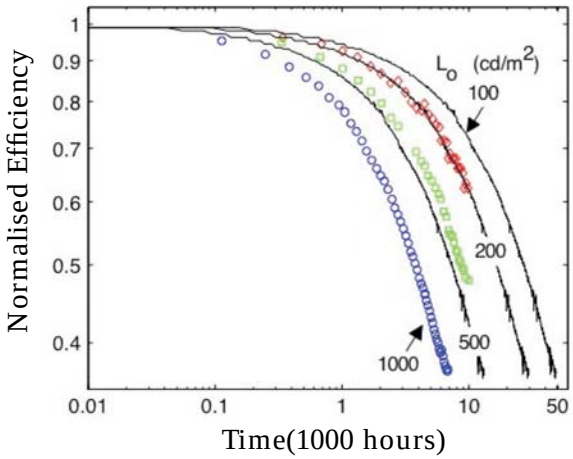


Figure 2.6: Luminance degradation of three identical phosphorescent OLEDs operated at different initial brightness of 200 cd/m^2 , 500 cd/m^2 , and 1000 cd/m^2 is reproduced from [1] (data points) and is compared to projections of luminance degradation (solid lines) determined by scaling the luminance output of the device that is operated at L = 1000 cd/m^2 . Each of the three devices is operated in a constant current mode.

AM feedback

Note that for a display the different graylevels (different L_0) will result in different ageing speeds. We will examine the worst case scenario of the highest graylevel. Let us focus on AM feedback for OLED. Say the desired optical output energy during a frame is $L_d \cdot T_f$. The OLED driving current resulting in L_d should be lower than the maximum allowed driving curren of the pixel, because the feedback will increase this current to compensate for the ageing. Therefore chosing $L_d = L_{\max}/\gamma$ means the maximum gain for the AM feedback is γ. With $t_{0.5}^{L_{\max}}$ being the on-time after which the output is only $1/2 \cdot L_{\max}$ and $\tau \approx 1/L_0$, we can write:

$$\begin{aligned} \tau_{L_{\max}} &= \frac{t_{0.5}^{L_{\max}}}{\ln(2)} = \frac{c}{L_{\max}} \\ \Rightarrow \quad L(t) &= L_0 \cdot e^{-\left(\frac{\ln(2)}{L_{\max} \cdot t_{0.5}^{L_{\max}}}\right) \cdot t \cdot L_0}, \quad \forall L_0 \in [0, L_{\max}] \end{aligned} \tag{2.8}$$

Let us normalise $t_{0.5}^{L_{\max}} = 1$ and $L_{\max} = 1$. On $t = 0$ with $L_0 = L_d = L_{\max}/\gamma$, the pixel output power without optical feedback is given by:

$$L(t) = \frac{1}{\gamma} \cdot e^{-\frac{\ln(2)}{\gamma} \cdot t} \tag{2.9}$$

After a time dt however, the output power will have diminished to

$$L(dt) = \frac{1}{\gamma} \cdot e^{-\frac{\ln(2)}{\gamma} \cdot dt} \tag{2.10}$$

and therefore the AM feedback will increase the current through the led so the output power remains constant. The gain $g(dt)$ is given by

$$g(dt) = e^{\frac{\ln(2)}{\gamma} \cdot dt} \cdot g(0) = g_1 \cdot 1 \tag{2.11}$$

and the new ageing curve is now

$$L(t)|_{t \geq dt} = \frac{1}{\gamma} \cdot \left(e^{-\frac{\ln(2)}{\gamma} \cdot dt} \cdot g_1 \right) \cdot e^{-\frac{\ln(2)}{\gamma} \cdot t \cdot g_1} = \frac{1}{\gamma} \cdot e^{-\frac{\ln(2)}{\gamma} \cdot t \cdot g_1} \tag{2.12}$$

The pixel will age faster because of the g_1 in the exponent. Similar to Eqn. (2.12) a general discretisation between t and $t+dt$ gives:

$$L(t+dt) = \frac{1}{\gamma} \cdot e^{-\frac{\ln(2)}{\gamma} \cdot \overbrace{dt \cdot g(t)}^{dA}} \tag{2.13}$$

In continuous time, this means the output luminance will be given by:

$$L(t) = \frac{1}{\gamma} \cdot g(t) \cdot e^{-\frac{\ln(2)}{\gamma} \cdot A(g(t))} \tag{2.14}$$

Calling the exponent in Eqn. (2.13) $dA = dt \cdot g(t)$ we find:

$$\frac{dA}{dt} = g(t) \Rightarrow A(t) = \int_0^t g(\varepsilon)\, d\varepsilon \tag{2.15}$$

and the output power can be written as:

$$L(t) = \frac{1}{\gamma} \cdot g(t) \cdot e^{-\frac{\ln(2)}{\gamma} \cdot \int_0^t g(\varepsilon) d\varepsilon} \tag{2.16}$$

Above equation is easily understood: after a while the momentary driving signal is amplified by the momentary gain so output power remains constant. However, the ageing curve is the result of the whole lifetime where different gains (and thus ageing speeds) where valid and an integration is necessary to account for previous behaviour.

For AM feedback the goal is to keep $L(t) = L_d = 1/\gamma$ by changing the gain. Thus we find $g(t)$ as a solution for

$$\frac{1}{\gamma} \cdot g(t) \cdot e^{-\frac{\ln(2)}{\gamma} \cdot \int_0^t g(\varepsilon) d\varepsilon} = \frac{1}{\gamma} \tag{2.17}$$

$$\Leftrightarrow \quad g(t) = e^{\frac{\ln(2)}{\gamma} \cdot \int_0^t g(\varepsilon) d\varepsilon} \tag{2.18}$$

$$\Leftrightarrow \quad \ln(g(t)) = \frac{\ln(2)}{\gamma} \cdot \int_0^t g(\varepsilon)\, d\varepsilon \tag{2.19}$$

$$\Leftrightarrow \quad g'(t) = \frac{\ln(2)}{\gamma} \cdot (g(t))^2 \tag{2.20}$$

With $g(0) = 1$ we find

$$g(t) = \frac{1}{1 - \frac{\ln(2)}{\gamma} \cdot t} \tag{2.21}$$

which is assymptotic for $t = \gamma / \ln(2)$. This means that even if the pixel could be driven beyond $L_{\max}$ without loss of linearity, the optical feedback would only be able to maintain a constant output power during $\approx 1.44 \cdot t_{0.5}^{L_{\max}}$.

As mentioned however, the maximum gain is γ and thus the time t_{fb} for which the optical feedback can keep the optical output power constant is given by:

$$t_{fb} = \frac{\gamma - 1}{\ln(2)} \cdot t_{0.5}^{L_{\max}} < \frac{\gamma}{\ln(2)} \cdot t_{0.5}^{L_{\max}} \tag{2.22}$$

Higher γ obviously means a longer lifetime as the initial output power is less. Keep in mind that lower initial output power also means a larger dynamic range for the driving signal and more stringent noise threshold is necessary for the driver IC circuits!

PWM feedback

For PWM optical feedback, the pixel is operated at high brightness for some fraction of the frame time, which is slowly extended as the pixel ages and loses efficiency. When the on-time of the pixel exeeds the frame time, the display's maximum lifetime is reached. As mentioned in previous paragraph this high brightness "overdriving" of the pixel will accelerate the ageing process. [6] therefore proposes AM feedback as a better option also because at higher current densities, OLED quantum efficiency is lower. Whereas the last argument is a valid one, the higher brightness overdrive nor the limitation of the frame time give any different results from the above presented calculations if we assume a pixel only ages when emitting light. For PWM the pixel is on only a fraction of the frame time T_f. The initial fraction being T_f / γ. However, as the pixel ages this on-time is increased with a gain factor $g(t)$. The optically emitted output energy

can thus be given by

$$E_{out} = \int_0^t L_{\max} \cdot e^{-\left(\frac{\ln(2)}{t_{0.5}^{L_{\max}}}\right) \cdot On(t)} \cdot \frac{g(t)}{\gamma} dt \tag{2.23}$$

Where $On(t)$ represents the actual time the pixel has be emitting light up to time t. Again, the exponent of the ageing curve (i.e. $On(t)$) is dependent on the gain $g(t)$ and it's evolution up until t. On $t = 0$ when no ageing has occured the relation between actual on-time and actually elapsed time is given by: $\Delta On(t) = \Delta t / \gamma$. After a while however, the on-time is increased with a gain and it can be said that:

$$\begin{aligned} dOn(t) &= \frac{dt}{\gamma} \cdot g(t) \\ \Rightarrow \quad On(t) &= \frac{1}{\gamma} \cdot \int_0^t g(\varepsilon)\, d\varepsilon \end{aligned} \tag{2.24}$$

With Eqn. (2.23) and (2.24) and normalising towards $t_{0.5}^{L_{\max}}$ and $L_{\max}$, the emitted output power is once again given by:

$$L(t) = \frac{dE}{dt} = \frac{1}{\gamma} \cdot g(t) \cdot e^{-\ln(2) \cdot \int_0^t g(\varepsilon) d\varepsilon} \tag{2.25}$$

and the previous conclusions remain valid! Whereas the maximum gain $g(t) = \gamma$ for AM meant a maximum driving signal could be applied, a maximum gain for PWM means the whole frame time is used to drive the pixel. As mentioned in Sect. 2.5 we found no evidence that pulsed driving deteriorates the ageing curve and above reasoning shows PWM and AM feedback are equally capable of extending display lifetime. Only the loss of quantum efficiency at higher currents [6], means AM is the better choice.

Note that we have only given a worst case scenario of a full graylevel. The predicted lifetime for a real display would therefore be higher. Over the lifetime of the display we can safely assume that the graylevels are uniformly distributed, thus a better (but still

rudimentary) estimate of the lifetime of the display would be

$$t_{fb}^{av} = \frac{1}{2^n - 1} \cdot \sum_{i=1}^{2^n-1} t_{fb}^{L_i} \tag{2.26}$$

where n is the NOB perceptual grayscaling and $t_{fb}^{L_i}$ is the obtained lifetime of the display if it would be constantly driven with graylevel i. The luminances L_i are of course dependent on the HVS used. Be

$$L_{\max} = \gamma \cdot L_{2^n-1} = \gamma \cdot (L_i \cdot \chi_i) \tag{2.27}$$

then it can easily be shown that

$$t_{fb}^{L_i} = \frac{\gamma - 1}{\frac{\ln(2)}{t_{0.5}^{L_{\max}}} \cdot \frac{1}{\chi_i}} = \frac{t_{0.5}^{L_{\max}}}{\ln(2)} \cdot (\gamma - 1) \cdot \chi_i \qquad \forall i \geq 1 \tag{2.28}$$

With the expression above Eqn. (2.26) becomes:

$$t_{fb}^{av} = \frac{t_{0.5}^{L_{\max}}}{\ln(2)} \cdot \frac{\gamma - 1}{2^n - 1} \cdot \sum_{i=1}^{2^n-1} \chi_i \tag{2.29}$$

Table 2.3 shows some normalised values of t_{fb}^{av} for $\gamma = 3$ for different output luminances and different NOB grayscaling, to give an idea of magnitude. We assumed different pixels with different maximum output power, but similar decay. Meaning that a pixel for a 1000 cd/m^2 display has a $t_{0.5}^{3000} = 1$ and the pixel used for a 500 cd/m^2 will have $t_{0.5}^{1500} = 2$ and a pixel for a 100 cd/m^2 display gives $t_{0.5}^{300} = 10$. For the linear driver, NOB of Tables 1.1 and 1.2 were used. We added the worst case scenario values too, to put the values into perspective. It is clear the average values will be much higher due to the logaritmic HVS curve which means most of the graylevels have luminances much below the full brightness luminance. [1] mentions OLED lifetimes of 5000 hr at 300 cd/m^2, giving $t_{0.5}^{3000} = 500$ hr. This means according to Table 2.3 an average lifetime of for an 8 bit grayscaling display of 213k hr, 140k hr and 120k hr for 100, 500 and 1000 cd/m^2 respectivily. [34] mentiones FED lifetimes of 10k hr for 400 cd/m^2 which means $t_{0.5}^{3000} = 1300$ hr. According average display lifetimes are 550k hr, 364k hr and 312k hr respectivily.

Another interesting way of formulating Eqn. (2.29) is by maximum achievable output power for a desired lifetime. Equation (2.29) implies that for a display technology to produce a uniform output during a certain lifetime t_{fb}^{av}, Eqn. (2.30) gives the maximum output power for full brightness (L_{2^n-1}) that can be obtained with optical feedback:

$$L_{2^n-1} = \frac{L_{\max}}{\gamma} = \frac{L_{\max}}{\frac{\ln(2)\cdot t_{fb}^{av}}{t_{0.5}^{L_{\max}}} \cdot \frac{2^n-1}{\sum_{i=0}^{2^n-1} \chi_i} + 1} \tag{2.30}$$

2.7.2 Pfahnl's metric for phosphor displays

In previous section we used an exponential ageing curve given by Eqn. (2.7). This curve was found in literature for OLED's, some FED's and some LED's. However most FED phosphors' ageing curve is better discribed by Pfahnl's metric [35]:

$$L(t) = \frac{L_0}{1 + c \cdot N(t)} \tag{2.31}$$

In the above equation the constant c is called the burn parameter of the material and $N(t)$ is the total number of electrons hitting the phosphor. When the pixel is driven with a constant current $N(t) \sim I_0 \cdot t$ where I_0 is the current needed to generate an initial luminance L_0. As the luminance of a phosphor is proportional to the electron current, Eqn. (2.31) can be rewritten as

$$L(t) = \frac{L_0}{1 + c \cdot L_0 \cdot t} \tag{2.32}$$

Consider $L_{\max}$ being the maximum allowed luminance of the pixel, with $t_{0.5}^{L_{\max}}$ the according halftime, then we can write c in terms of these quantities and we find:

$$L(t) = \frac{L_0}{1 + \frac{L_0}{t_{0.5}^{L_{\max}} \cdot L_{\max}} \cdot t} \tag{2.33}$$

With the same reasoning as we used in the previous paragraph we can introduce the optical feedback, with gain $g(t)$ and maximum

gain γ. Similar to Eqn. (2.16) and (2.25) we find after normalising towards $L_{\max}$ and $t_{0.5}^{L_{\max}}$:

$$L(t) = \frac{g(t)}{\gamma + \int_0^t g(\varepsilon)\, d\varepsilon} \tag{2.34}$$

As optical feedback aims to keep $L(t) = 1/\gamma$, above equation yields a solution for $g(t)$:

$$g'(t) = \frac{1}{\gamma} g(t) \overset{g(0)=1}{\Rightarrow} g(t) = e^{\frac{t}{\gamma}} \tag{2.35}$$

With a maximum gain of γ the worst case and average values for t_{fb} are given by:

$$t_{fb}^{L_{2^n-1}} = \gamma \cdot \ln(\gamma) \cdot t_{0.5}^{L_{\max}} \tag{2.36}$$

$$t_{fb}^{av} = \frac{\gamma \cdot \ln(\gamma)}{2^n - 1} \sum_{i=1}^{2^n-1} \chi_i \cdot t_{0.5}^{L_{\max}} \tag{2.37}$$

In Table 2.3 the values for Pfahnl's metric are listed and as Pfahnl's metric defines a slower aging curve, they result in larger values. Figure 2.7 shows the evolution of the gain $g(t)$ for an exponential ageing and for ageing described by Pfahnl's metric for $\gamma = 3$.

2.7.3 Monte Carlo analysis

The values in Table 2.3 are but an estimate of the real ageing as they merely give the average over all brightness levels. In reality of course a will never be continuously driven by the same grayscale. A correct way to simulate the ageing of the pixel and the effect of the optical feedback would be to use information of the display content and calculate the ageing: the statistical distribution of the applied brightness levels can be used to do a Monte Carlo analysis of the ageing. It is obvious that for example a display used for movies will give a very different distribution than one used for data display and a different ageing curve will appear.

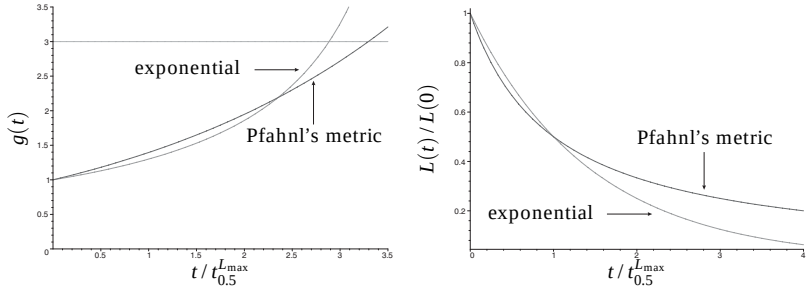
	100		500		1000	
	Exp	Pfahnl	Exp	Pfahnl	Exp	Pfahnl
6	447	509	298	340	261	298
7	432	494	286	328	248	283
8	426	487	280	320	242	277
W.C.	28.85	32.96	5.77	6.59	2.88	3.30

Table 2.3: Achievable lifetime factors $t_{fb}^{av} / t_{0.5}^{3000}$ where the maximum gain γ was kept constant $= 3$. Worst case scenario's are also enlisted to put the values into perspective. Values for an exponential ageing model and Pfahnl's metric for phosphor ageing are listed.

As this simulation was only an afterthought, we did not find the time to analyse the distribution of several content types and simulate the ageing curve of a display based on the ageing models. Figure ... nevertheless shows the results of a single Monte Carlo simulation done on a display with $1000 cd/m^2$ and 8 bit resolution. We simulated a simple uniform statistical distribution of the grayscales, an exponential ageing model and repeated the same simulation 100 times. The grayscale level was randomly altered every frame for a 60Hz refresh rate. As can be seen the Monte Carlo simulated lifetime factor is much lower than the average calculated value! A thorough study with different distributions seems very interesting.

2.8 Conclusion

In this chapter we discussed the two most common driving techniques PWM and AM. Table 2.8 gives a short overview of what are the most important considerations in our opinion. The weight that is given to each of these topics is very dependent on technology and display application. For example for some display technologies the response time constraint of a PWM driver is too stringent for high performance applications. InGaN LED's on the other hand require the constant working point of a PWM driver. In our work we intro-



(a) $g(t)$ for $\gamma = 3$ and $L(0) = L_{max}/\gamma$ (b) Ageing curves for exponential ageing and Pfahnl's metric

Figure 2.7: (b) Ageing of the pixel according to the two models (without feedback) and (a) the gain evolution when feedback is applied. $\gamma = 3$ and $L(0) = L_{max}/\gamma$ were used for these curves.

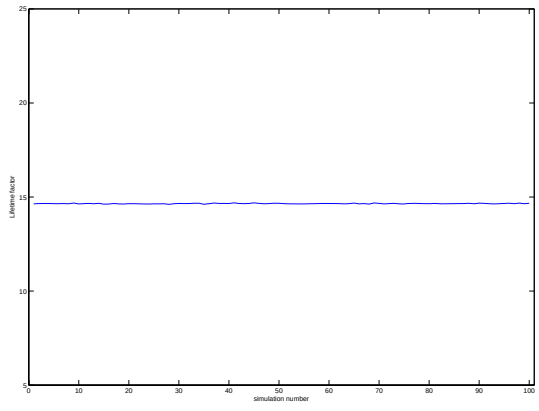


Figure 2.8: Repeated Monte Carlo simulation of the lifetime factor for a 1000 cd/m^2 display with 8 bit perceptual grayscaling.

	PWM	AM
IC output stage	Less complex	More complex
Working point	Constant	Changing
Techn. Response time	Very fast	Slow
Fb. IC integration	Large fb. signal	very small fb. signal

Table 2.4: Overview of the most important differences between AM and PWM driving and their influence on display quality and driver IC.

duced the optical feedback for a modular display. As mentioned AM grayscaling results in very small optical feedback signals for an integrated solution and in order to lower the disign constraints we chose to implement optical feedback on a driver with PWM grayscaling. For the optical feedback loop itself we also chose PWM so the simplicity of the driver output stage remains.

In our choice of a PWM grayscaling driver Sect. 2.1 mentiones the PWM grayscaling should not use binary scaled subframes to reduce dynamic contouring. Sect. 2.4 showed that it is best to generate the graylevels by switching on and off only once as this reduces the switching errors. Sect. 2.7 showed that feedback can only expand the display's lifetime with a certain factor. PWM and AM seem to be equally efficient and equations were derived.

3

Optical feedback circuit design

In previous chapters we mentioned the need for optical feedback to reach sufficient uniformity during the display's lifetime. However the implementation was found to be very dependent both on grayscale driving technique and display architecture. In Chapt. 2 we compared PWM and AM grayscaling and concluded that PWM is a better choice for a modular display. As PWM is inherently linear, Chapt. 1 showed that high resolution PWM is necessary to obtain perceptual grayscaling. With the choice for PWM grayscaling made, this chapter will describe the architecture of the driver IC.

3.1 Standard optical feedback

3.1.1 Circuit description

Let us focus on Fig. 3.1 which shows the easiest way to obtain optical feedback. We proposed this circuit in [36] but also [7] uses a similar implementation. A capacitor with capacitance C is charged to a voltage V_{dac}. When the pixel is turned on, the photodetector

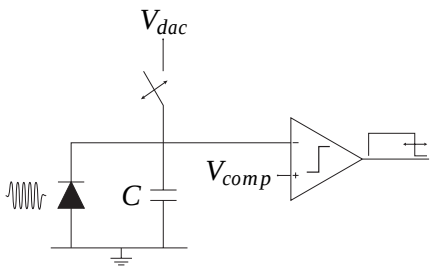


Figure 3.1: Proposed circuit for optical feedback. Grayscaling and optical feedback are applied by PWM.

(a photodiode in Fig. 3.1) will sink a photocurrent i_{ph} proportional to the incident light. This photocurrent will discharge the capacitor until $v(t)$ reaches the treshold which makes the comparator switch. The charge Q that was discharged by the photocurrent is:

$$Q = C\left(V_{dac} - V_{comp}\right) = \int_0^{t_{on}} i\left(t\right) dt = \eta_{det} \cdot \int_0^{t_{on}} L\left(t\right) dt = \eta_{det} \cdot E_{ph} \quad (3.1)$$

with η_{det} being the detector's efficiency and E_{ph} the emitted energy. This means the pixel will remain on until a certain amount of energy $E_{ph} \sim Q$ is emitted. A lower luminance $L(t)$ will simply result in a larger t_{on} until E_{ph} is emitted. At t_{on} the comparator switches the pixel off and no more light is emitted. The average emitted optical output during a frame is given by:

$$L_{av} = \frac{1}{T_{frame}} \int_0^{t_{on}} L\left(t\right) dt = \frac{C\left(V_{dac} - V_{comp}\right)}{\eta_{det}} \quad (3.2)$$

Equation (3.2) shows that the average output is independent from the pixel's output power and efficiency. However, as mentioned in Chapt. 1 the detector efficiency does show. Calibration of the driver-pixel entity might be needed. The charging voltage V_{dac} can be used to implement graysclaing. With $V_{dr} = V_{dac} - V_{comp} = V_{dr,\max} \cdot x$ and chosing C so that

$$L_{\max} - L_{\min} = \frac{C \cdot V_{dr,\max}}{\eta_{det}} \quad (3.3)$$

we find:

$$L_{PWM} = (L_{max} - L_{min}) \cdot x + L_{min} \tag{3.4}$$

Some considerations are in place though:

1. When discharging the capacitor we assumed no voltage dependency of the photocurrent. In reality however the equation for the capacitor voltage is given by:

$$C(v(t)) \frac{dv(t)}{dt} = -i(t, v(t)) \tag{3.5}$$

No photodetector is a perfect current source but the current is dependent on the voltage across the detector. In Chapt. 5 we will present measurements which show that the photocurrent remains linear with the incident light and can be written as

$$i_{ph}(v(t)) = i_0(t)(\alpha v(t) + 1) = \left(\eta^0_{det}(\alpha v(t) + 1)\right) L(t) \tag{3.6}$$

where $i_0(t)$ is the photocurrent for $v(t) = 0$. The efficiency η_{det} is now voltage- (and thus time-) dependent with η^0_{det} the efficiency for $v(t) = 0$. For the sake of completeness Eqn. (3.5) also shows the capacitance C dependent on $v(t)$ as is the case for some silicon integrated capacitors. However this dependency is neglectible compared to the voltage dependency of the photodetector. The voltage dependency of the photocurrent implies that E_{ph} will no longer be proportional to $V_{dr} = V_{dac} - V_{comp}$. For example if we assume an ideal pixel with

$$L(t) = L_0 \cdot H\left(v(t) - V_{comp}\right) = \begin{cases} L_0 & \text{for } t \leq t_{on} \\ 0 & \text{for } t_{on} < t \leq T_{frame} \end{cases} \tag{3.7}$$

with $H(t)$ the heavyside function and the detector efficiency given by Eqn. 3.6 then it is easily shown that

$$L_{av} = \frac{C}{\eta^0_{det} \cdot \alpha \cdot T_{frame}} \ln\left(\frac{\alpha V_{dac} + 1}{\alpha V_{comp} + 1}\right) \overset{\lim_{\alpha \to 0}}{\Rightarrow} \frac{C}{\eta^0_{det} T_{frame}} \left(V_{dac} - V_{comp}\right)$$

(3.8)

It is clear that voltage dependency gives "infralinear" behaviour towards the driving signal, which would need an even larger NOB precision (see Chapt. 1) to implement perceptual grayscaling than a linear driver. Small voltage dependency is therefore preferable. It should be noted that this voltage dependency does only influence the linearity towards grayscaling. As $i(t, v(t)$ is still perfectly proportional to $L(t)$ the optical feedback is not "distorted". Indeed Eqn. (3.8) is still independent of $L(t)$. Measurements on photodiodes are presented in Chapt. 5 and present $\alpha \approx 2\%$ which gives only little variation from a linear characteristic. For simplicity reasons we will therefore use the linearisation in following.

2. The optical feedback signal is only dependent on the emitted light of the pixel and not on the ambient light which also causes L_{min}. Wether this is valid depends on the display architecture and display assembling. For the SPSD[1] display architecture the driver might be shielded for ambient light and this is a defendable assumption. For the MPSD display architecture however this is not. A ambient light cancellation will be necessary after which the here presented considerations remain valid.

3. In the description of the circuit we assumed a perfect comparator and perfect pixel. The comparator switches instantaniously and from that time the pixel was assumed not to emit light anymore. In Sect. 2.4 we pointed out that every pixel has a fall time during which it still emits light. Therefore, the total amount of emitted optical power is given by:

$$E_{ph,tot} = E_{ph,Q} + E_{ph,fall} \tag{3.9}$$

Yet $E_{ph,fall}$ is not measured by the circuit of Fig. 3.1 and therefore $E_{ph,tot}$ will not be perfectly proportional to Q. An error is introduced and maximum fall times can be calculated. However, before we do this another, more important problem needs

[1] Single Pixel Single Driver

to be adressed: how can we implement calibration ability to the circuit and what are the consequences.

3.1.2 Calibration

In Chapt. 1 we mentioned that in order for optical feedback to give a comparable measurement, the feedback circuit should be calibrated. Where for an active matrix dislay with optical feedback this might not be necessary, for a modular display approach, the light coupling of the different pixels towards the driver IC can be totally different and requires some calibration.

Because of these variations between the different measurement systems (optical feedback loops) two pixels with equal output characteristics will be emitting with different average power over a frame. We can therefore say that the average output power of a pixel during one frame is given by:

$$L_{out} = (L_{\max} - L_{\min}) \cdot \frac{x}{\beta^*} + L_{\min} \tag{3.10}$$

The parameter $\beta \in [1, \beta_{\max}]$ represents the deviations between the different measurement systems. Calibration means that we should somehow compensate for this β^*.

Single Parameter Loop

Calibration can be done via quantity x that is also used for grayscaling. This means that $x \in [0, \beta_{\max}]$. For the circuit in Fig. 3.1 V_{dac} was used for grayscaling and its range should be extended by a factor $\beta_{\max}$. Thus we can write:

$$L_{out} = (L_{\max} - L_{\min}) \cdot \frac{\beta_{\max}}{\beta^*} \frac{k}{2^r - 1} + L_{\min} \tag{3.11}$$

In order to represent meaningfull grayscaling and preserve display uniformity, we derived the necessary NOB in Chapt. 1. The range of x is increased with a factor $\beta_{\max}$ compared to Eqn. (1.17), but the

same conditions remain valid. The difference between k and $k+1$ is:

$$\Delta L = (L_{\max} - L_{\min}) \cdot \left(\frac{\beta_{\max}}{\beta^* \cdot (2^r - 1)} \right) \tag{3.12}$$

which is the largest for $\beta^* = 1$. In Chapt. 1 we found the NOB m for a linear driver without considering calibration. Therefore we can roughly say:

$$\frac{\beta_{\max}}{2^r - 1} \leq \frac{1}{2^m - 1} \Rightarrow r \geq \log_2 (\beta_{\max} (2^m - 1) + 1) \approx \log_2 (\beta_{\max}) + m \tag{3.13}$$

This is not exactly correct as n was already rounded up, but it gives a good measure. In Sect. 1.5 we mentioned that the magnitude of $\beta_{\max}$ is determined by:

- the driver IC parameters: resistor and capacitance values,... are only 20% precise.
- the spectral responsivity of the photodetector: a display has red, green and blue pixels which all generate a different feedback signal magnitude. As the driver IC would be the same for all these pixels, it must be able to cope with this difference in responsivity. Table 3.2.4 shows this factor theoretically goes up to ≈ 1.5.
- the coupling of light into the detector. This ratio will be calculated further in this chapter but is obviously very dependend on the module construction. A larger module size can increase this factor very fast. Typically a factor 4 to 20 can occur!

A combination of the causes listed above suggests a value of $\beta_{max} = 20$ is possible. This would mean a $r \approx 5 + m$ bit precision for the driver. If we look at Table 1.2 this would mean at least 17 bit precision for a 100 cd/m^2 display and even 20 bit for a 1000 cd/m^2 display in order to preserve display uniformity. These values much too high for a practical implementation. Moreover it would mean that each pixel would have different k-values (see Eqn. (3.11)) for its graylevels, which would require a pixel specific data transformation e.g. via a (very large) lookup table.

Separate Gain

It would be a more logical choice to introduce a gain B to the feedback circuit which is used to calibrate the measurement system independently from the grayscaling variable x. Eqn. (3.10) becomes:

$$L_{out} = (L_{\max} - L_{\min}) \frac{x \cdot \hat{B}}{\beta^*} + L_{\min} \tag{3.14}$$

To take variations of β^* into account, it can be said:

$$\forall \beta^* \in [1, \beta_{\max}], \exists\, B^* \in [B_{\min}, B_{\max}] : \frac{B^*}{\beta^*} = 1 \tag{3.15}$$

In the above equation, $B^* = \beta^*$ is the ideal value of the gain B. However, we already mentioned in Sect. 1.5 that this gain calibration should be stored and therefore must be digitalized. This means we will adjust to a certain digital value $\hat{B}$ which is only an approximation of the desired analog value B^*. Consider this digital to analog conversion given by:

$$\hat{B} = B_{\min} + \Delta B \cdot \sum_{i=0}^{s-1} b_i 2^i \qquad \text{with } \Delta B = \frac{\beta_{\max}}{2^s - 1} \tag{3.16}$$

then the ideal value B^* will be approximated within 1 LSB/2: $B^* \in \left[\hat{B} - \frac{\Delta B}{2}, \hat{B} + \frac{\Delta B}{2}\right]$. As x is r bit adjustable to a value $x(k)$ in order to implement the correct PWM duty cycle for a certain perceptual graylevel as discussed in Chapt. 1. Thus we can write:

$$L_{PWM}(k) = (L_{\max} - L_{\min}) \frac{\left(x(k) \pm \frac{\Delta x}{2}\right)\left(B^* \pm \frac{\Delta B}{2}\right)}{\beta^*} + L_{\min}$$

This means an error ΔL can occur on the desired output $L_{PWM}(k)$:

$$\Delta L = (L_{\max} - L_{\min}) \frac{\Delta x}{2} + (L_{PWM}(k) - L_{\min}) \frac{\Delta B}{2B^*} \ldots$$

$$\ldots + (L_{\max} - L_{\min}) \frac{\Delta x \cdot \Delta B}{4B^*} \tag{3.17}$$

Once more the conditions towards grayscaling and uniformity must be met:

- The graylevels must be monotonic:

$$L_{PWM}(k,j) - \Delta L > L_{HVS}(j - 1/2) \tag{3.18}$$

$$L_{PWM}(k,j) + \Delta L < L_{HVS}(j + 1/2) \tag{3.19}$$

- The graylevels must be noticeably different:

$$L_{PWM}(k,j-1) - \Delta L > (L_{PWM}(k,j) + \Delta L) + 1\ JND \tag{3.20}$$

$$L_{PWM}(k,j-1) + \Delta L < (L_{PWM}(k,j) - \Delta L) - 1\ JND \tag{3.21}$$

- The display must be perceptually uniform:

$$L_{PWM}(k,j) - \Delta L > L_{PWM}(k,j) - 1\ JND \tag{3.22}$$

$$L_{PWM}(k,j) + \Delta L < L_{PWM}(k,j) + 1\ JND \tag{3.23}$$

Table 3.1 gives an overview of the required NOB for B. We evaluated for $\beta_{\max}$ equal to 50, 20 and 2. As is obvious, higher $\beta_{\max}$ requires a larger NOB. For a 1000 cd/m^2 display a 12 bit precision is needed for large $\beta_{\max}$ and with Eqn. (3.16) and Eqn. (3.17) it rises 1 bit when $\beta_{\max}$ doubles. As was mentioned different spectral responsivity for the different colours requires at least $\beta_{\max} = 2$ for a MPSD[2] display architecture. Table 3.1 shows that still an 8 bit adjustment is needed.

3.1.3 Conclusion

In this section we introduced a first circuit for PWM optical feedback. The proposed circuit provides an analog PWM driver as the voltage V_{dac} is used for grayscaling. Therefore a high precision DAC is needed. As the optical feedback for different pixels should be calibratable the NOB precision rises even further to unacceptable values. Therefore a seperate calibration parameter should be introduced in the loop. A first rough calculation showed that two DAC's are necessary but both with acceptable precision.

In Chapt. 2 we mentioned one of the major advantages of PWM is the possibility of an easy digital implementation (e.g. via a

[2] Multi Pixel Single Driver

Table 3.1: The required NOB for preceptually uniform grayscaling when applying optical feedback with calibration based on a seperate quantity *B*. Different values for $\beta_{\max}$ are considered: 50,20 and 2. The values listed assume that the grayscaling quantity *x* has the maximum of the precisions listed in Tables 1.1 and 1.2.

	100			500			1000		
	50	20	2	50	20	2	50	20	2
6	12	11	8	12	11	8	12	11	8
7	12	11	8	12	11	8	12	11	8
8	14	13	9	13	11	8	12	11	8

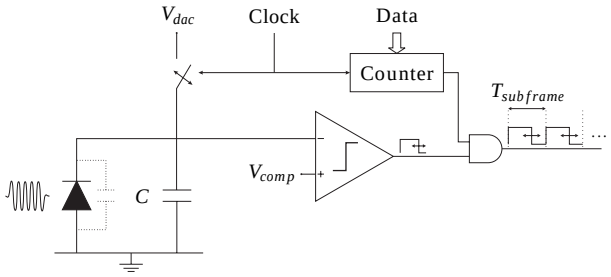
counter). The proposed circuit in Fig. 3.1 implements a fully analog PWM driver with optical feedback which needs a large DAC (up to 15 bit resolution). A 15 bit digital counter on the other hand would not only be much easier to design, but would also require significantly less silicon area.

The seperation of this calibration parameter from the grayscaling parameter is discussed in following paragraph and the digitalization of grayscaling is discussed in the following paragraph.

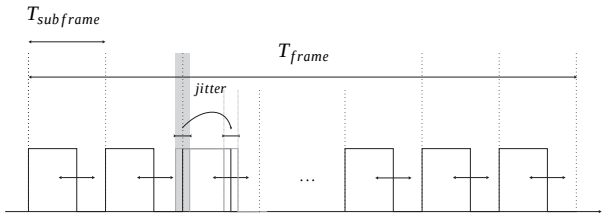
3.2 Adjusted feedback circuit

3.2.1 Circuit description

Figure 3.2(a) shows how PWM grayscaling can be done digitally. The circuit generates grayscaling with a digital r bit counter. Without optical feedback this should be enough to implement a digital PWM. The PWM *k*-value of the desired graylevel is loaded into the counter at the beginning of the frame and the counter (data) generates an appropriate PWM signal by counting the number of "subframes" the pixel should be on. Basically the frame is divided into smaller subframes (2^r-1 in total) while the optical feedback keeps the LSB ammount of emitted energy during one subframe



(a) Digital PWM with optical feedback



(b) Output of schematic shown in Fig. (a)

Figure 3.2: Digital PWM grayscaling with calibratable optical feedback.

constant. The optical feedback side is the same as in Fig. 3.1, but the charge and discarge cycle is now much faster. The capacitor is once more charged with a voltage V_{dac} which is no longer responsible for grayscaling, but fulfills the role of parameter B now. Therefore the grayscaling parameter (i.e. the counter) and the calibration parameter are effectively seperated from each other. The changes to the circuit have, beside the operational differences, also some other implications.

3.2.2 NOB of parameters

Up until now we always presumed an analog signal for grayscaling. E.g. in Fig. 3.1 the grayscaling is generated by an analog DAC and a noise of 1/2 LSB ($\Delta x/2$) has to be taken into account when calculating the required NOB for monotonic, meaningfull and uniform perceptual grayscaling. When providing digital PWM with optical feedback as in Fig. 3.2(a) no noise-error is made as we count

discretely. The equivalent analog noise is found in the clock jitter but this has no influence on the driver's performance. Figure 3.2(b) shows the output of the circuit. As clock jitter can occur, it will alter the moment where the pixel is switched on. The optical feedback will regulate the on-time of the pixel so the occuring jitter will simply lead to a time shift of the on-pulse. This is however possible as the PWM optical feedback only uses a fraction of the subframe to drive the pixel. Only when the on-time becomes as large as the whole subframe (at the end of the display's lifetime) will clock jitter influence the average emitted energy during the subframe. We can say clock jitter will (very) slightly reduce the lifetime of the display but does generally not influence the performance of the circuit. This means the digital grayscaling will not introduce non uniformity and the required NOB for the counter are listed in Table 3.2 and slightly lower than the ones in Table 1.1. This results in a smaller counter, but more importantly in less and longer subframes. The NOB for B does not change when taking this change into account, so Table 3.1 remains valid.

Table 3.2: The required NOB for the digital counter. As digital PWM is inherently uniform and discrete, these values are generally 1 bit lower than the previously mentioned values.

	100	500	1000
6	9	11	12
7	11	12	13
8	13	13	14

3.2.3 Pixel transient response

In Sect. 3.1.1 it was already mentioned that the optical feedback circuit does not take the emitted optical energy after the switching of the comparator into account. However, this problem was subordinate to the calibration problem. With the new circuit proposed, let us try to quantify this extra optical energy and look at the conse-

quences.

The circuit shown in Fig. 3.2 will provide optical feedback during a subframe by charging the capacitor with a certain charge $Q = C \cdot \left(V_{dac} - V_{comp}\right)$. Due to the optical feedback signal, the capacitor is discharged and the pixel is driven until this charge Q is depleted. Q is therefore proportional to an emitted energy $E_{ph,sf}$ during a subframe:

$$E_{ph,sf} = \int_0^{t_{on}} L\left(t\right) dt \sim \int_0^{t_{on}} I\left(t\right) dt = Q \tag{3.24}$$

This means the on-time of the pixel is altered so the area in gray in Fig. 3.3 will remain constant. Note that due to the transient response when switching the pixel on $t_{on}^{new} \neq t_{on}^{old} \cdot a$. However, when switching the pixel off, there is a transient response during which the pixel still emits light: E_{fall}, which is hatched in Fig. 3.3. The optical feedback will not take this contribution into consideration and this might be considered an "error contribution".

Yet the proposed driver will also require calibration to define the best charge Q (or V_{dac}) suited for the driver-pixel entity. This means we will measure the pixel's output with an external detector and change Q until the externally measured energy equals a desired energy $E_{d,sf}$. Therefore, this "error contribution" E_{fall} will be compensated for by the initial calibration. As Fig. 3.3 shows this is not an "all-solving" solution: when the pixel ages, E_{fall} decreases and an error on the output energy is still made. Let us determine the maximum fall time t_f so this error is small enough to preserve monotonic, distinguishable and uniform grayscaling.

Subframe Driving

Fig. 3.2(b) shows the used driving waveform: each subframe the duty pixel is switched on for a certain time defined by the optical feedback and switched off again. Calibration of the driver-pixel entity means

$$E_{d,sf} = E_{ph,sf} + E_{fall} \tag{3.25}$$

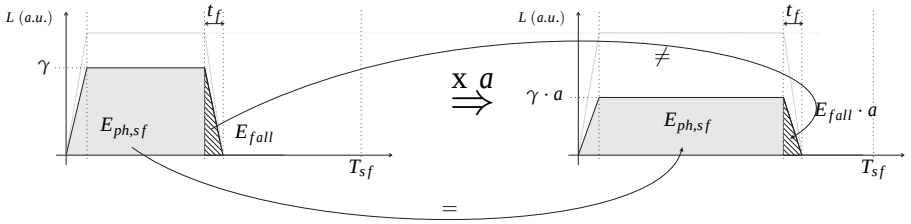


Figure 3.3: The influence of pixel response time. The pixel is driven with a driving signal shown as the dotted line. This driving signal preserves the same magnitude but is streched in time. The emitted optical power is shown initially (left) and after some ageing occured (right) by the solid line.

with, according to Fig. 3.3:

$$E_{fall} = \frac{t_f}{2} \left(L_{\max} - L_{\min}\right) \cdot \gamma \tag{3.26}$$

γ is the same parameter that was introduced in Sect. 2.7: as PWM feedback should increase it's duty cycle, it should begin by overdriving the pixel with a factor γ and start with a duty cycle of $1/\gamma$.

As the pixel ages with a factor a, the optical output power diminishes but the optical feedback will alter the on-time t_{on} of the pixel so that $E_{ph,sf}$ is emitted while the capacitor is discharged. However, the contribution E_{fall} is not compensated. As the magnitude of the electrical driver signal remains equal, it is acceptable to assume that the transient responses remain the same and t_f remains constant. The conversion to optical energy however deteriorates with a and for a general graylevel it can be said:

$$E_{PWM}(k) = k \cdot E_{ph,sf} + k \cdot E_{fall} \cdot a \neq k \cdot E_{d,sf} \tag{3.27}$$

An error in average output power occurs and during an entire frame it is given by:

$$\Delta L = k \cdot \frac{t_f}{2T_{frame}} \left(L_{\max} - L_{\min}\right) \cdot \gamma \left(1 - a\right) \tag{3.28}$$

which reaches a maximum for $a = 1/\gamma$. As this error is made every subframe, the total error is proportional to k and yields very low ac-

ceptable fall times in order to achieve a monotonic, distinguishable and uniform grayscaling.

Note that the error due to the limited resolution of the calibration parameter B (i.c. $\left(V_{dac} - V_{comp}\right)$), which was described in Sect. 3.1.2, is still present. This represents an error on the charge Q which leads to an erroneous $E_{ph,sf}$. However this erroneous contribution is object to the optical feedback and will therefore not change due to ageing. Obviously when calculating a correct condition for t_f one should take this error into account. Yet Table 3.3 shows the "best case scenario" when this error isn't even taken into account. It is clear that fall times of a few nanoseconds are out of reach for any emissive display technology! Note that for an exponential decaying model (see Fig. 2.4 on p. 30) $\tau = t_f / 2$.

Table 3.3: The maximum fall time t_f for a subframe driven optical feedback. Only the fall time error was taken into account. Real values are even lower.

	100	500	1000
6	245 ns	55 ns	27 ns
7	61 ns	27 ns	13 ns
8	15 ns	14 ns	7 ns

In Fig. 1.2(b) (p. 20) we showed that the relative magnitude of 1 JND is very small for high luminance values and is asymptotic to 0.65%. As the uniformity constraint is typically the most stringent one (compare Table 1.1 with Table 1.2) we can write down an easy rule for the fall time error considering the worst case scenario (full brightness):

$$t_f < \frac{2 \cdot 0.0065 \cdot T_{frame}}{(\gamma - 1)\,(2^r - 1)} \tag{3.29}$$

Note that once more the calibration error ΔB should also be taken into account and the constraint is even more stringent.

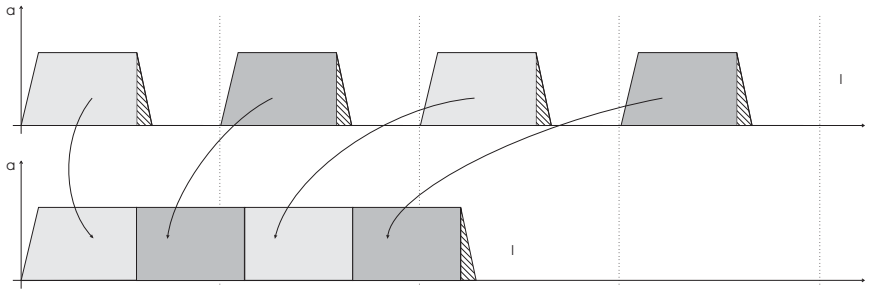


Figure 3.4: Concatenation of the subframes to a single on-time.

Concatenated Driving

When using "subframe driving" as mentioned in previous section, we switch the pixel on and off every subframe. The error made is therefore multiplied by the number of subframes the pixel is driven. This makes the error rise to fast for larger graylevels. Therefore it would be a better idea to:

- "concatenate" the subframes into one pulse so the relative weight of E_{fall} reduces for higher graylevels. This introduces an error during calibration.
- calibrate for a full brightness driving signal. Then the error will be smallest for full brightness and grow for smaller brightness graylevels.

Thus during calibration

$$E_{d,full} = (2^r - 1) \cdot E_{d,sf} = (2^r - 1) \cdot E_{ph,sf} + E_{fall} \tag{3.30}$$

The desired energy for a certain graylevel is then given by:

$$E_{d,gray} = k \cdot E_{d,sf} = k \cdot E_{ph,sf} + k \cdot \frac{E_{fall}}{2^r - 1} \tag{3.31}$$

Yet in reality we will emit a different energy during a frame:

$$E_{PWM}(k) = k \cdot E_{ph,sf} + E_{fall} \cdot a \tag{3.32}$$

With E_{fall} again given by Eqn. 3.26. Note that indeed even without ageing concatenation introduces an error. The overall error on the average output power during T_{frame} is given by:

$$\Delta L = \left| \frac{t_f}{2T_{frame}} (L_{\max} - L_{\min}) \gamma \left(a - \frac{k}{2^r - 1} \right) \right| \tag{3.33}$$

Table 3.4 shows the required values for t_f to recieve monotonic, distinguishable and uniform grayscaling with $a \in [1/\gamma, 1]$. The ∞ column shows the maximum fall time t_f allowed if the PWM was perfect (NOB for x is ∞) and no calibration error is present. These are the "best case" values. In the $\beta = 1$ column, a real PWM with NOB from Table 3.2 is used, still without calibration (therefore $\beta = 1$). The last column incorporates all types of errors. Logically we found these values very dependent on the NOB for x and B and by increasing these NOB by only 1 bit it is possible to come very close to the "best case" values. This is shown in the last row. Still, these fall times are very small, yet feasable for e.g. LED displays.

For slower displays technologies this adds to the conclusions of Chapt. 2: PWM feedback seems irreconcilable with high end applications and at best narrowly possible for low and applications.

Table 3.4: Acceptable fall times t_f in nanoseconds for concatenated driving. Still these values are very low, but feasible for for example LED displays.

	100			500			1000		
	∞	$\beta=1$	$\beta\neq1$	∞	$\beta=1$	$\beta\neq1$	∞	$\beta=1$	$\beta\neq1$
6	2700	2700	2600	540	540	530	260	260	260
7	2700	2400	2300	540	540	530	260	260	240
8	1600	900	900	540	290	150	260	210	130
NOB+1		1300	1300		540	540		260	260

Note that concatenated driving requires a few changes to the circuit. The counter should no longer count synchronously with the subframe clock T_{sf} but with the switching of the comparator and the

pixel should only be driven by the counter signal. This way the pixel is only switched off once at the end. A comparator with hysteresis is necessary to make sure the counter will not skip any subframes. On the other hand the capacitor should be charged after every discharge cycle. We will discuss this in following sections.

Photodetector transient response

In the previous paragraphs we only discussed the pixel's transient response and assumed a perfect photodetector with infinit bandwidth. In any case the bandwidth of the photodector should also be sufficient. For an integrated silicon photodetector a photodiode is a very fast detector with nanosecond rise and fall times. However, photodiodes have quite low responsivity (ampere per watt incident light) and we will show in next section that this is a severe problem for a MPSD architecture. For example a phototransistor has a much higher responsivity but suffers from very low bandwidth and is not useable in this circuit.

3.2.4 Charge considerations for MPSD architecture

We adressed the calibration problem from the first circuit by introducing digital PWM and subframe based optical feedback as it allowed the grayscaling and calibration to be seperated. This comes at the cost of increased bandwidth for the optical feedback loop as the charge on the capacitor should be evacuated within a subframe instead of a whole frame. This means the capacitor should be chosen much smaller, yet Fig. 3.2 shows $C \geq C_{det}$ as the photodetector is parallel with the charging capacitor. The other alternative is to reduce the charging voltage V_{charge}. However, we showed that this voltage should be adjustable with at least 8 bit resolution between its minimum and maximum value to allow driver calibration. This combination might be a problem. In order to assess this problem, a better knowledge of the magnitude of the photocurrent and detector capacity is necessary.

Incident Light

To focus our calculations we will assume a LED display from this point on as all our measurements were done with LED's as well. Furthermore to simplify the calculations the display pixels are assumed to be lambertian emitters with luminance L independent from the viewing angle: $L(\theta,\phi) = L$. Typical display application use LED's with a larger upwards luminance, yet for our story a lambertian assumption will yield in best case values.

Figure 3.5 shows a possible display tile layout for a MPSD architecture. The pixels are 3 color LED's, pitched at a distance p from each other and the detector is positioned at the side of the tile so light from all pixels can reach it. Placing the detector-driver in the middle of the tile would be better but seems difficult from a assembly point of view. The relation between the luminance L of a lambertian lightsource and the total luminous flux $dF^{lum}_{LED,3cl}$ that is emitted (only upwards) by a part dS_{LED} of light source (i.e. a LED) is given by:

$$dF^{lum}_{LED,3cl} = \pi L \cdot dS_{LED,3cl} \tag{3.34}$$

The illuminance of the detector is given:

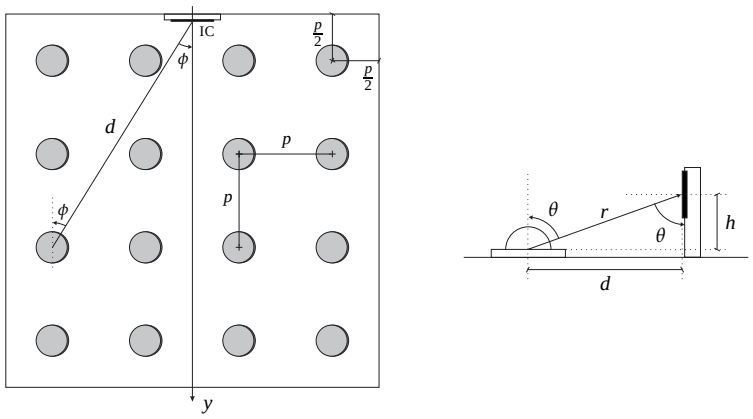
$$E = \int_{S_{LED,3cl}} \frac{dF^{lum}_{det}}{dS_{det}} = \int_{S_{LED,3cl}} \frac{L dS_{LED,3cl}\cos(\theta)}{dS_{det}} \frac{dS_{det}\sin(\theta)\cos(\phi)}{r^2} \tag{3.35}$$

When approximating the 3 color LED as a point source θ, ϕ and r do not change when integrating over the entire LED surface and both equations above yield to:

$$E(\theta) \approx \frac{F^{lum}_{LED,3cl}}{\pi} \frac{\cos(\theta)\sin(\theta)\cos(\phi)}{r^2} \tag{3.36}$$

with $F^{lum}_{LED,3cl}$ the total output power (luminous flux) of the 3 color LED as a photometric quantity. For a display with total luminance L and a 3 color pixel with pixel pitch p, according to Eqn. (3.34) each 3 color pixel emits a luminous flux

$$F^{lum}_{LED,3cl} = \pi \cdot L \cdot p^2 \tag{3.37}$$



(a) Topview 4x4 tile (b) Sideview

Figure 3.5: Example of a 4x4 tile where the driver IC with integrated detector is placed on the side of the tile.

θ, ϕ and r are shown in Fig. 3.5. As the detector is also very small we can approximate the total luminous flux that reaches the detector as:

$$F_{det}^{lum} \approx S_{det} \frac{F_{LED,3cl}^{lum}}{\pi} \frac{\cos(\theta)\sin(\theta)\cos(\phi)}{r^2} \tag{3.38}$$

Equation (3.38) was derived for photometric quantities but is also valid for radiometric flux. As the photocurrent is proportional to the radiometric flux of a single color of the 3 color LED, we need to know the corresponding radiant flux per color per LED. For most commercial displays the 3 color LED's are calibrated to the D65 white point. This means the power of the red, green and blue LED's are adjusted so the D65 white point is reached. Figure 3.6 shows the sprectra of the LED's we used for measurements in this research. The power ratio's $\alpha_i^{'}$ for the D65 white point are listed in the inset table. It should be noted that these proportions are quite dependent on the exact LED spectra.

With $S_i(\lambda)$ the normalised spectra of the different color LED's (R,G and B), the total radiometric power spectrum of a 3 color LED

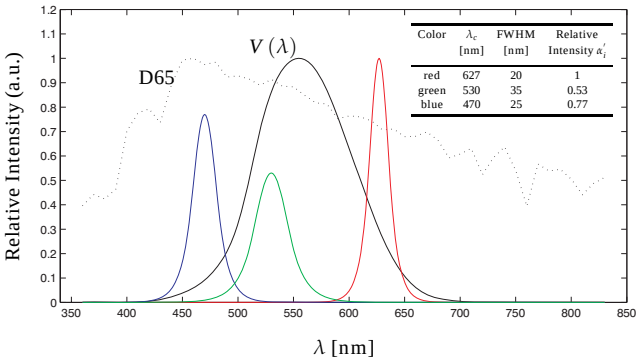


Figure 3.6: LED spectra and specifications. The relative intensities are for the D65 white point

can be normalised (to 1 Watt) and is given by:

$$F_{LED,3cl}^{rad} = \int_{\lambda} \left(\alpha_R S_R(\lambda) + \alpha_G S_G(\lambda) + \alpha_B S_B(\lambda)\right) d\lambda \tag{3.39}$$

with

$$\alpha_i = \frac{\alpha_i'}{\int_{\lambda} \left(\alpha_R' S_R(\lambda) + \alpha_G' S_G(\lambda) + \alpha_B' S_B(\lambda)\right) d\lambda} \tag{3.40}$$

With Eqn. (1.1) giving the relation between photometric and radiometric quantities, the radiant flux $F_{LED,i}^{rad}$ for each color is then given by:

$$\begin{aligned} F_{LED,i}^{rad} &= \frac{F_{LED,3cl}^{lum} \cdot \alpha_i \int_{\lambda} S_i(\lambda)\, d\lambda}{683 \cdot \int_{\lambda} \left(\alpha_R S_R(\lambda) + \alpha_G S_G(\lambda) + \alpha_B S_B(\lambda)\right) V(\lambda)\, d\lambda} \\ &= \frac{F_{LED,3cl}^{lum}}{K} \cdot \alpha_i \int_{\lambda} S_i(\lambda)\, d\lambda \end{aligned} \tag{3.41}$$

K represents the number of lumen luminous flux that is emitted by the 3 color LED with a radiant flux of 1 Watt. We found with the spectra of the used LED's 270 lumen for 1 Watt[3]. With Eqn. (3.38)

[3] D65 white represents 185 lumen for 1 Watt radiometric power

and Fig. 3.5 the total optical power reaching the detector is:

$$F_{det,i}^{rad} = S_{det} \cdot \frac{F_{LED,i}^{rad}}{\pi} \frac{h \cdot d \cdot y}{d\left(h^2 + d^2\right)^2} \tag{3.42}$$

Photocurrent

Table 3.5: Photodetector efficiency for the different LED's. Also the relative proportions are given.

Red	Green	Blue
0.43 A / W	0.35 A / W	0.29 A / W
1	0.81	0.67

To calculate the photocurrent, the photodetector responsivity should also be taken into account. It is clear that this will also be wavelength dependent. Table shows the theoretical photodiode responsivity η to the red, green and blue LED's (see Chapt. 5 for calculation). We can approximate the photocurrent for each color with these values:

$$\begin{aligned} I_{ph,i} &= \frac{S_{det}}{\pi} \frac{y \cdot h \cdot d}{d\left(h^2 + d^2\right)^2} \cdot \frac{F_{LED,3cl}^{lum}}{K} \cdot \alpha_i \int_{\lambda} \eta_{det}(\lambda)\, S_i(\lambda)\, d\lambda \\ &\approx \frac{S_{det}}{\pi} \frac{y \cdot h \cdot d}{d\left(h^2 + d^2\right)^2} \frac{F_{LED,3cl}^{lum}}{K} \cdot \alpha_i \cdot \eta \int_{\lambda} S_i(\lambda)\, d\lambda \end{aligned} \tag{3.43}$$

In Eqn. (3.43) distance d and y are fixed, but the height h of the detector is very important. Figure 3.7 shows the expected photocurrent as a function of the height of the photodetector for the blue LED's on a 4x4 tile with a display luminance of 2000 cd/m^2 and detector size of $1mm^2$. All different pixels of the tile are shown. The influence of the height of the detector is clearly seen. Note that depending on the height of the detector the ratio $I_{\max} / I_{\min}$ varies enourmously as for each pixel another optimal h exists.

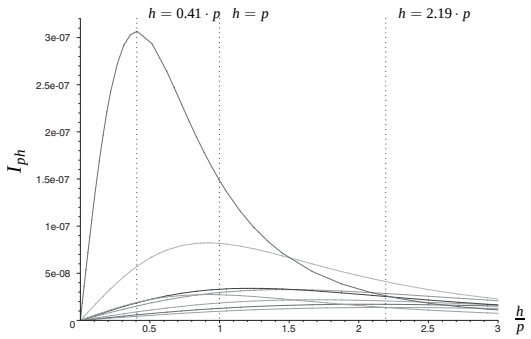


Figure 3.7: Expected photocurrent from the different pixels of a 4x4 tile as a function of the height of the detector. A blue LED was assumed and a detector area of 1mm^2

In Table 3.6 three heights are examined, also shown with the dotted lines in Fig. 3.7: maximum $I_{\max}$, maximum $I_{\min}$ and $h = p$. Note that these heights are defined proportional to the pitch p and therefore the photocurrent becomes independent of the pitch. Therefore Table 3.6 gives the expected quantities for different luminances only. The found photocurrents are for a 1mm^2 detector. The maximum and minimum power are calculated with a red and green LED respectivily but the maximum and minimum photocurrent with a red LED and blue LED respectivily.

The expected minimal photocurrent is very small and even in the best case only a few nA. The maximum current can be much higher depending on a good positioning of the detector. However, as discussed in Sect. 3.1.2, a very large ratio $\beta_{\min} = I_{\max} / I_{\min}$ requires a higher NOB precision for the charging voltage.

Charging voltage

As mentioned we are interested in a large photocurrent but combined with a small detector capacitance to allow a larger charging voltage as the detector capacitance is parallel to the charging capacitance. The total charge should be discharged in a time t_{sf} / γ by a photocurrent γI_{ph} and the required charging voltage will be largest

Table 3.6: Expected quantities for a MPSD 4x4 tile.

	500 cd/m^2			1000 cd/m^2			2000 cd/m^2		
h	0.41 p	p	2.19 p	0.41 p	p	2.19 p	0.41 p	p	2.19 p
$E^{rad}_{Red,\max}$ [W/m^2]	0.295	0.143	0.040	0.59	0.285	0.079	1.180	0.571	0.158
$E^{rad}_{Blue,\min}$ [W/m^2]	0.004	0.009	0.012	0.008	0.017	0.025	0.016	0.035	0.049
$I_{\max}$ [nA/mm^2]	112	30	15.1	224	59.8	30.1	448	119	60.2
$I_{\min}$ [nA/mm^2]	1.11	2.43	3.45	2.22	4.86	6.87	4.43	9.72	13.7
$\beta_{\min} = \frac{I_{\max}}{I_{\min}}$	101	12.3	4.39	101	12.3	4.39	101	12.3	4.39
NOB$_\beta$	14	11	10	14	11	10	14	11	10
NOB$_L$	11	11	11	12	12	12	12	12	12
$V_{\max}$ [mV]	9.6	2.560	1.291	9.6	2.560	1.291	19.2	5.119	2.582
$V_{\min}$ [mV]	0.095	0.208	0.294	0.095	0.208	0.294	0.19	0.416	0.589
Δv [μV]	0.580	1.148	0.973	0.580	1.148	0.973	1.161	2.230	1.947

for $C_{tot} = C_{det}$:

$$V_{charge} = \frac{\frac{t_{sf}}{\gamma} \cdot \gamma I_{ph}}{C_{tot}} \leq t_{sf} \cdot \frac{I_{ph}}{C_{det}} \tag{3.44}$$

The photocurrent is obviously proportional to the area of the detector yet so is the detector capacitance. Therefore chosing a larger detector will not increase the charging voltage. A good estimate is given by the parasitic capacitance of an NWELL in the I2T100 technology as the detector capacitance: $C_{det} = S_{det} \cdot 95\mathrm{e}^{-6}\ pF/\mu m^2$. In Table 3.6 the expected charging voltages for both maximum and minimum current are listed for the different heights examined. As stated in previous sections this charging voltage should also be adjustable to calibrate the driver-pixel entity and the NOB is dependent on the ratio $\beta_{min} = V_{charge}^{\max} / V_{charge}^{\min} = I_{\max} / I_{\min}$ as presented in Sect. 3.1.2.

One look at Tabel 3.6 makes it clear that these voltages are much too low from a designer's point of view. Only a few mV range for a 10+ DAC is impossible. Therefore we can conclude that for a MPSD architecture the high bandwidth combined with the small photocurrents seems impossible. Note that in the beginning of this section we assumed lambertian emittors. It is clear that non-lambertian emittors which emit more upwards will generate even smaller photocurrents. Thus these considerations can be seen as best case.

For a SPSD architecture the driver IC can be mounted very close to the pixel and much higher photocurrents are to be expected, though quantification is much more dependent on the actual assembly and the pixel characteristics than in the MPSD discussed and therefore not done. Yet it seems possible to obtain large enough photocurrents for a subframe calibration. However, capacitor charging is another problem as will be discussed in the next section.

3.2.5 Capacitor charging

As mentioned pure subframe driving where the pixel is switched on and off each subframe is not possible for uniformity reasons. Therefore concatenated driving with subframe based optical feed-

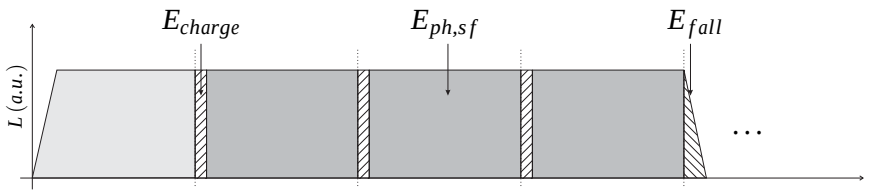


Figure 3.8: Charging error for concatenated driving

back was proposed. This means the capacitor, whether it is a dedicated and / or the photodetector's, should be charged with a charge Q every subframe and during that time the optical feedback will not work properly. Figure 3.8 shows the driving waveform. Each subframe there is a contribution E_{charge} during a time t_{charge} during which the capacitor is charged for the next subframe. Similarly to the E_{fall} contribution, E_{charge} is not subject to the optical feedback and for an ageing factor a it can be written:

$$E_{PWM}(k) = k \cdot E_{ph,sf} + (k-1) \cdot E_{charge} \cdot a + E_{fall} \cdot a \tag{3.45}$$

where we assumed a precharged capacitor at the beginning of the frame. If the calibration is done on a full brightness signal, the desired output energy during a frame is given by:

$$E_{d,gray} = k \cdot E_{ph,sf} + (k-1) \cdot E_{charge} + k \cdot \frac{E_{fall}}{2^r - 1} \tag{3.46}$$

The error on the average output luminance L is given by:

$$\Delta L = \left| \left(\frac{t_f}{2} \left(\frac{k}{2^r - 1} - a \right) + k \cdot t_{charge} (1-a) \right) \frac{(L_{\max} - L_{\min})\,\gamma}{T_{frame}} \right| \tag{3.47}$$

The allowed charging time is dependent on L, β, NOB perceptual grayscaling, t_{fall}, ... However, the charging error is similar to the subframe driving error from Sect. 3.2.3 with $t_{load} = t_f / 2$ which was the reason for concatenated driving! Therefore for the sake of argument we will focus on (half of) the values of Table 3.3 which is actually an overestimate of the allowed charging time. This means

the charging capacitor should be charged within a few ns to a precise voltage! This would be very difficult in regard to transient response of the DAC.

3.2.6 Conclusion

The proposed circuit adaptation was necessary to separate the calibration and grayscaling parameters yet it introduced some unsurmountable obstacles due to the massive increase in bandwidth:

- for MPSD architecture the needed charging voltage is much to low to be workable. This is because of the small "photocurrent per capacitance" I_{ph}/C_{det}. A possibility would be to negate the detector capacitance's influence with an opamp based integrator. However, the very small expected currents combined with the detectors capacitive load and the high bandwidth requirements make for a more than challeging design.

- for both SPSD and MPSD architecture the driving waveform should be concatenated to a single pulse to adress the response characteristics of the pixel, even for the fastest display technologies such as LED.

The circuits discussed in previous sections raised some issues, but were as a matter of fact only applicable to a SPSD architecture. Indeed, the feedback was instantaneous and continuous. We discussed the MPSD architecture to determine whether the photocurrent was sufficient, yet passed over the fact that it is not possible to monitor all the different pixels continuously as their contributions would interfere. Only for a SPSD architecture one would be able through assemblation to seperate the different pixel contributions from each other. However, this does not mean the main conclusions of previous sections are without value. Parameter seperation, concatenated driving and bandwidth reduction remain necessary! Note that for an MPSD architecture also ambient light can reach the detector and should be taken into account.

3.3 Sampled optical feedback with ambient light correction

3.3.1 Circuit description: sampling

The main focus of this work is to extend display uniformity lifetime. The ageing of a display technology is a slow process that does not necessarily requires continuous feedback circuits such as the ones described in the sections above. To compensate for pixel ageing it would be sufficient to determine and adjust the adequate driving waveform periodically, e.g. every 24 hours. As the optical measurement is seperated from the actual driving, it can be performed with a much lower bandwidth. On the other hand, fast variations in light output, e.g. temperature based variations, will no longer be compensated for.

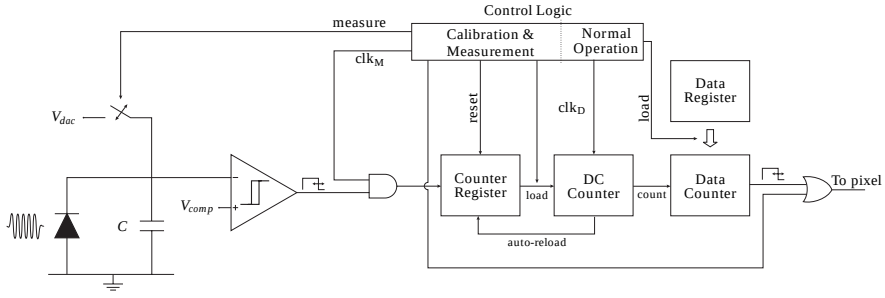


Figure 3.9: Sampled optical feedback circuit

Figure 3.9 presents the sampling optical feedback circuit. As can be seen, the optical feedback is still the same but the actual driving circuit is extended a bit.

Measurement When a measurement is performed, the control logic will charge the capacitor with V_{DAC} and activate the pixel. While the photocurrent discharges C, the comparator output is no longer used to drive the pixel, but in stead the duty cycle length of this discharge pulse is digitally measured with a clock clk_M and its value is stored in the DC counter / register.

Normal operation The stored duty cycle (DC) is loaded into the DC counter and the pulse width is scaled down to a single subframe by a clock clk_{DC}, much faster than clk_{M}. The data counter holds the required number of subframes (k-value) and each time the DC counter overflows it decrements the data counter and auto - reloads itself with the DC value from the register. This way the subframe contributions are concatenated as was discussed in Sect. 3.2.3.

Calibration The initial calibration can be performed as a combination of a measurement and normal operation. First a random V_{DAC} is used and the duty cycle is measured. This is used in normal operation to drive the pixel. While driving the pixel an external measurement can determine the emitted output power of the pixel and an adequate V_{DAC} can be calculated. This cycle (on chip measurement - normal operation - external measurement) can be repeated until the appropriate V_{DAC} is found.

In this implementation, the bandwidth of the measurement can be chosen rather freely as it is scaled down digitally, allowing much larger charging voltages. As the concatenation is also completely digital it does not require high charge currents. The price however is also twofold: firstly the feedback is no longer continuous and secondly an approximation error is made by digitalising the duty cycle. Therefore the measurement resolution should be sufficient. Scaling the duty cycle to a single subframe will therefore result in a very high clock frequency clk_{D}. To quantify the required measurement resolution, we will once more identify the different errors that occur. First however, we introduce ambient light correction to the circuit.

3.3.2 Circuit description: ambient light rejection

The different circuits presented up till now assumed incident light that only originated from the pixel that needed feedback. For a SPSD architecture this is defendable as the pixel / driver entity might be capsulated so only pixel light can reach the detector. For a MPSD

architecture however by defenition all pixels can contribute to the photocurrent. This requires measurements to be done seperatly and a sampled feedback was not only preferable but necessary. However, as ambient light can also contribute to the photocurrent, this contribution has to be substracted during the measurement. Figure 3.10 shows a possible implementation of an ambient light rejection (ALR) circuit.

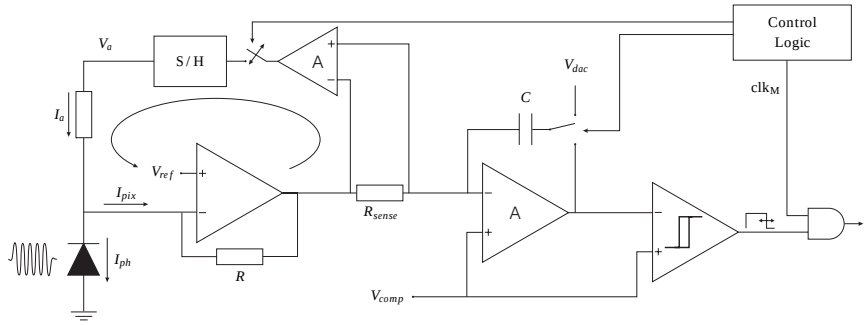


Figure 3.10: Ambient light rejection circuit for sampled optical feedback

Opamp A_{int} is an integrator where capacitor C is the charge / discharge capacitor. Before the integrator however a feedback loop (denoted with the circular arrow) is added to compensate for the ambient light contribution to the photocurrent. When a measurement is conducted with the pixel off, only ambient light will contribute to the photocurrent I_{ph}. The feedback loop regulates the current I_a via V_a so no current will flow through the sensing resistor R_{sense}.

A sample and hold (S / H) circuit will then capture the voltage V_a and the actual pixel measurement can be done. During the actual measurement, the S / H provides I_a and the actual current discharging the capacitor is $I_{ph} - I_a = I_{pix}$. With the actual measurement during only 1 frame (= 16.6 ms at 60 Hz), the ambient light contribution can be considered constant. Thus the duty cycle is only defined by the pixel contribution as is desired. Note that the digital "processing" of the duty cycle, shown in Fig. 3.9 remains the same, yet was not included as not to overload Fig. 3.10.

In Chapt. 6 we will describe the feedback circuit more pro-

foundly, yet here we wish to point out some considerations. The two circuits from Fig. 3.9 and Fig. 3.10 introduce two new errors: a sampling error due to the quantisation of the duty cycle and an ambient light error as no feedback loop is perfect. Therefore in the next paragraphs we will calculate required sampling resolution and required ambient light rejection.

3.3.3 Sampling resolution and ALR ratio

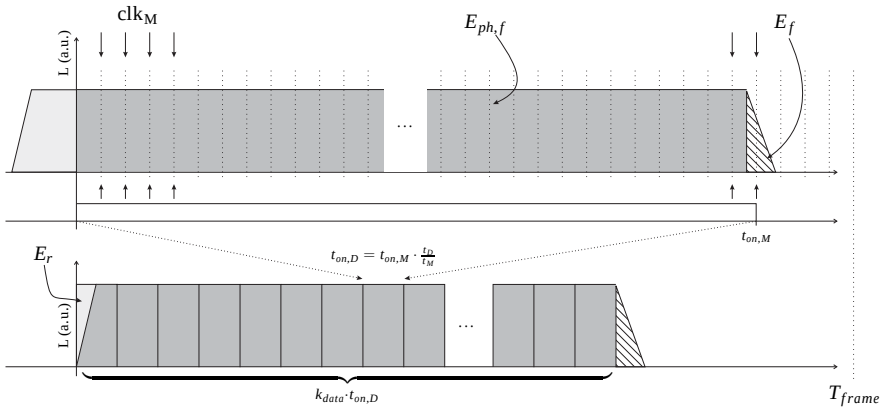


Figure 3.11: Measurement for sampled optical feedback with ALR. The on time is measured first and then "replayed" k times.

The upper graph of Fig. 3.11 shows the measurement which is done in an entire frame. Because the ALR circuit has some operational amplifiers, it is very hard to correctly detect the rise-time contribution of the pixel. This would require high bandwidth, low overshoot,... and would complicate the design enormously. Therefore, when a measurement is performed, the pixel should be activated in advance. When the discharging of the capacitor is started, the duty cycle is measured digitally (middle graph) and the measured duty cycle is then scaled and replayed k times as shown in the lower graph.

During initial calibration the required capacitor voltage is determined based on a full brightness signal $k = 2^r - 1$ (as mentioned in

Sect. 3.2.3) and the desired emitted energy is given by:

$$\begin{aligned} E_{d,full} &= (2^r-1)\,\frac{\frac{CV^*}{I^0_{pix}\gamma\beta^*}(L\cdot\gamma)}{2^r-1} + \left(E_f - E_r\right) \\ &= E^*_{ph} + \left(E_f - E_r\right) \end{aligned} \tag{3.48}$$

with V^* the optimal charging voltage, $L\cdot\gamma$ the (fixed) luminance of the PWM driven pixel, γ the overdrive factor and β^* the actual value of β for the considered pixel. $I^0_{pix}\cdot\gamma$ represents the minimum expected photocurrent contribution from a pixel with luminance $L\cdot\gamma$ at the time of initial calibration (when no ageing has occured yet).

In reality however, some errors are made and the pixel ages. A new measurement is necessary and the emitted output energy is given by:

$$E_{PWM}(k) = \frac{k}{2^r-1}\left(\frac{C\left(V^*\pm\frac{\Delta V}{2}\right)}{I^0_{pix}\gamma a\beta^*\pm\Delta i_a} + \frac{T_{fr}}{2^s}\right)(L\cdot\gamma\cdot a) + a\left(E_f - E_r\right) \tag{3.49}$$

In the above equation the error $T_{fr}/2^s$ is the maximum sampling error. Note that this error can only be an overestimate of the duty cycle. $\Delta V/2$ is the already mentioned uncertainty on V^* and Δi_a represents the remaining ambient light contribution due to finite ALR. Defining $\alpha = \Delta i_a/(I^0_{pix}\cdot\gamma)$ we can rewrite $E_{PWM}(k)$:

$$\begin{aligned} E_{PWM}(k) = \frac{k}{2^r-1}E_{d,full} + \left(a - \frac{k}{2^r-1}\right)\left(E_f - E_r\right) + \ldots \\ \ldots + \frac{k}{2^r-1}\left(L\gamma a\frac{T_{fr}}{2^s} \pm E^*_{ph}\frac{\Delta V}{2V^*} \pm E^*_{ph}\frac{\alpha}{a\beta^*} \pm E^*_{ph}\frac{\Delta V}{2V^*}\frac{\alpha}{a\beta^*}\right) \end{aligned} \tag{3.50}$$

Once more the occuring errors should be small enough to allow meaningfull, distinguishable and uniform perceptual grayscaling. As the errors are additive, it is clear that for example a higher sampling resolution will allow a smaller DAC resolution and lower

ambient light rejection. It should be noted that the fall and rise time error is the most important error for smaller graylevels, whereas the other types of errors are limiting for larger graylevels. Therefore increasing resolution or ALR ratio α (ALRR) will almost not influence the allowed $dt_{fr} = t_f - t_r$.

Table 3.7: The required sampling resolution and ALR ratio α for a $1000\,cd/m^2$ display with $NOB_{gr} = 8$ and $\beta = 20$.

NOB_V	NOB_S	α	dt
11	11	$0.4e^{-3}$	100ns
∞	9	$1.25e^{-3}$	175ns
∞	∞	$2.3e^{-3}$	250ns

Table 3.7 shows for a display with $1000cd/m^2$ luminance, $\beta = 10$ and 8 bit perceptual grayscaling. We find the necessary NOB_{PWM}=14 and NOB_V=11 and show the required NOB_S for sampling and required ALRR α as well as the allowed dt_{fr}. The required sampling resolution NOB_S is found to be 11 bit. However, when "replaying" the pulse width as a single subframe (see Fig. 3.11) we need a very fast clock clk_{DC} with a frequency given by:

$$f_{DC} = f_{frame} \cdot 2^{NOB_S} \cdot \left(2^{NOB_{PWM}} - 1\right) \tag{3.51}$$

For a display with 1000 cd/m^2 luminance and 8 bit perceptual grayscaling ($NOB_{PWM} = 14$) and we find $f_{DC} \approx 2$ GHz! Larger technologies, such as the 0.7 μm I^2T100 technology used in this work, have large devices with large gate capacitances and are simply not suited for such high frequencies. In Table 3.7 the minimum sampling resolution is also shown to be 9 bit, which implies a 500 MHz f_{DC} remains required for a $1000/8$[4] display!

The required ALRR α is also much too low: from Table 3.6 we learn that a minimum expected photocurrent $I_0 \cdot \gamma = 5\ nA$ is not unrealistic when using on chip photodiodes. With $\alpha = 0.4e^{-3}$ this

[4] 1000 cd/m^2 luminance and 8 bit perceptual grayscaling

would result in a maximum ambient light error current $\Delta i_a = 2\ pA$. This would be an extremely challeging design for the ALR circuit. Table 3.7 also mentiones the maximum ALRR to be $2.3e^{-3}$, yielding $\Delta i_a = 11.5\ pA$ which is still very low. Using better suited photodetectors such as phototransistors (see Chapt. 5), the minimum photocurrent can be higher, yielding more feasable Δi_a. Even then it is clear that increasing DAC resolution NOB_V would allow higher ALRR and lower maximum clockfrequency.

3.3.4 Photodetector choice

Until now little attention was given to the photodetector choise, yet previous paragraph showed the importance of an efficient photodector to allow higher ambient error currents. Previous circuits as well as circuits found in the literature that use PWM optical feedback [7, 15, 14, 13] all implement real-time optical feedback which require a high bandwidth photodetector. In a silicon technology photodiodes have the necessary bandwidth, but they yield very low photocurrents as already mentioned.

An alternative are phototransistors,also used in [7, 15, 13], which benifit from the current gain of a BJT. Specific active matrix technologies can optimise their process so the BJT bandwidth remains sufficient. However, as will be described in Chapt. 5 a silicon implementation of a phototransistor in I^2T100 has significant current gain, but this comes at the price of severly reduced bandwidth. This renders a phototransistor unfit for realtime optical feedback. For the proposed sampled optical feedback this is no longer a problem. As has been shown in Fig. 3.11 the pixel is activated in advance and only when the circuit (including the phototransistor) has reached steady state, a measurement is conducted. This means a much higher photocurrent can be expected and the ALR circuit design will be much easier.

3.3.5 Capacitor charging

Compared to the previous circuit of Fig. 3.2 the charging speed of the capacitor is no longer important. A measurement is only done

occasionally and the capacitor can be charged slowly, with a small current in advance. This means the required bandwidth for the DAC can be chosen much lower, also simplifying the design.

Also a too low charging voltage is no longer an issue. The measurement is done during a much larger time than a single subframe and the charging voltage will increase with the same factor. Depending on the expected photocurrents an appropriate charging capacitor and / or measurement time can be chosen. By chosing a appropriate measurement time one might minimalise the required charging capacitor to only the inherent detector capacitance and so reducing silicon area of the driver. Note that in the previous section we assumed a measurement time of an entire frame. Chosing another measurement time will alter the equations a little, but the conclusions about sampling resolution, fall and rise times, remain more or less the same.

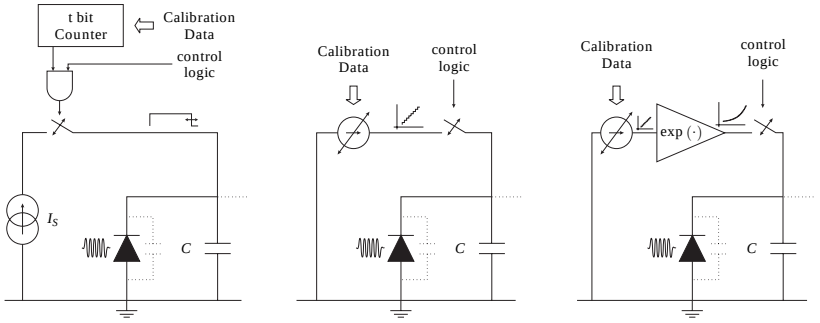
However, we mentioned in previous section that in order to reduce the maximum on chip clock frequency, the resolution for the charging voltage (NOB_V) should increase substantially. However, a digital to analog converter requires a lot of silicon area, growing steep with increasing resolution. Therefore in the next paragraph we will briefly discuss several possible DAC implementations.

3.3.6 DAC implementation

Figure 3.12 shows 3 possible implementations for the DAC. Generally we assume the measurement time and / or the capacitor is chosen so the charging voltage's dynamic range is large enough, allowing a feasable stepsize ΔV of the charging voltage.

Switched current source

Figure 3.12(a) shows a seemingly simple and straighforward implementation to minimise the silicon area and complexity of the DAC. A constant current source is used to charge the capacitor while the switch is closed and the charging time is set by a simple digital



(a) Current source DAC (b) Linear voltage DAC (c) Exponential DAC

Figure 3.12: Capacitor charging circuits: (a) with a switched current source, (b) with a linear and a (c) exponential voltage DAC.

counter. The charging voltage is given by:

$$V_{charge} = \frac{I_S \cdot \Delta t}{C} \sum_{i=0}^{t-1} b_i 2^i \tag{3.52}$$

To focus our thoughts, let us assume $C = 200\ pF$ and $V_{charge,\max} = 3\ V$. $I_S = 1\mu A$ will charge the capacitor in $600\mu s$ and for a 12 bit precision this would require a clock of $\approx 7MHz$. A smaller current will reduce this clock frequency, but results in more stern noise demands as I_S needs to be very precise. Furthermore the output voltage swing of the current source should be as high as possible. Generating a very precise and stable output current I_S independent of the output voltage, combined with fast switching of a rather large capacitive load (e.g. 200 pF) seems a design equally as challeging as a regular voltage DAC. In this work we chose to work with a voltage DAC and will not discuss a switched current source implementation.

Voltage DAC

Figure 3.12(b) shows a standard linear voltage DAC, which generates a digitally adjustable voltage and charges the capacitor with variable current. In previous sections such an implementation was

assumed and the output voltage is given by:

$$V_{DAC} = V_{comp} + V_{\min} + \Delta v \cdot \sum_{i=0}^{t-1} b_i 2^i \tag{3.53}$$

The error that is made by the finite resolution of V_{DAC} is given by:

$$\begin{aligned}(L_{PWM}(k) - L_{\min}) \cdot \frac{\Delta V}{V^*} &< L_{PWM}(k) \frac{\Delta V}{V^*} \\ &< 1\ JND - \Delta L_S - \Delta L_{r,f} < d \cdot L_{PWM}(k) \qquad (3.54) \\ \frac{\Delta v}{V^*} &< d \qquad (3.55)\end{aligned}$$

with V^* the ideal charging voltage and ΔL_S and $\Delta L_{r,f}$ the luminance errors due to sampling and rise/fall times respectively. We demanded the total error to be smaller than 1 JND, which is normally the most stringent requirement for monotonic, meaningfull and distinguishable grayscaling. With the stepsize Δv given by

$$\Delta v = \frac{\beta - 1}{2^t - 1} V_{\min} \tag{3.56}$$

Eqn. (3.55) teaches for a worst case ($V^* = V_{\min}$:

$$t \geq \log_2 \left(1 + \frac{\beta - 1}{d}\right) \tag{3.57}$$

We discussed that an increase in resolution (t) will lower the corresponding luminance error ΔL_V and allow for lower sampling speeds as ΔL_S can be larger. However, a digital to analog converter requires a lot of silicon area, growing steep with increasing resolution.

Important in Eqn. (3.55) is that for larger V^* also a larger stepsize Δv is allowed as the relative error should be small enough. Previous calculations always assumed the worst case scenario where $V^* = V_{\min}$ ($\beta^* = 1$), which yields a very small Δv and as the DAC is linear, a very high required resolution to span the range defined by $\beta_{\max}$. It is clear that a linear DAC is not a good choice when the relative error is important. Figure 3.12(c) shows an implementation where

we use an exponential amplifier, resulting in facto in an exponential DAC. The output voltage is given by:

$$V_{DAC} = V_{comp} + V_{\min} \cdot e^{\delta v \cdot \sum_{i=0}^{t-1} b_i 2^i} \tag{3.58}$$

The difference between two succeding values is now proportional to the selected value:

$$\Delta v_- = \hat{V}(i)\left(1 - e^{-\delta v}\right) \tag{3.59}$$

$$\Delta v_+ = \hat{V}(i)\left(e^{\delta v} - 1\right) \tag{3.60}$$

with $\hat{V}(i)$ the selected value. As $V^* \in \left[\hat{V} - \Delta v_-, \hat{V} + \Delta v_+\right]$, it can be shown that:

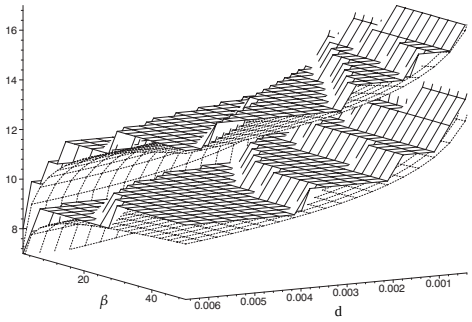
$$t \geq \log_2\left(1 + \frac{\ln(\beta)}{\ln\left(\frac{2+d}{2-d}\right)}\right) \tag{3.61}$$

Figure 3.12 shows the required NOB t for a linear and exponential DAC. For higher β we can win up to 3 bits in precision with an exponential amplifier, for lower β only 1 or 2 bits are won. An architecture with higher β will benifit from an exponential DAC, which can be significantly smaller, but for lower β it seems not interesting. It should be noted that the overall noise threshold remains of course the same for both DAC's. In Chapt. 6 we will discuss the circuit implementation of a linear and exponential DAC more profoundly.

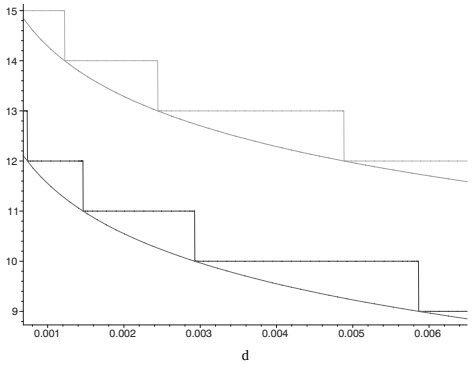
3.4 Conclusion

In the section above the optical feedback circuit was discussed for a modular display architecture. We mainly focussed on a MPSD architecture where a single driver chip is used to drive and monitor a number of pixels.

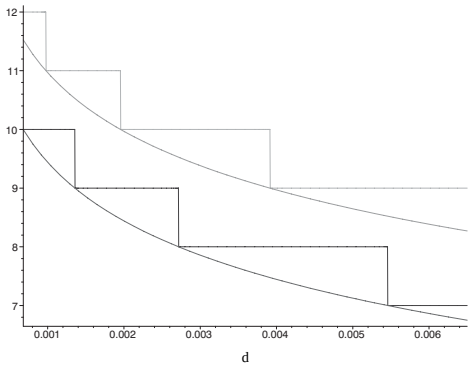
Starting with a basic optical feedback circuit as also found in literature, it was shown that implementing driver calibration into a fully analog optical feedback circuit requires some design changes.



(a) NOB_V as function of β and d



(b) NOB_V for $\beta = 20$



(c) NOB_V for $\beta = 2$

Figure 3.13: NOB_V for a linear and exponential DAC.

The use of a single voltage for both grayscaling and calibration results in an extremely stringent DAC requirement.

An easy adaptation to digital grayscaling was proposed and showed that concatenation to a single PWM pulse was necessary to reduce transient problems. For a MPSD architecture we estimated the expected photocurrents. The high bandwidth requirements however allowed only integrated photodiodes with low responivity. We showed that, at least for a MPSD architecture, the high bandwidth was clearly an issue.

This leaded to the proposal of a sampled feedback mechanism, solely for ageing correction, with reduced measurement bandwidth. Furthermore a MPSD architecture needs an ambient light reduction circuit and a possible implementation of such a circuit was presented. As the goal of the optical feedback circuit is to preserve display uniformity, the most important design parameters (only on a macro level) were discussed and their requirements to achieve monotonic (meaning each next graylevel is brighter than the former), distinguishable (meaning any two graylevels are always > 1 JND from each other) and uniform grayscaling. We found that a silicon implementation for high end displays is not so evident. The playback frequency tends to be unfeasably high and the ALR circuit should be a very low noise design. By increasing the DAC resolution both constraints can be lowered. The reduced measurement bandwith has the advantage that also slower photodetectors can be used with higher responsivity. This could further simplify the ALR circuit design.

4
Driver Architecture

Whereas previous chapter focused on the architecture of the optical feedback circuit, this is only a part of the driver IC. Therefore, before continuing to the actual driver schematics implementation, we will present the entire driver IC's architecture as well as discuss some additional considerations regarding this architecture.

4.1 Block Diagram

The global driver block diagram is shown in Fig. 4.1. Note that module sizes do not at all correspond to actual silicon implementation sizes. Basically the driver can be devided into 3 main parts.

Firstly an analog "measurement mode" part which consists of the optical feedback circuit (OFC) as discussed in previous chapter, the photodetector (or array of photodetectors), the DAC and appropriate registers.

Secondly there is a "video mode" part where the measured duty cycle and video data are used to drive the pixel's output stage. In

contrast to the "measurement mode" part the basic building block as shown on the block diagram (Fig. 4.1) is necessary for each driven pixel. The output stage is of course very dependent on the type of emissive technology that is used.

Thirdly there is a digital part which attends to interfacing and data handling, but also has the circuits to generate clocks, timing signals and general control signals for the two other parts. In the next sections we will discuss some considerations about data handling, clock generation and general driver architecture.

4.2 Dataflow

4.2.1 Addressing the driver

A typical modular display (like a LED wall) is build out of panels, typically of 50x50 to 100x100 tricolor pixels[1]. The modular approach in this work assumed tiles of 3x3 or 4x4 tricolor pixels each with their own driver IC. Therefore each panel will consist of a high number of tiles that have to recieve data to drive their pixels. Because the driver IC can be easily endowed with additional communicational intelligence, different adressing schemes are possible which are illustrated in Fig. 4.2.

Data shifting An easy way to adress all pixels would be to shift the data through from driver IC to driver IC. This means a predefined path between the tiles should exist and all data is transmitted serially. Once all data has been shifted through the tiles are allowed to read the data. This approach does not require any address for the tiles.

Active Matrix To reduce the bandwidth the tiles can be placed in a matrix and each driver IC can be provided with a row select input and a data input. Only when the driver IC detects a high row select input will it accept the data on the data line. This is similar to an active matrix used in LCD displays and allows to

[1] based on the online BARCO product spectrum

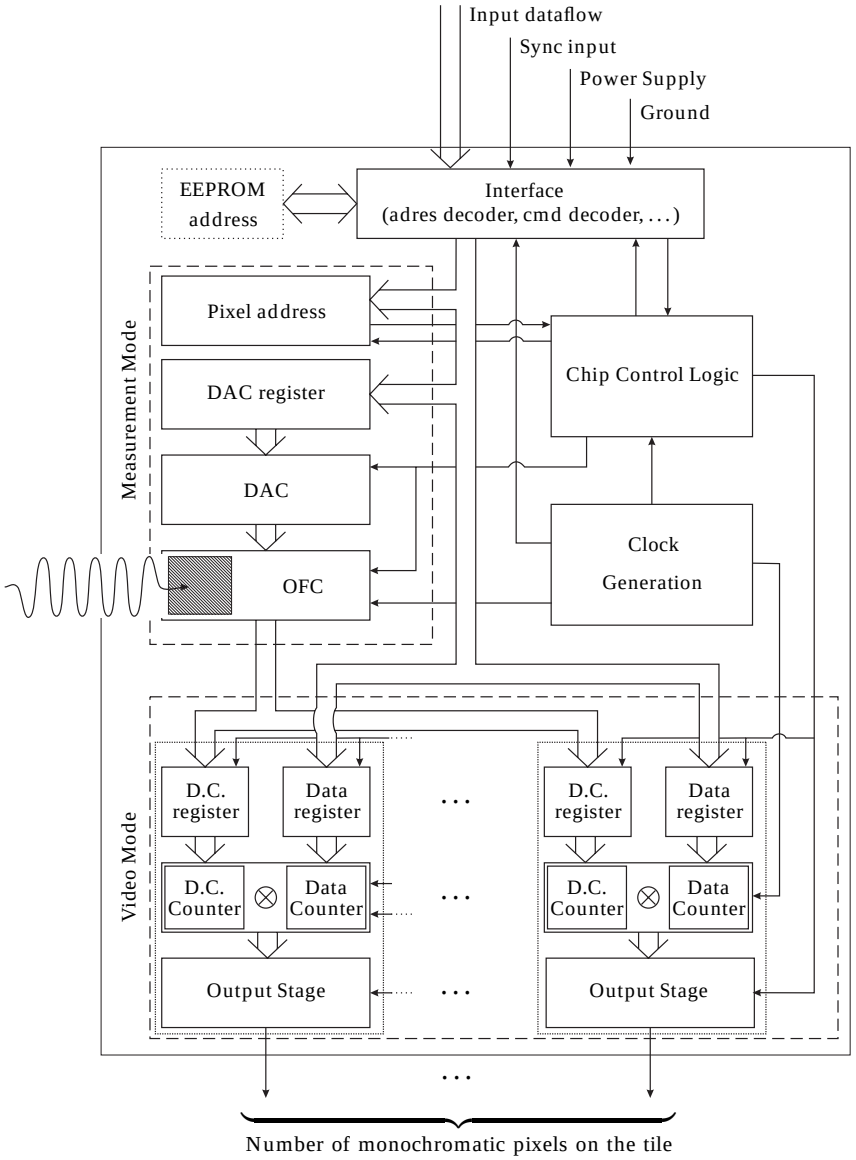
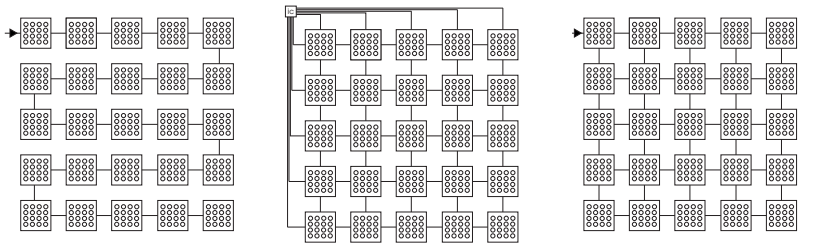


Figure 4.1: Driver Block Diagram



(a) Data shifting (b) Active matrix (c) Dedicated addressing

Figure 4.2: Panel buildup illustration

reduce the datastream bandwidth with the number of colums as all column get their data simultaneously. However an extra driver / multiplexer IC is necessary to drive the different rows and columns.

EEPROM addressable The modular approach of the display opens the possibility for free-form displays where we can easily add or remove some tiles. By connecting all tiles to a bus system and providing them with an address, each tile can be addressed seperatly, regardless of the display's form or the number of tiles. Of course an external operator should be aware of the exact position of each tile and their corresponding address. Each tile should have a unique address so a programmable memory block should be available on each tile. For silicon technologies with EEPROM extension available the address memory (only a few bytes at most) can be integrated within the driver IC, but a seperate memory IC would also suffice. The tile address should be programmed before the tile is inserted in the display or the possibility for easy in situ programming should be available.

Freeform auto adressing In this context it is usefull to mention the state of the art for modular display addressing. [17] and [37] present a modular display architecture with auto addressing mechanism. In this approach, each (rectangular) tile can have four neighbours (up,down,right,left) and is connected to them

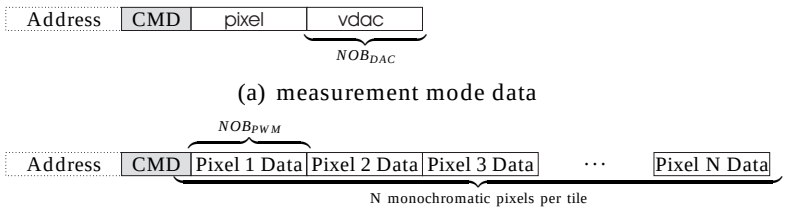
through the driver IC. Thus a grid is formed (possibly with holes as it is a free-form display) and only one tile (or driver IC) is connected to the outside interface. At startup the interface will give this module an address. Once the tile has an address it will allow address requests from its neighbouring tiles. A request algorithm will thus provide each driver IC with a unique address. Once the algorithm is sure all tiles have their addresses, each driver IC will function as grid knot which bypasses all data which isn't addressed to it. This algorithm requires only digital circuits and is easily integrated in the driver IC. No information on silicon area is yet available.

In this work we did not go as far as a full tile assembly and therefore did not integrate an on chip EEPROM address memory nor the proposed algorithm from [17, 37]. Our prototype driver has an enable pin either for matrix adressing or for an external address decoder.

It should be noted that serial data transmission will lead to rather high bitrates. A panel of 81x81 pixels, conveniently consisting of 27x27 tiles of 3x3 tricolor pixels, will need $3 \cdot NOB_{PWM}$ bits for each tricolor pixel. For a low end display we found still 11 bit PWM was required, leading to $\approx$ 12kbit data. With a refreshrate of 60Hz a bitrate of at least 12Mbit is required. This is purely the data, without additional address bits, header bits, error bits. In an active matrix addressing scheme this would be divided by the number of columns, in casu 27. Also the other mentioned architectures could implement some degree of parallellism, however at the cost of additional external drivers or extra data lines and I/O for the driver IC.

4.2.2 Driver operation

The driver has two operation modes: a measurement mode during which a new duty cycle is measured and video mode where the stored measurement is used for driving the pixel(s). The data handling block should allow data to be processed and stored correctly. Therefore Fig. 4.3 shows the introduction of a small header to the



(a) measurement mode data

(b) normal operation data

Figure 4.3: Data protocol for the driver IC

datastream which allows the driver to differentiate between the two modes. This header can also be used to do a full reset or power down of the tile.

Measurement mode

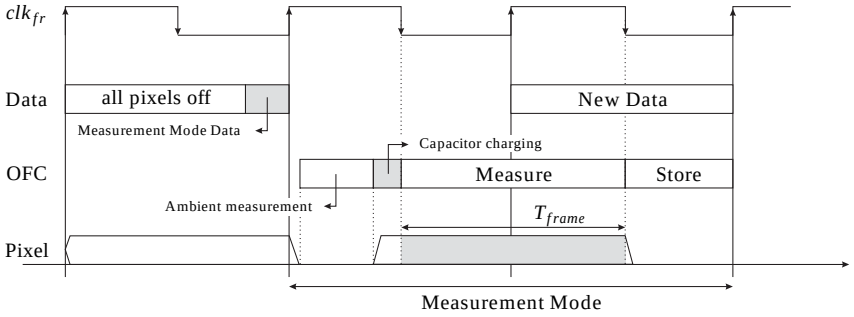


Figure 4.4: Measurement mode operation

When a measurement is performed, the driver IC requires foremost the pixel address on tile. For example a 3x3 tile has 9x3 monochromatic pixels (RGB) and would require a 5 bit tile address. This address is stored in the "pixel address register". The control logic (see Fig. 4.1) will use this address to activate the correct output stage and deactivate all other pixels on the tile. Afterwards, the control logic will store the measured duty cycle in the "DC register" of the correct pixel. Secondly a NOB_V bits set up value for the DAC

voltage is required. This value is specific for each pixel, but as we use a sampled feedback, is only required when a measurement is performed and should not be stored on the driver IC or on the tile. In stead it can for example be stored with the software controlling the display.

When the measurement cycle begins, first an ambient light measurement is conducted, followed by the actual measurement. During this time it is clear no pixels in the vicinity should be activated as they would disturb the measurement. Therefore during the previous frame all pixels should be set to the off state. For the pixels that are measured this is overridden by their driver IC. The pixel is activated, the capacitor loaded with the correct DAC voltage and a ambient light corrected measurement is performed. After the measurement, all pixels can recieve new video data. As a measurement only takes a few frames, a panel can be recalibrated within a very short time. For example for a panel with 81x81 pixels (typical for e.g. LED panels) consisting of 3x3 tiles where only 9 pixels are measured simultaniously, requires less then $\approx$ 60 seconds for a full "update".

Video mode

Once a pixel has been measured the "DC register" has a value writen to it and video mode operation can be used. This is the normal operation mode where video data is used to drive the pixels. During this mode each pixel needs to be supplied by a NOB_{PWM} bit data word every frame (see Fig. 4.3). As mentioned a fully serial approach for the entire display can lead to rater large bitrates. As this data is to be transmitted before the next frame, each pixel requires a data register to store its video data in.

Initial Calibration

During initial calibration the appropriate DAC voltage for each pixel should be determined by means of an external measurement that is equal for all pixels. This can be done in an iterative way, where the display switches constantly between measurement mode and video mode operation. First an arbitrary DAC value is used, an on chip

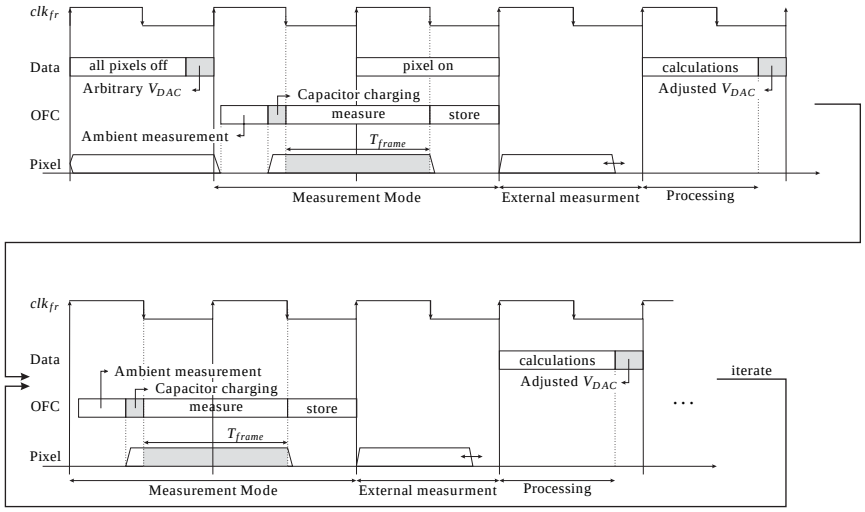


Figure 4.5: Calibration mode operation

measurement is performed to establish the duty cycle. Next the pixel is driven in video mode and an external measurement is made. Due to the external clk_{frame} that is used as synchronisation signal, this can be done easily. The external measurement system can easily calculate a better DAC voltage for the pixel and a new measurement can be performed. After a few iterations, the optimal DAC value is found and this can be stored on the driving PC. Whenever an "update" is needed these values can easily be transmitted to the appropriate driver IC as mentioned above.

4.3 Clock generation and synchronisation considerations

As all driver IC's work independantly from each other, some synchronisation is required to indicate the beginning of frames. An obvious choice would be to distribute the frame clock clk_{frame} to the different driver IC's. On the other hand, we already showed the driver IC needs a rather high internal clock frequency (up to 1 GHz)

to create the duty cycle for the PWM control. Deducing this clock via DLL or PLL from the distributed clock would ensure synchronisation and equallity over the different driver IC's, yet a seemingly impossible task because of the very large upscaling ratio. The distributed clock should be as low as possible because of the large capacitive load (all the different tiles), yet this is inversely proportional to the upscaling ratio.

However for the internal clock frequencies f_{DC} and f_M there is no need of synchronisation between the different driver IC's. An on chip measurement is totally independent from the outside world and simply measures the duration of a duty cylce. It does not need to be synchronised to anything. At normal operation f_{DC} is used to recreate the duty cycle. Only the start of a frame is important and requires a sync signal. Once the frame has started the internal clock clk_{DC} can start the counting. Without inter IC synchronisation at worst a shift of 1 periode t_{DC} can occur, which is without any consequence.

Even more important is that also IC to IC variations in clock frequency are perfectly acceptable. When a measurement is performed the duty cycle is stored as a number of clock periods t_M. For this measurement we showed a full frame measurement was best and derived a minimum resolution so the sampling error would be low enough. This is the only constraint for t_M:

$$t_M \leq \frac{t_{frame}}{2^{NOB_S} - 1} \tag{4.1}$$

A different clock periode t_M will simply yield a different count for the same duty cycle. At normal operation the same clock is used and the correct duration is obtained. If a variation α exists between the different IC's, then $t_M \cdot (1 + \alpha)$ should comply with Eqn. (4.1). This means t_M will overflow the measurement counter before the end of the measurement time (1 frame period) but this is easily solved by expanding the counter with one bit.

The above considerations imply that no extensive synchronisation effort is required on chip and frequency spread is allowed. On the other hand clock jitter, drift and temperature behaviour do are important. Clock jitter and temperature drift will introduce addi-

tional errors on the duty cycle duration. Time dependent frenquency drift on the other hand is only important untill the next measurement, when it is "reset". As the design of on chip clock generation is a research effort "an sich" we used an externally provided clock for prototype testing.

5
Integrated Photodetectors

Based on the analysis of the previous chapters we can start with the actual design of a test IC. Whereas chapter 6 will explain the implementation of the discussed circuits in silicon, this chapter starts with the design of photodetectors. In this work all circuits are designed in ON Semiconductor's I^2T100 technology. This technology is a $0.7\mu m$ 100V BCD process with many more layers available than in a standard CMOS process. Special diffusions and implants are indeed needed for the high breakdown requirements (100V) of the DMOS structures that are available in this technology. The circuits discussed in chapter 6 only use the $0.7\mu m$ 5V CMOS technology node that is defined in I^2T100, yet for the design of photodetectors the availability of extra layers is very interesting. As mentioned before some display technologies have higher voltage requirements than the standard 5V CMOS provides and a higher voltage technology becomes necessary. These two reasons justify the choice for I^2T100 as a the technology used in this research.

In this chapter we will briefly present the well known physical mechanism for optical generation in Sect. 5.1 for better understand-

ing. Section 5.2 will discuss the design of integrated photodiodes in I^2T100. We discuss device simulations, actual silicon implementation and measurements. Section 5.3 will do the same for integrated phototransistors.

5.1 Photogeneration in silicon

5.1.1 Optical absorption

Optical detectors in semiconductor technologies are based on the absorption of the energy of incident photons. The energy of a photon can be transferred to an electron in the valence band and thus this electron can be brought to the conduction band of the semiconductor where it contributes to a current. An electron-hole pair is thus generated. With the photon energy given by:

$$E_{photon} = h \cdot \nu = \frac{hc_0}{\lambda_0} \tag{5.1}$$

it is clear the electron in the valence band needs an additional energy larg enough to cross the silicon bandgap $E_g^{Si} = 1.1eV$. This means photons with a lower energy (which is light with larger wavelength) will not be absorbed. For silicon this means the wavelength of the incident light

$$\lambda \leq 1110nm \tag{5.2}$$

to be absorbed and for higher λ silicon is transparant. For smaller wavelengths an absoption coefficient $\alpha(\lambda)$ is defined which defines the penetration depth $1/\alpha(\lambda)$ of the light into silicon based on Lambert-Beer's law:

$$I(y) = I_0 \exp^{(-\alpha(\lambda)y)} \tag{5.3}$$

Here $I(y)$ [photons$\cdot cm^{-2} \cdot s^{-1}$] represents the intensity of light at depth y and I_0 is the light intensity at the silicon surface. Figure 5.1 shows the penetration depth of visual light in silicon which goes up to several μm for red light. As we used in this work green, blue and red LED's, Table 1.1 lists the specific penetration depths at their specific wavelenghts.

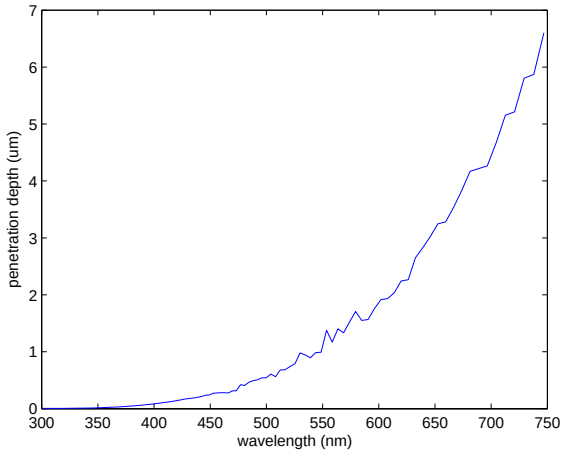


Figure 5.1: Penetration depth over visual spectrum

Color	Central Wavelength	$1/\alpha$
blue	$470nm$	$310nm$
green	$540nm$	$890nm$
red	$635nm$	$2.6\mu m$

Table 5.1: Penetration depth of Red, Green and Blue (RGB) LEDs in silicon.

5.1.2 Photocurrent

As described previously, the generation of electron-hole pairs occurs as photons with energy greater than the bandgap are absorbed. However in normal conditions these electron-hole pairs will be subject to recombination to maintain equilibrum in the semiconductor. Therefore the generated electron-hole pairs need to be collected to minimise recombination. This is done via a pn junction shown in Figure 5.2 ([38]). The electrical field that is present in the depletion layer at the junction will pull the electrons to the p-type material where they recombinate and generate a majority current. The holes on the other hand are pulled to the n-type material. Thus the electron hole pair no longer recombinates and contributes to a

"photocurrent". Clearly a wider depletion layer will increase the photocurrent. The analytical expression for an abrupt pn junction is given by:

$$W = \sqrt{\frac{2\varepsilon_r\varepsilon_0}{q}\frac{N_A+N_D}{N_AN_D}\left(\frac{kT}{q}\ln\left(\frac{N_AN_D}{n_i^2}\right)-U-\frac{2kT}{q}\right)} \quad (5.4)$$

with N_A and N_B the doping levels of the p and n-type respectively. U is the applied voltage over the pn junction. Two things are important: a lower doping will increase the width of the depletion layer and a negative volage U as well.

Photons incident beyond the depletion layer will also create electron hole pairs, yet in regions where no electrical field is present. Therefore these pairs will recombinate and not add to the photocurrent. However some of the minority carriers will enter the depletion layer through diffusion before they recombinate and still add to the photocurrent. The distance over which minority carriers diffuse is called the diffusion length $L_{n/p}$. An analytical expression for $L_{n/p}$ is rather complex, but it is obvious that lower doped regions have a lower recombination speed and thus a higher diffusion length. Diffusion length is difficult to calculate but [39] mentions several tens of μm are possible in standard low doped silicon. Note that for example for solar cells diffusion based photocurrent is the main contributor to the photocurrent and technologies are used with diffusion lengths of $1mm$!

Clearly the easiest way to make a photodetector is a simple pn junction. As this is basically a diode, these photodetectors are called photodiodes. Therefore next section will discuss the (limited) possibilities to create photodiodes in I^2T100.

5.2 Photodiodes

5.2.1 CMOS compatible photodiode

To form a pn junction there are a limited number of possibilities in I^2T100. The technology has a p-substrate with a low doped ptype

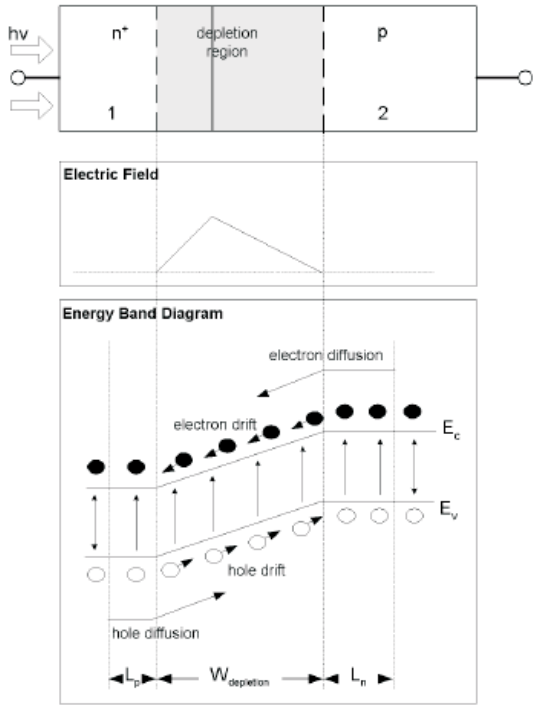


Figure 5.2: Schematic representation of a pn juntion in silicon

epitaxial layer (PEPI) on top. In this PEPI a twin well (NWELL / P-WELL) process is defined as is common for CMOS processes. Contacts, drains and sources of the MOST's are made in highly doped p+ and n+ diffusions (NDIFF / PDIFF). In the standard CMOS this means only following structures are possible:

1. NWELL / PEPI
2. NDIFF / PEPI
3. NDIFF / PWELL / PEPI

From the previous section we learned that low doped regions are best suited as they give a larger depletion region. This means the third option is not really interesting compared to the second one since the PWELL has a higher dopation than the PEPI. The choice between the first two options is also logical: a lower doped NWELL will extend the depletion width in both PEPI and NWELL. The only downside is that the NWELL / PEPI junction lays deeper under the silicon surface and based on eqn. (5.3) this means some portion of the light will already be absorbed before it reaches the active junction.

In this work we were able to recieve the actual process data from the I^2T100 proces from ON semiconductor. This was used for physical simulations with ISE TCAD software. This allowed to simulate the exact physical process steps such as implantations, diffusions,... to virtually create the device. With this physical simulation also the opto-electrical behaviour of the device can then be simulated. Figure 5.3 shows a 2D cross section of a simple NWELL / PEPI structure. The NWELL (cathode) is connected to a 2V DC value and thus the diode is reversely biased. The white lines represent the boundries of the depletion layer and show the depletion region is $\approx 1\mu m$ wide. The cathode (NWELL) current is collected by a n+ doped region within the nwell, the anode (PEPI) current is collected partially through the bottom contact of the substrate and partially throught he PDIFF diffusions on ground potential in the PEPI.

As all process parameters are strictly set, doping levels can not be optimised towards optical performance. Only the layout of the device can be chosen freely. Simply increasing the width of the

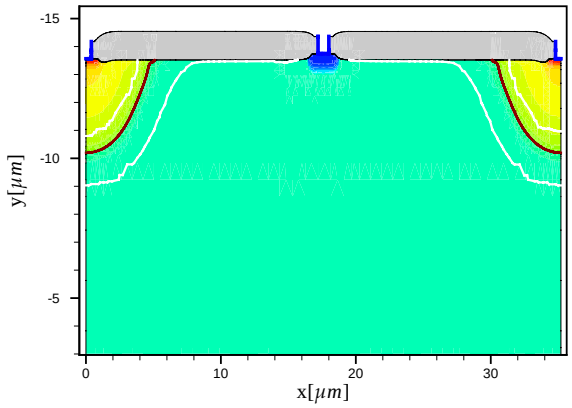


Figure 5.3: CMOS photodiode: NWELL/PEPI junction forms the active region. Cathode is set at 2V.

Nwell (and thus of the diode) will increase the depletion area and proportionally with the area the photocurrent will rise. However as can be seen in Fig. 5.3 the depletion region follows the junction up to the surface of the silicon. These vertical borders of the Nwell should contribute much more to the creation of photocurrent as they are placed vertically. Figure 5.4 shows how NWELL "cells" in the PEPI will create more of these vertical junctions to improve the responsivity. One could chose the NWELL spacing so the vertical junctions would touch each other and thus create large depleted regions. However there is a downside to this structure: each NWELL should of course be connected separately, resulting in an increased area needed for metalisation to extract the anaode currents. Also the intermediate PEPI areas should be connected to extract the current efficiently. The added metalisation would overlap most of the depleted regions between the wells. Therefore we chose the spacing between the NWELL's so the metal would not cover the vertical depletion regions. On Fig. 5.3 we see the depletion layer is $\approx 2.5\mu m$ wide into the PEPI. A minimum PDIFF contact dimension in I^2T100 is $1.6\mu m$ which means optimally the spacing between the NWELL's should be $6.6\mu m$. In the NWELL the depletion layer only extends

for $\approx 1\mu m$. Also a NDIFF contact of $1.6\mu m$ is needed here and the NWELL can be chosen $3.6\mu m$ wide. Before discussing the measurements on this diode we will also describe a photodiode which uses the available BCD layers of I^2T100.

5.2.2 BCD compatible photodiode

As mentioned I^2T100 is a BCD process with several additional process steps to allow high voltage DMOS devices to be made next to the standard CMOS node. Practically a few process steps are important:

1. NTUB: this is a deep but low doped n-type implant. It is used to isolate High Voltage nDMOS devices from the ptype PEPI so they can be floating. As it also functions to create a drift region for the I^2T100 lateral DMOS's its doping level should be high enough to allow small DMOS structures but low enough to reduce the added series resistance. It is much lower doped than a standard CMOS NWELL.

2. BLN: a very high doped ntype implant that is placed in the substrate before the EPI is grown. It is for isolation of the NTUB towards the substrate. NTUB and substrate are low doped and pulling the NTUB higher than ground (substrate) will create a large depletion area. When the voltage becomes too high punchthrough of the NTUB will occur. Therefore a highly doped BLN is placed underneath each NTUB to avoid this.

Basically the low doped NTUB layer offers new possibilities for a better photodiode. To have a better understanding of how to use this implant we will briefly describe the sequence of the most important process steps of I^2T100 that were used:

substrate We start from the low doped ptype substrate.

BLN implant A very high doped n+ is implanted in the substrate. The implantation dose is roughly comparable to the n+ implant used for the drains / sources of the MOST devices.

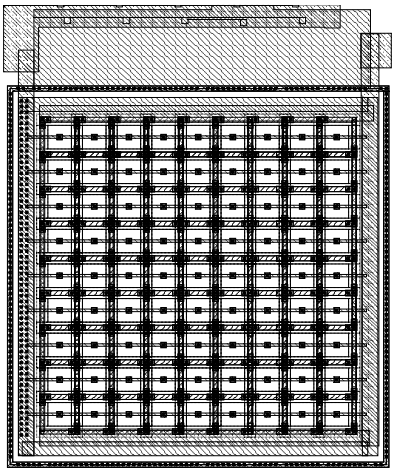


Figure 5.4: IC layout of the 2D Nwell/Epi structure. The idea is followed in both x and y axis, resulting in a cell based photodiode.

BLN annealing After the implant a long and heavy (high temperature) annealing step is done to diffund the BLN implant more uniformly over a wider area.

EPI growth Next the ptype EPI is grown on top of the substrate. In this EPI, typically only 10-15μm thick, the actual devices will be formed.

NTUB implant The next implant is the one for the NTUB. This is a lower doped ntype implant but as it need to reach the BLN in NDMOS devices, it is implanted with high energy.

NTUB annealing More important for us the implant phase is followed by a very long and high temperature annealing process to diffund the NTUB implant uniformily and all the way up to the BLN. This means the NTUB will be a very large structure and it is difficult to control the exact dimensions due to this large diffusion in all directions.

CMOS WELLS After the NTUB is placed the normal CMOS process steps are undertaken. The PWELL and NWELL's are implanted and annealed. However the annealing steps here

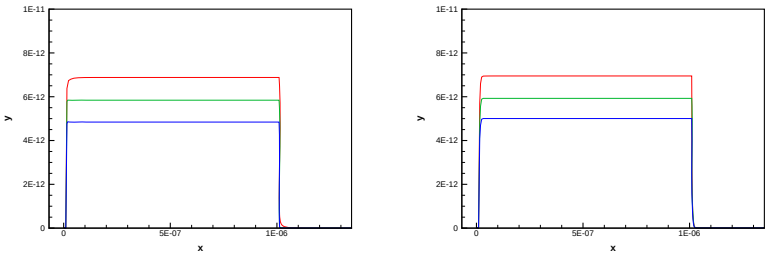
are much less than the ones used for BLN and NTUB and therefore the dimensions are much better controllable.

CMOS n+/p+ Finally gate oxides and poly gates are defined. Next the source / drain and contacts active regions are implanted.

Though the NTUB layer is indeed low doped and interesting, we see it has some drawbacks for the design of a photodiode. For example one could duplicate the NWELL / PEPI structure as described in Sect. 5.2.1 but with NTUB cells instead. However the large size due to the heavy annealing step of the NTUB would result in an NTUB of over $20\mu m$ wide. Clearly to create such a photodiode a very large IC area is needed but not available for this research. Furthermore the gain in vertical depletion area at the NTUB vertical borders would be reduced by the large necessary spacing between the NTUB's. Therefore such a device was nor simulated nor designed.

Other interesting possibilities based on the NTUB layer do exist however. Figure 5.6 shows the dual structure of the CMOS compatible diode: a PWELL inside the NTUB. Comparing to the CMOS photodiode we see the PWELL / NTUB junction is a bit smaller. Here the same cell based structure can be defined, yet now underneath this upper cell structure there is an extra, much wider depletion layer between the NTUB and PEPI. This is shown in Fig. 5.6. The normal BLN underneath the NTUB is specifically not included as it would destroy this depletion layer. From a NDMOS point of view this is necessary, yet for an optical device this is not wanted. It should however be noted that this extra depletion layer is located rather deep into the device: $\approx 8\mu m$. With the values of penetration depths from Table 5.1 in mind, this junction will only contribute to the photocurrent for reddish light, but almost nothing for blue light. As can be seen from Fig. 5.6 the depletion layer between NTUB / PEPI is roughly equally wide in the NTUB as in the PEPI layer, showing very similary doping for these layers. Because of this extra depletion layer we expect a better performance of the BCD photodiode than the pure CMOS diode.

Figure 5.5 shows the 2D simulated photocurrent $[A / \mu m]$ through a single CMOS cell and its BCD counterpart. The devices were sim-



(a) Simulated photocurrent of a single CMOS cell.

(b) Simulated photocurrent of a single BCD cell.

Figure 5.5: Simulation of the photocurrent in a single CMOS (left) and BCD (right) cell.

ulated with a transient simulation for red, green and blue light with an cathode (ntype) voltage of 2V. We see a very fast response as expected for a photodiode and indeed a higher photocurrent for the BCD diode than the CMOS diode.

5.2.3 Measurements

The measurements of the on chip photodetectors were done with a red, green and blue LED with lambertian radiation pattern. These LEDs were placed $15cm$ and orthogonally above the IC, so the incident optical power is very uniform over the IC surface which is only a few mm^2. The LED current was swept and the incident optical power at the silicon surface was measured with a calibrated $1cm^2$ optical detector as a reference. The on chip devices were measured with a high precision Source Measure Unit (SMU) on a probing station, a setup capable of measuring $< 1pA$ currents. The photodiodes were biased with 2V on their cathode.

Figures 5.7 show the measured photocurrents for the CMOS photodiode with NWELL / PEPI. The device has an area of $100\mu m^2$, comprising of 9x9 active cells (see Fig. 5.4). Figure 5.8 shows the measurement for its BCD counterpart with PWELL in NTUB. We see indeed that the blue light gives less photocurrent as expected. To be able to qualify these photodiodes an interesting parameter is the

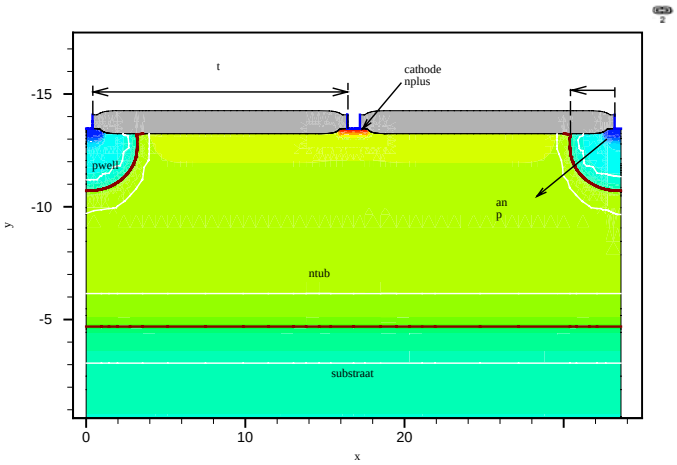


Figure 5.6: BCD photodiode. The white lines depict the depletion layers. The cathode is set at 2V.

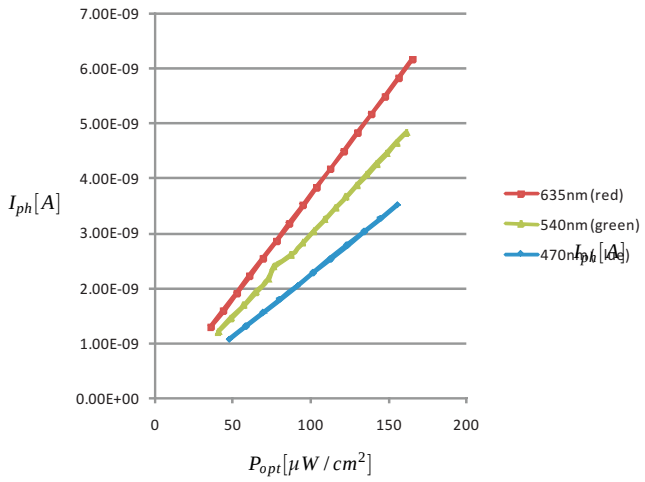


Figure 5.7: CMOS photodiode: NWELL / PEPI

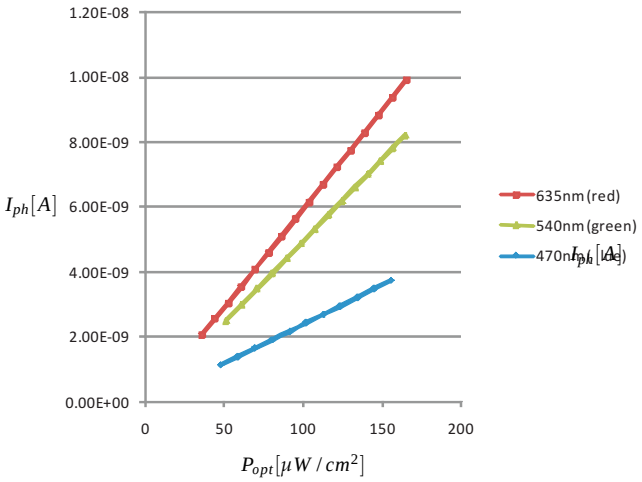


Figure 5.8: BCD photodiode: PWELL / NTUB

responsivity of the detector ([39]):

$$R = \frac{I_{ph}}{P_{opt}} = \frac{q\lambda}{hc}\eta = \frac{\eta\lambda[\mu m]}{1.243}\frac{A}{W} \tag{5.5}$$

The responsivity is defined as the resulting photocurrent I_{ph} for a certain incident optical power and can be expressed as a function of the quantum efficiency η of the detector and the wavelength λ of the incident light. The quantum efficiency η is a measure for the fraction of incident light that actually contributes to the photocurrent. A part of the incident light will reflect from the surface of the photodetector, resulting in an optical quantum efficiency η_0 and the remaining photons will not all contribute to the photocurrent, defining an internal quantum efficiency η_i:

$$\eta = \eta_0 \cdot \eta_i \tag{5.6}$$

For an ideal photodetector $\eta_i = 1$ the maximum responsivity for a silicon resistor are listed in Table 5.2, both with and without the optical quantum efficiency taken into account (with η_0 calculated based on the index of refraction of silicon [39]).

Color	Central Wavelength	$R(\eta_0 = 1)$	η_0	$R(\eta_0 \neq 1)$
blue	$470nm$	0.38	0.77	0.29
green	$540nm$	0.43	0.82	0.35
red	$635nm$	0.51	0.84	0.43

Table 5.2: Maximum Responsivity and optical quantum efficiency for the measurements.

Color	Central Wavelength	$R(CMOS)$	$R(BCD)$
blue	$470nm$	0.22	0.24
green	$540nm$	0.3	0.5
red	$635nm$	0.37	0.6

Table 5.3: Measured responsivities for CMOS and BCD photodiode

However, when looking at Fig. 5.7 and 5.8 we find the responsivities listed in Table 5.4. For the CMOS photodiode they are very close to the maximum value and for the BCD photodiode we find higher responsivities than theoretically possible!

In section 5.1 we already mentioned the existence of two types of photocurrent contributions: drift driven photocurrent and diffusion driven photocurrent. Figure 5.9 shows a cross section of a simulation of the BCD photodiode (PWELL / NTUB). Surrounding the active device a large PEPI region is simulated as is the case for the actual implementation on the IC. Both PWELL anode and PEPI substrate are connected to ground, the cathode is set at 2V. Figure 5.10 shows the simulated photocurrents throught the different contacts with incident light of $635nm$ (red light). The dotted lines show the generated photocurrent if the light only falls from $x \in [20\mu m, 50\mu m]$, whereas the solid lines give the photocurrent when also on the surrounding PEPI there is incident light.

From Fig. 5.10 we see the anode current is the same in both cases. The anode current is the current collected at the PWELL and comes from the depletion region between NTUB and PWELL. The substrate contact gives a much higher contribution in this simulation

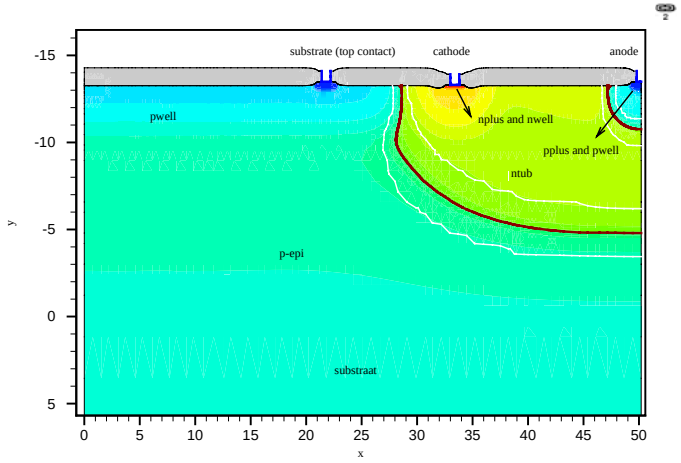


Figure 5.9: PEPI edge around the BCD photodetector. The PWELL implant generates a gradient in the edge.

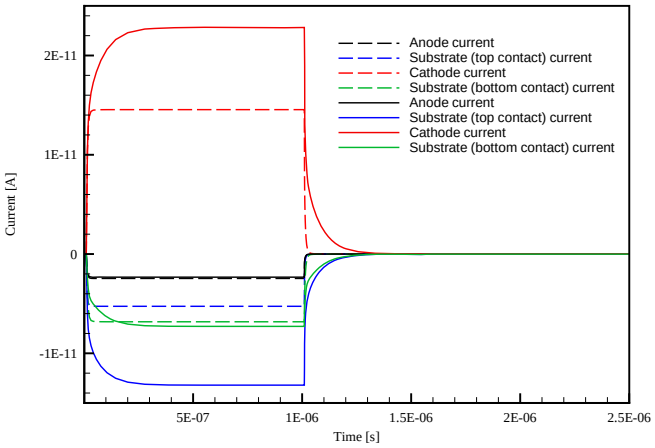


Figure 5.10: Influence of PEPI edge around the BCD photodiode on the photocurrent.

which is obvious when we compare the depletion layers in Fig. 5.9. When we enlarge the PEPI region with $20\mu m$, the anode current remains exactly the same as is to be expected. However the substrate and cathode currents increase significantly. As can be seen the solid lines also rise much slower, showing this is probably a diffusion contribution. It should be noted that the PEPI region is not perfectly uniform doped. In I^2T100 all open area gets a default PWELL implant as can be seen in Fig. 5.9. This implant induces a certain gradient in the doping profile and thus a small electrical field is present in the surrounding PEPI. Clearly this gives a small drift to the holes and electrons which seemingly increases the diffusion length even further!

We did simulations up to several tens of μm of surrounding PEPI and the influence remained even for large distances. Figure 5.11 shows the layout of the photodetectors on the test IC. Though we created all different devices with exactly the same dimensions, their distance to other devices and their surrounding area is different! This makes it basically impossible to obtain a decent comparison between the different devices. To reduce the diffusion contribution we used a copper foil to cover the IC. In this foil openings were made with a laser to allow incident light on the photodiodes. This foil was then glued with a flip chip technique onto the IC. Figure 5.12 shows the measured photocurrents of the BCD photodiode for both unshielded and shielded IC. Clearly the measured photocurrent is much lower and more realistic responsivities are found as shown in Table 5.4. However to be able to land with the prober needles on the bonding pads there was still some (very small) area that is open to incident light. Therefore the responsivities of Table 5.4 could still be an overestimate.

Remarks and future work

The measurement results of the photodiodes were uncomparable due to the parasitic contribution from the device edges. For a decent characterisation of the photodiodes these contributions should be cancelled out. Figure 5.13 shows schematically how this can be done: the P+ substrate contact should be surrounded by an NWELL

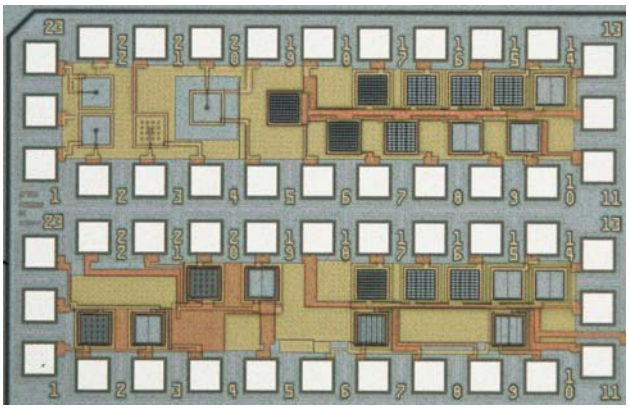


Figure 5.11: On chip photodetectors

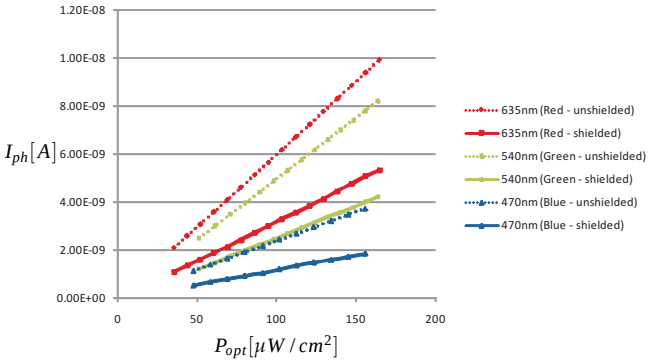


Figure 5.12: BCD diode photocurrent shielded and unshielded

Color	Central Wavelength	R (BCD - unshielded)	R (BCD - shielded)
blue	$470nm$	0.24	0.12
green	$540nm$	0.5	0.26
red	$635nm$	0.6	0.32

Table 5.4: BCD photodiode responsivities with and without the added copper foil

(or NTUB) guard ring and another P+ substrate ring. This way the holes and electrons coming from adjacent regions are collected before they can contribute to the cathode current. Note that this basically means we placed a second "photodiode" around the active device which collects all the unwanted current. The ntype guard ring should be placed at V_{dd} for best behaviour. In I^2T100 some pcells (predefined devices of the technology such as a MOST), indeed have the option for such a guard ring and even a double guardring structure (see Fig. 5.13). The photodiode measurements show why.

5.3 Phototransistors

In the previous section we mentioned that photodiodes have theoretically a quite small responsivity of maximum $0.5A/W$. As mentioned in Chapter 3 this is a major problem for the optical feedback loop as it means a very small magnitude of the feedback signal in a multi pixel module. To increase the feedback gain there were also phototransistors implemented on the test IC.

A phototransistor is actually a bipolar transistor that uses the base-collector diode as a photodiode which is reversly biased. The electron-hole pairs that are generated in the depletion layer will be separated by the electrical field. We will focus our thoughts on a PNP phototransistor. There the holes are send to the collector, the electrons diverted to the ntype base. These injected electrons in the base form the needed base recombination current for holes injected from the emittor and the optically generated base current is aug-

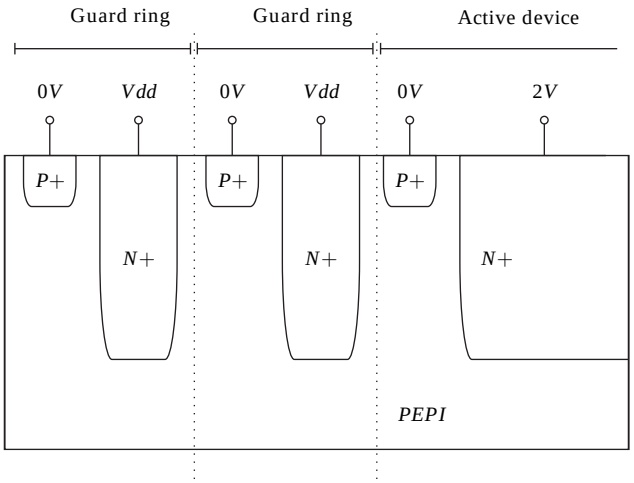


Figure 5.13: Schematic representation of guardring to block the parasitic contribution

mented by the current gain β of the bipolar transistor. The base of the pnp can be left floating so no other base current will offset the signal. From [40] we learn

$$\beta \approx \frac{1}{\frac{W_B^2}{2\tau_b D_n} + \frac{D_p}{D_n}\frac{W_B}{L_p}\frac{N_A}{N_D}} \approx \frac{2\tau_b D_n}{W_B^2} \tag{5.7}$$

with W_B the base witdth of the transistor, τ_b the minority carrier lifetime in the base (i.c. holes), D_p and D_n the diffusion constanst for holes and electrons and L_p the diffusion length for holes in the emittor. N_A and N_D are the doping densities of acceptor and donors (base). We see that a higher doping level N_D for the base is interesting and a lower doping level for emittor and collector to increase the current gain. Furthermore the same considerations that are valid for a photodiode apply to the reverse base-collector pn junction. This means a low doping level is interesting for collector and base in order to have a larger depletion region. Of course the base width W_B should be as small as possible.

5.3.1 CMOS phototransistor

Figure 5.14 shows a PNP bipolar transistor made in a standard CMOS process. The NWELL serves as a ntype base, the emittor is formed by a p+ active area diffusion and the adjacent PWELL is the collector. It should be noted that the base width is not very well defined for this device. The NWELL and PWELL implants are quite heavy and need an successive annealing step to diffuse. Therefore the exact base width is not really accurately set. This device can be optimised even further by leaving the PWELL implant next to the NWELL to increase the depletion layer of the photodiode even further. However we show this device for the dynamics of the phototransistor. Figure 5.15 shows the corresponding photocurrents that are found when illuminating the device with red light. As shown on the figure the light is incident from 10ns to 1ms. The emittor of the pnp is driven at 2V, the collector at 0V and the base contact is not connected. This means the only base current will be the photocurrent. We see as soon as the light illuminates the device, the photodiode generates a small photocurrent of a few pA. However no transistor operation is noted until $100\mu s$. Note that there is always a parasitic vertical pnp to the PEPI substrate which collects a portion of the current. In [39] values up to 40% of the emittor current because of this vertical pnp are mentioned. This corresponds with the simulation results from Fig. 5.15.

Figure 5.16 shows the electrostatic potential distribution inside the device at two distinct times. On the left side at 100ns where only a small photocurrent is seen. The right figure shows the situation at 1ms. As can be seen at 100ns the NWELL potential is still at 2V. Thus the emittor base junction is not forward biased and not bipolar operation is present. At 1ms the NWELL is brought to a lower voltage and the emittor base junction is forward biased with bipolar operation as a result. This means especially the large base collector junction capacitance has to be discharged to obtain transistor operation. However there is only the very limited photocurrent available to do this: incident photons in the depletion layer will generate electron hole pairs that will be split. The electrons are driven by the electric field to the NWELL base and will slowly build up negative

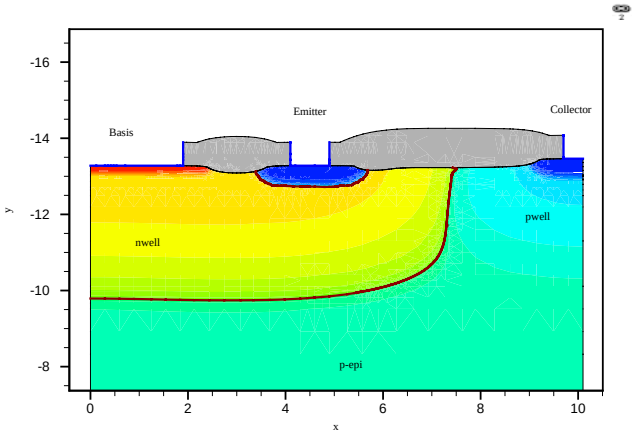


Figure 5.14: Cross section of a possible bipolar transistor in I^2T100

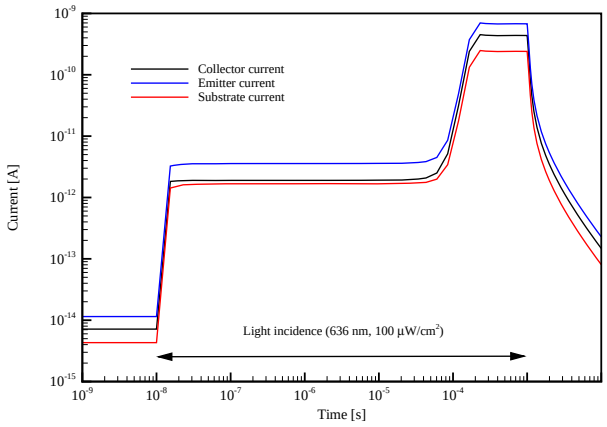


Figure 5.15: Simulated currents for a simple CMOS pnp bipolar transistor

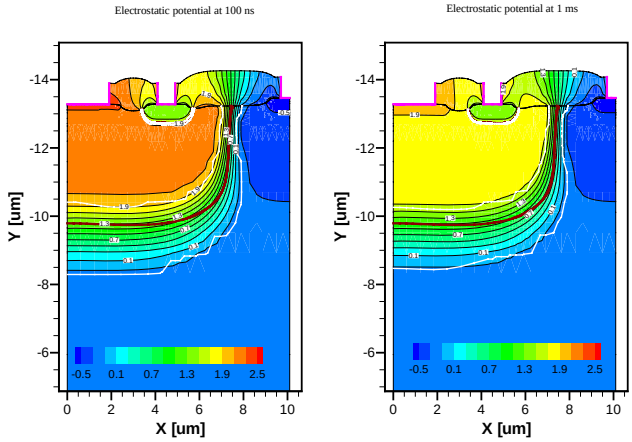


Figure 5.16: Potential gradient in the device at 100ns and 1ms

charge that pulls the base down. Only when the emittor base junction is forward biased the photo-electrons are used as the necessary recombination base current to keep this junction forward biased and provide bipolar operation.

Though the CMOS device of Fig. 5.14 works as a bipolar transistor, we already mentioned its base width is badly defined by the NWELL. In a CMOS process however the gate of the MOST is the most important parameter of the technology which is very accurately defined due to the self aligned PDIFF implant of the active area. Therefore it would be logical to use these process steps and define a "gated" base. Figure 5.17 shows schematically a standard pmos transistor. Indeed the NWELL bulk, normally connected to the source of the MOST, can be used as the base of a bipolar transistor if left floating. The source and drain can be used as collector and emittor and by enlarging the collector PDIFF diffusion the base collector junction can be increased to collect more photocurrent. The hatched area represents the active photodiode between base and collector. As mentioned there is a parasitic pnp transistor to the substrate with a much larger junction but also a much wider base (the NWELL depth). As mentioned in Sect. 5.2.1 the PDIFF / N-WELL photodiode of the base collector junction is definately not op-

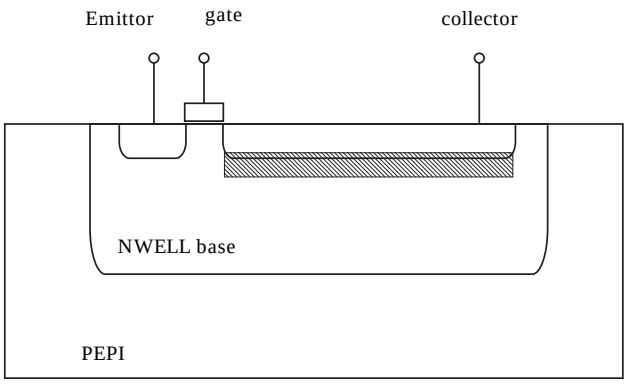


Figure 5.17: Schematic of a MOST used as a bipolar transistor

timal. Therefore we will discuss the exact operation of the gated bipolar for a more optimised device that uses available BCD layers as well.

5.3.2 BCD phototransistor

Device layout

Figure 5.18 shows schematically the final BCD bipolar transistor that was created on the IC. Again the NTUB/PWELL combination is used to provide a larger depletion region of the photodiode (base collector junction). This is now combined with the diffusions and gate of a normal MOST. The base is formed by a NWELL to provide a higher doping level to increase the current gain of the transistor. (see Eqn. (5.7)). Due to the gate, the holes injected from the emittor will have a very short base distance to travel before they reach the PDIFF collector. Thus little recombination current is needed or a large current gain is established. The PDIFF collector is placed over the edges of the NWELL and PWELL to connect the photodiode.

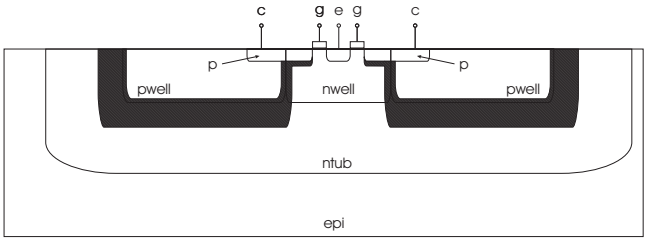


Figure 5.18: BCD bipolar transistor

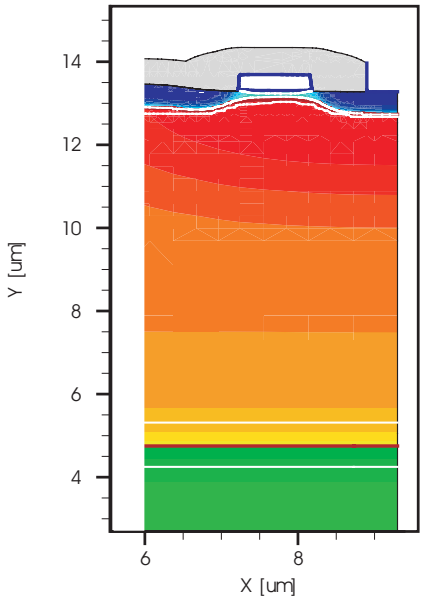


Figure 5.19: Low V_t implant below the gate

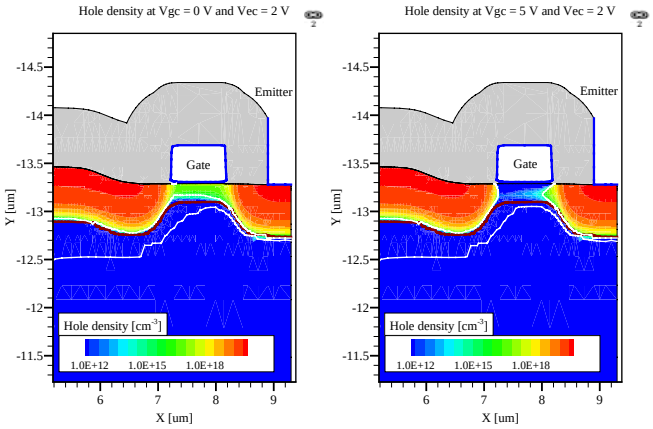


Figure 5.20: Influence of the gate voltage on the hole density in the base

Gate Voltage influence

In first simulations we only used the gate to define the base width. The poly gate itself however was kept floating during simulations. A very high short current between emittor and collector was found. Figure 5.19 shows a detail of the gate of the transistor (gate length = $1\mu m$). The orange color shows the ntype regions, blue color represents ptype. As can be seen below the gate a ptype region shorts the emittor with the collector when the gate floats. This is due to the low V_t implant under the gate. This is a ptype doping that is implanted in the PDIFF active area of the MOST in I2T100 to regulate the V_t of the pMOST. Normally the NWELL bulk of a pMOST is connected to the source, so this is no problem but here the NWELL is floating. Figure 5.20 shows how this can be solved by pulling the gate to the highest voltage in the circuit. The hole density under the gate is shown for a gate of $1\mu m$ at $0V$ and $5V$. At $0V$ basically the channel under the gate is formed as in a normal pMOST. However, when the gate is pulled above the source / emittor of the transistor, the opposite occurs: the low V_t implant is reversed to an ntype region directly under the gate and the short dissapears. In practice it is enough to connect the gate to the emittor of the bipolar transistor, however the

higher the gate voltage, the lower the hole density underneath the gate becomes. As the current gain of the bipolar transistor is higher with a higher doping level of the base, the optimum situation is a higher gate voltage!

Figure 5.21 shows the hole density in the base for different gate lengths. The right side figure shows that for the I^2T100 minimum gate width of $0.7\mu m$ there is still a short leading to large leakage currents. Figure 5.22 shows this: for a gate width of $0.7\mu m$ the leakage current is very large but also the photocurrent gain is much larger due to the small base width. For a gate width of $2\mu m$ on the other hand there is no leakage (as is seen in Fig. 5.21) but also much lower current gain.

Influence of parasitic pnp

As mentioned before there is always a parasitic pnp to the substrate. The base width of this transistor is however very large and therefore a small current gain β is found. For the CMOS phototransistor the NWELL depth is still relatively small, yet for the BCD phototransistor the NTUB is much larger and very little current to the substrate is expected. In I^2T100 we are able to define a BLN underneath the NTUB to block the parasitic pnp completely. This very high doped ntype layer will however not only block the parasitic pnp, but also drastically reduce the depletion layer underneath the NTUB. As this also acts a photodiode, a lower current output is expected with BLN. Figure 5.23 shows the simulated current with and without BLN. Indeed the parasitic pnp towards substrate generates little current, yet with a BLN the substrate current is blocked. On the other hand the loss of the NTUB/PEPI junction severely reduces the emittor current.

5.3.3 Measurements

The measurements results of the photodiode were overshadowed by the problem of the diffusion currents from regions adjacent to the device. The same problem occurs here because of the NTUB/PEPI junction which inserts the diffusion current into the NTUB base pro-

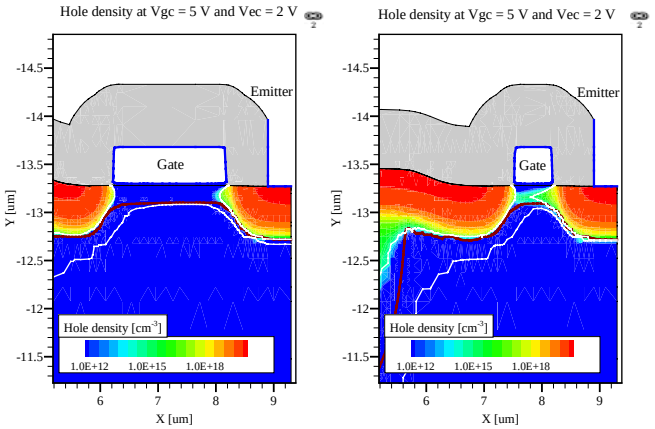


Figure 5.21: Influence of the gate voltage on the hole density in the base for different gate lengths.

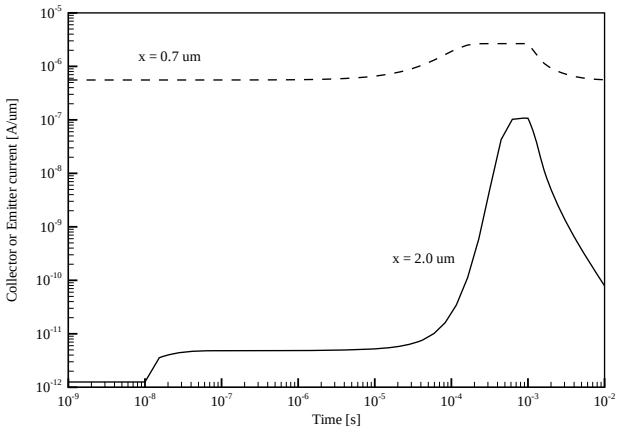


Figure 5.22: Leakage photocurrent for different gate lengths. The V_t implant is not reversed completely for too small gate length!

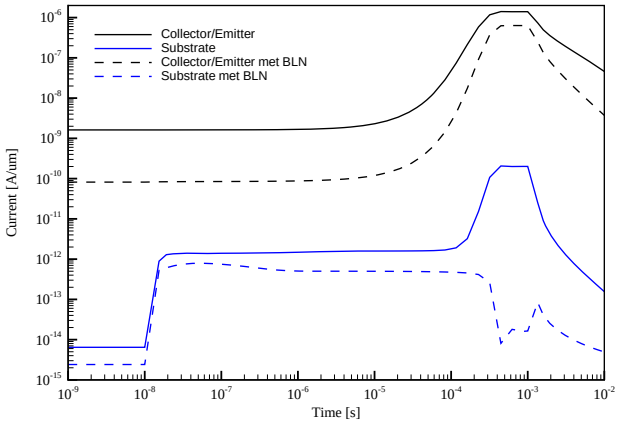


Figure 5.23: Influence of BLN underneath the NTUB for a BCD phototransistor.

viding recombination current. Therefore once more there is need of a good guarding structure to compare the different transistors. However no transistors with such a guarding structure were implemented, making a comparison very hard.

Figure 5.24 shows the behaviour of the BCD phototransistor with a gate of $1\mu m$ and no BLN under the NTUB. The incendent light has a power of $0.78W/m^2$ and a wavelength of $635nm$. The gate was kept at 5V, collector at 0V and the emittor voltage was swept. The graph shows that as long as the base-emittor junction is not forward biased, no bipolar transistor operation is possible. As soon as the base-emittor junction is forward biased, the bipolar transistor will boost the current. When the gate-emittor voltage becomes positive however (last datapoint), a channel forms underneath the gate and normal MOSFET operation takes over.

Figure 5.24 shows the measured influence of a device with and without BLN underneath the NTUB. Red, green and blue incident light was measured. We see that also for the blue light there is still a large difference between the two devices. However the NTUB/PEPI depletion layer is located very deep compared to the penetration depth of the blue light. This shows again the influence of the dif-

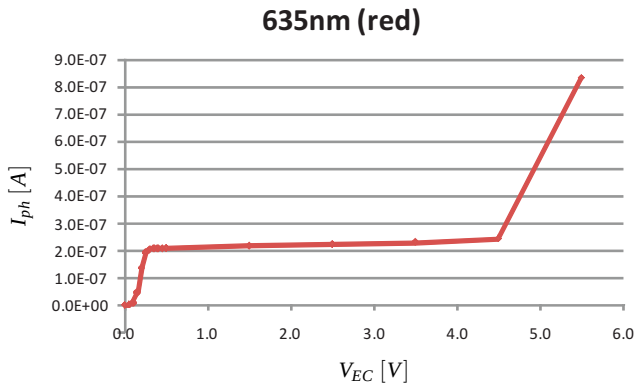


Figure 5.24: Photocurrent vs. V_{EC} of BCD phototransitor with gate=1μm and without BLN. Incident red light (635nm) at 0.78W/m^2.

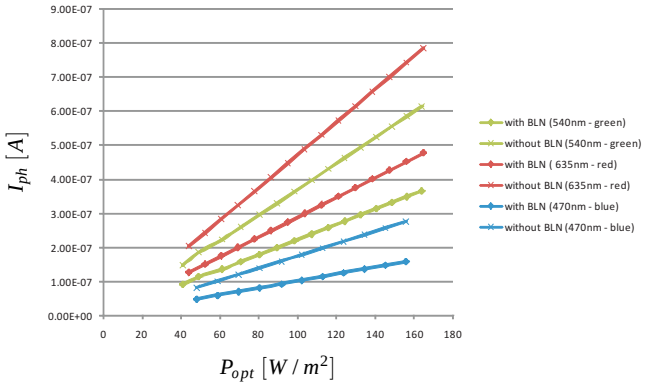


Figure 5.25: Photocurrent of BCD phototransitor with gate=1μm. The crossed datapoints are from a device without BLN, the diamond datapoints from a device with BLN.

fusion currents from the adjacent silicon. As mentioned the BLN blocks the downside of the NTUB from incoming current, making it a boundry against the diffusion currents coming from the substrate.

Figure 5.26 shows the photocurrent of the BCD bipolar transistor with BLN with three different gate lengths: $0.7\mu m$, $1\mu m$ and $2\mu m$ and incident green light. We see clearly that the current gain is as expected larger for a smaller gate lenght. If we calculate the ratios we find:

$$\frac{I_{ph}^{1\mu m}}{I_{ph}^{0.7\mu m}} = 0.865 \neq 0.49$$

$$\frac{I_{ph}^{1\mu m}}{I_{ph}^{2\mu m}} = 2.48 \neq 4$$

The same ratios were found for red and blue light. However from Eqn. (5.7) we expect a square dependency. We believe that the deviation is once more related to the different injection of diffusion currents from the adjacent silicon. As this is different for each device an error occurs. It should be noted that based on the simulations we expected a high leakage / short current for the device with $0.7\mu m$ gate width. The measurements were done with gate at 5V and emittor at 2.5V and as seen in Fig. 5.26 this appears not to be the case in reality. Figure 5.27 shows a measurement but with the copper foil placed over the IC. This time red light is incident but we see much smaller photocurrents than in Fig. 5.26. Calculating the ratios between the photocurrents now gives much better results.

$$\frac{I_{ph}^{1\mu m}}{I_{ph}^{0.7\mu m}} = 0.46 \approx 0.49$$

$$\frac{I_{ph}^{1\mu m}}{I_{ph}^{2\mu m}} = 3.8 \approx 4$$

Though the same remarks as for the photodiodes concerning diffusion currents are valid here, Fig. **??** gives a maximum for the photocurrent. For $100\mu W/cm^2$ we find a maximum of 60nA for red incident light. This corresponds to only $6A/W$, which is rather small.

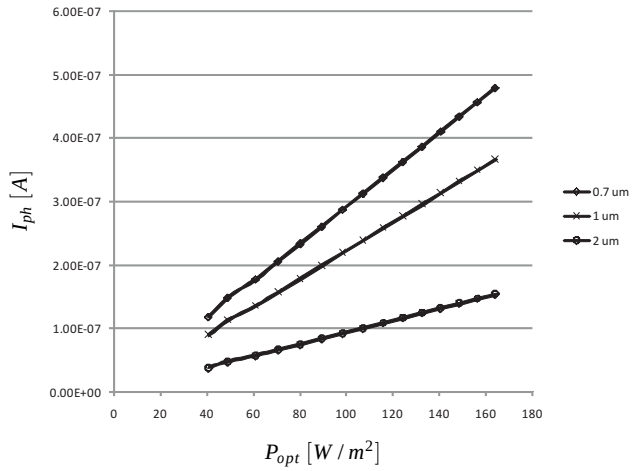


Figure 5.26: Photocurrent of the BCD phototransistor with BLN for different gate lengths for green incident light (540nm).

However it must be noted that these devices have a BLN underneath, basically blocking the very large NTUB / PEPI depletion layer.

Figure 5.28 shows the current that can be expected without BLN but with a copper foil blocking (most of) the diffusion currents. For red light at $100\mu W/cm^2$ we find 232nA, corresponding to a much larger value of $23.2A/W$, though it is uncertain how much influence the adjacent silicon has. [41] however mentiones a lateral phototransistor with $202A/W$ reponsivity. [**?**] also mentions much higher responsivities for smaller devices ($24\mu m$x$24\mu m$) up to $1040A/W$! A $1.2\mu m$ base width is compared to a $0.8\mu m$ gate width of a CMOS phototransistor. However the $1.2\mu m$ device has much higher responsivity, without any explanation. Keeping the above simulations and measurements into mind, we suspect the diffusion currents from adjacent silicon provide the answer and actual responsivity might be many times smaller. We however found no papers in literature regarding this measurement problem we occured.

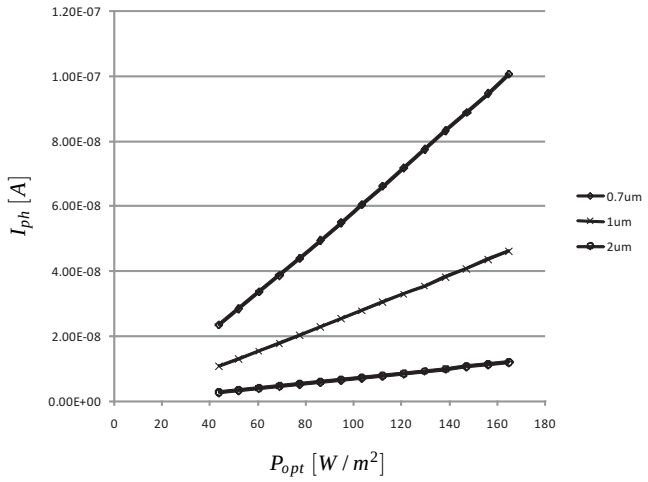


Figure 5.27: Photocurrent of the BCD phototransistor with BLN for different gate lengths for red incident light (635nm). The rest of the IC is covered with a copper foil to block the incident light.

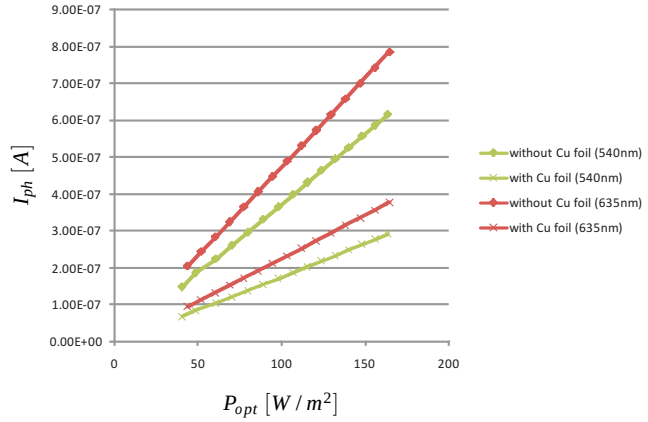


Figure 5.28: Photocurrent of the BCD phototransistor without BLN and $1\mu m$ gate. Both with and without copper foil covering the IC.

6
Circuit Design

In Chapt. 3 the optical feedback circuit was discussed and an implementation was presented on a building block level. In Chapt. 4 this was integrated in the overall driver IC's architecture. With the high level description given, the last two chapters give look closer to the actual silicon implementation. Chapter 5 showed how photodiodes and phototransistors can be integrated in I^2T100 and this chapter will focus on the optical feedback circuit. The purpose of this work however is to determine the feasability of the integrated optical feedback, identify the constraints that are important for an integrated silicon implementation and give a proof of concept. For such a proof of concept and for testing purposes it is not necessary nor possible to implement all blocks presented in the driver architecture of Fig. 4.1.

The main design focus was a proof of concept for the OFC[1], including the DAC, with integrated optical detector. In this chapter the most important circuit implementations on a driver IC prototype will be discussed. Obvious implementations such as digital control

[1] Optical Feedback Circuit

logic, interfacing, counters, ... are not discussed.

Section 6.2 will discuss more profoundly the implementation of an exponential voltage DAC to reduce the necessary DAC resolution. For expample the influence of offsets and gain errors will be discussed. In section 6.3 we will take a closer look to the optical feedback loop implementation and some of the problems encountered. Finally section 6.4 discusses the measurement results from the test IC.

6.1 Test IC parameters

Table 6.1 shows the parameter set that was chosen to the design the proof of concept IC. Though previous chapters gave an in depth description of PWM based optical feedback also for high end displays, we reduced the specifications for our test design to have a more realistic design effort.

We designed a feedback loop with 4 bit perceptual grayscaling in mind for a $1000cd/m^2$ display. Based upon the equations from previous chapters a PWM resolution of 9 bit and 11 bit sampling resolution are required. The feedback circuit was designed for a variation factor $\beta = 6$. This leads to a 12 bit linear DAC or a 10 bit exponential DAC.

The maximum allowed ALRR $\alpha = 1e^{-3}$ is very small. To have a feasable design we chose $\Delta i_a = 250pA$, resulting in a minimum photocurrent $I^0_{pix} \cdot \gamma = 250nA$ before ageing and a maximum photocurrent of $1.5\mu A$.

The capacitance needed for the measurement can easily be found:

$$C = \frac{\left(I^0_{pix} \cdot \gamma \cdot \beta\right)\left(\frac{T_m}{\gamma}\right)}{V_{max}} \tag{6.1}$$

We chose $V_{max} = 3V$ to have a large stepsize for he DAC. T_m is the measurement time and for a pixel the resulting pulse width before ageing should of course be T_m/γ to allow an extention of the duty cycle by a factor $\gamma = 3$ when ageing occurs. As seen in equation 6.1,

the needed capacitance can be scaled down by reducing the measurement time but this also increases the necessary bandwidth of the integrator. With $T_m = T_{frame}$ the required minimum capacitance is $C = 2.7nF$ which is clearly not integratable in the IC. Reducing the measurement time to $T_m = T_{sfr}$ would result in $C = 5pF$ which is perfectly integratable. On the other hand such a small capacitance will be more sensitive to charge injection and leakage currents, so it is in our best interest to have a higher C. Table 6.1 shows two sets of parameters for the feedback loop that were implemented: one with integrated capacitor and one with an added external capacitor. It should be noted that the measurement time was chosen with the sampling clock in mind. An external clock signal of 12 MHz was used which gives an upper boundry for the sampling clock and allows a minimum measurement time of $16/3 \cdot T_{sfr}$. We chose a sampling time of $8 \cdot T_{sfr}$ and the resulting capacitance is $42pF$ which is easily integratable on chip. The pins of this capacitor were also available externally and extra capacitance could be placed in parallel. We also did measurements with an added external capacitor of $220pF$, making a total capacitance of $262pF$ and a measurement time of $48 \cdot T_{sfr}$.

6.2 Voltage DAC design

6.2.1 Linear DAC

In Sect. 3.3.6 we already briefly showed that for larger β it is interesting to use an exponential amplifier. In the used equations an ideal linear DAC and an ideal exponential amplifier were assumed. However in a circuit implementation offset errors and gain errors will occur and their influence has to be taken into account. Without going into detail about their origin yet, generally the output of a linear DAC can be written as:

$$\hat{V} = V_\varepsilon + \Delta v \cdot (1 \pm \rho) \cdot \sum_{i=0}^{n-1} b_i 2^i \tag{6.2}$$

Table 6.1: Proof of concept IC design parameters

Parameter	Value	Explanation
NOB_{gr}	4	4 bit perceptual, 15 grayscales
NOB_{PWM}	9	required PWM resolution
NOB_S	11	sampling resolution
γ	3	overdrive factor
β	6	
α	$1e^{-3}$	$\Delta i_a = \alpha \cdot I^0_{pix}\gamma = 250pA$ $I^0_{pix} \cdot \gamma = 250nA$
$dt_{fr,\max}$	$170ns$	allowed $(t_{fall} - t_{rise})$
T_{sfr}	$32\mu s$	31.25 kHz
T_{frame}	$(2^9-1)T_{sfr}$	61 Hz refresh rate
	External Capacitor	
T_m	$48 \cdot T_{sfr}$	
f_S	1.333 MHz	$2^{11} / T_m = 12MHz/9$
C	$262nF$	
	Integrated Capacitor	
T_m	$8 \cdot T_{sfr}$	
f_S	8 MHz	$2^{11} / T_m = 12MHz \cdot 3/2$
C	$42pF$	

In this we assume a monotonic DAC with adequate INL[2] and DNL[3]. An offset $V_\varepsilon = \varepsilon \cdot V_{\min}$ and a gain error ρ are introduced. To obtain a correct duty cycle the charging voltage $\left(\hat{V} - V_{comp}\right) \in [V_{\min}, V_{\max}]$. Therefore following conditions should apply:

$$|V_\varepsilon| \leq V_{\min} \tag{6.3}$$

$$-|V_\varepsilon| + \Delta v \cdot (1-\rho) \cdot (2^n - 1) \geq V_{\max} = \beta \cdot V_{\min} \tag{6.4}$$

$$\Rightarrow \Delta V_{\min} = \Delta v \cdot (1-\rho) \geq \frac{(\beta + \varepsilon)\, V_{\min}}{(2^t - 1)} \tag{6.5}$$

Equation (6.5) specifies for a certain $NOB_V = t$ the minimum Δv needed to span the entire $[V_{\min}, V_{\max}]$ range.

On the other hand the digital to analog conversion finite resolution introduces an error. The ideal charging voltage V^* will be as closely matched by $\hat{V}$. However on $\hat{V}$ a noise error of 1/2 LSB can occur randomly. In Fig. 6.1(a) and (b) we try to illustrate this. At calibration a voltage $\hat{V}_i^*$ is chose so $V^* \in]\hat{V}_i^* + \Delta V/2, \hat{V}_i^* + \Delta V/2[$. For example in Fig. 6.1(a) the round dot represents the ideal charging voltage V^*. During calibration $\hat{V}_i$, the actual output value of DAC value i, might be the maximum ($= \hat{V}^* + \Delta V/2$). A second measurement (necessary to determine the best DAC value for the pixel) with increased DAC value to i+1 might give the maximum output $\hat{V_{i+1}}$ and therefore we will choose value i as the best DAC value at calibration. This is shown by the middle round dot in Fig. 6.1(a).

After some time an update measurement will be performed and the capacitor will be charged again by the DAC. However the actual DAC voltage $\hat{V}_i \in]\hat{V}_i^* - \Delta V/2, \hat{V}_i^* + \Delta V/2[$. Therefore an underestimate of maximum $3/2\Delta V$ can occur. Similarly Fig. 6.1(b) shows an overestimate of $3/2\Delta V$.

To find the maximum ΔV for uniform grayscaling we demand:

$$\Delta L_V < 1JND - \Delta L_S - \Delta L_{r,f} - \Delta L_{\Delta i_a} \tag{6.6}$$

Comparing the above equation with 3.50, the (very small) second order term was omitted to simplify the equations. With the above

[2]Integral Non-Linearity
[3]Differential Non-Linearity

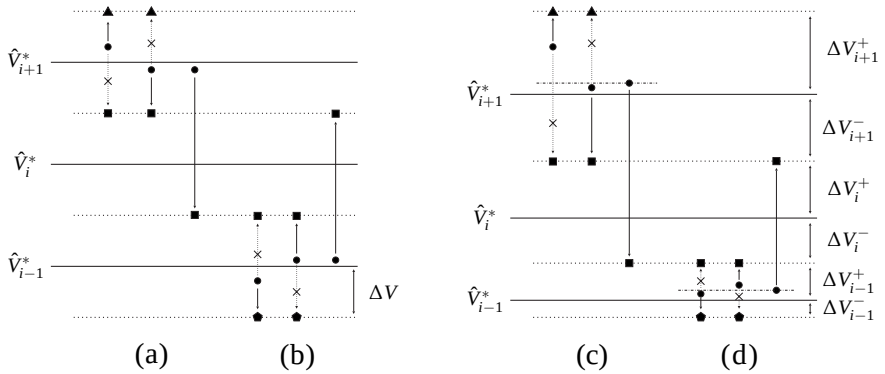


Figure 6.1: Errors for a linear and exponential DAC with finite resolution

reasoning and Eqn. (3.50) we find:

$$(L_{PWM}(k) - L_{\min}) \cdot \frac{3\Delta V}{2V^*} < L_{PWM}(k) \frac{3\Delta V}{2V^*}$$

$$< 1\ JND - \Delta L_S - \Delta L_{r,f} - \Delta L_{\Delta i_a} < d \cdot L_{PWM}(k) \tag{6.7}$$

Figure 6.2 shows the allowed relative error $\Delta L_V / L_{PWM}(k)$ with the different types of errors taken into account. The values used for these errors are found in Table **??**. We see that higher graylevels are determinative for the allowed relative error. Eqn. (6.7) leads to:

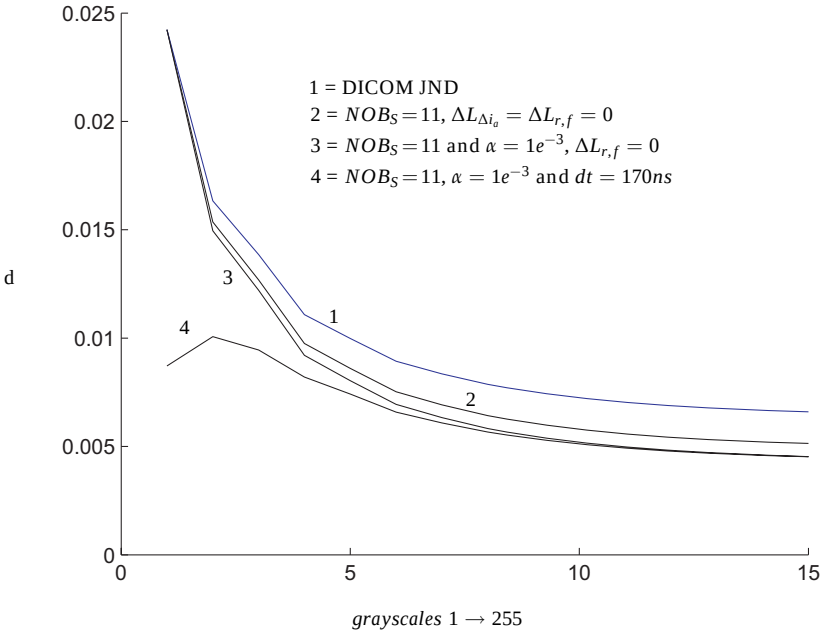
$$\frac{3\Delta V}{2V^*} \leq d \Rightarrow \Delta v(1+\rho) \leq \frac{2d}{3} \cdot V_{\min} \tag{6.8}$$

This "error condition" sets an upper boundry for Δv.

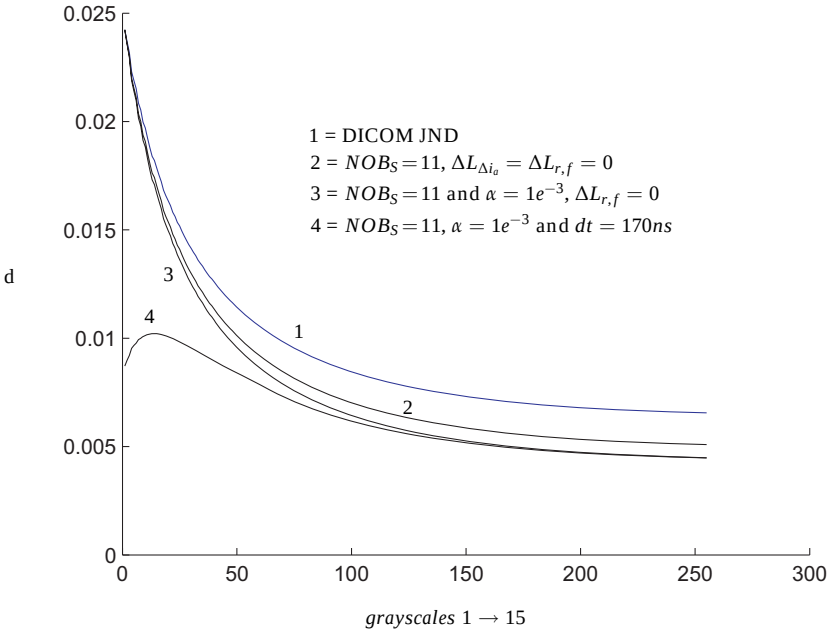
Combining the "error condition" with the "range condition" given by Eqn. (6.5), lets us define a minimal NOB_V t:

$$NOB_V = t \geq \log_2 \left[\frac{3}{2} \left(\frac{1+\rho}{1-\rho} \right) \left(\frac{\beta+\varepsilon}{d} \right) + 1 \right] \tag{6.9}$$

Typically for a 5V CMOS technology opamp offset is up to 10mV. This simply adds linearly to the required range of the DAC as we need to be able to compensate for it. Thus the linear DAC is rather



(a)



(b)

Figure 6.2: Allowed relative DAC error d for (a) a 1000/4/9 display and (b) a 1000/8/14 display. The different graphs show the allowed relative error with different error-contributions taken into account.

unsensitive to offset. The gain error ρ works directly on the stepsize Δv and therefore obviously the NOB_V rises $\approx$ proportionally with ρ. Unfortunatly the gain error is a result of technology variations and can easily be up to 10%.

With the NOB_V defined, we can use the highest possible Δv for our DAC as this gives the easiest design. However there is another upper boundry for Δv from an implementation point of view: Δv should be large enough to span the entire range (see Eqn. (6.4)), small enough so the induced error is small, yet with a certain $NOB_V = t$ the maximum voltage should be low enough for the DAC output stage to remain linear. For a typical opamp class AB output stage this yields:

$$V_\varepsilon + \Delta v\,(1+\rho)\left(2^t - 1\right) \leq V_{dd} - V_{DS,sat} \tag{6.10}$$

Typically the condition following from from Eqn. (6.10) gives a much more stringent upper boundry for Δv than the error condition (Eqn. (6.8)).

6.2.2 Exponential DAC

As mentioned Eqn. (6.7) shows that introducing an exponential amplifier can decrease the required DAC resolution. In stead of a direct linear adjustment of V, a linear signal can be feeded into an exponential gain stage, resulting in a linear to exponential conversion.

Again we will take the possible multiplicative and additive errors into account: a general offset $V_\varepsilon = \varepsilon V_{\min}$ and general gain error κ, but also offset η and gain error α for the linear input voltage of the exponential gain stage. We thus implemented an exponential DAC where the output voltage $\hat{V}$ is given by:

$$\hat{V} = D \cdot (1 \pm \kappa) \cdot e^{\pm\eta - \Delta(1\pm\rho)\sum_{i=0}^{n-1} b_i 2^i} \pm V_\varepsilon \tag{6.11}$$

D is the required exponential amplifier gain to have the correct output voltages. It should be noted that the exponential gain stage that was designed is "inverting", meaning that a higher (linear) input voltage will lead to a lower (exponential) output voltage.

In order to span the entire range of the charging voltage, we find a lower boundary for Δ:

$$\begin{aligned} & D \cdot (1 \pm \kappa) \cdot e^{\pm\eta} \cdot e^{-\Delta(1\pm\rho)\left(2^t-1\right)} \pm V_\varepsilon \leq V_{\min} \\ & \Rightarrow D \cdot (1+\kappa) \cdot e^{\eta} \cdot e^{-\Delta(1-\rho)\left(2^t-1\right)} \leq (1-\varepsilon)\, V_{\min} \end{aligned} \tag{6.12}$$

$$\begin{aligned} & D \cdot (1 \pm \kappa) \cdot e^{\pm\eta} \pm V_\varepsilon \geq V_{\max} \\ & \Rightarrow D \cdot (1-\kappa) \cdot e^{-\eta} \geq (\beta+\varepsilon)\, V_{\min} \end{aligned} \tag{6.13}$$

From Eqn. (6.12) and (6.13) a minimum value for Δ can be derived so $\hat{V}$ will span the entire necessary range:

$$\Delta \geq \frac{\ln\left(\left(\frac{\beta+\varepsilon}{1-\varepsilon}\right)\left(\frac{1+\kappa}{1-\kappa}\right)\right) + 2\eta}{(1-\rho)\left(2^t-1\right)} \tag{6.14}$$

Once again a finite resolution of the DAC leads to an error ΔL_V. Due to the exponential amplifier however, the calculation of the maximum error is slightly more complicated. Figure 6.1(c) and (d) illustrate the differences between the DAC output levels. For linear DAC driving the exponential amplifier the possible deviation of 1/2 LSB = $\Delta/2$ is also exponentially scaled. On the other hand, when calibrating, the absolute deviation to the ideal output is measured. Therefore for a certain choise of DAC output $\hat{V}_i^*$ the ideal charging voltage V^* obeys:

$$\hat{V}_i^* - \Delta V_i^- - \frac{\Delta V_{i-1}^+ + \Delta V_{i-1}^-}{2} \leq V^* \leq \hat{V}_i^* + \Delta V_i^+ + \frac{\Delta V_{i+1}^+ + \Delta V_{i+1}^-}{2} \tag{6.15}$$

Therefore for the maximum underestimate happens when

$$V^* = \hat{V}_i^* + \Delta V_i^+ + \frac{\Delta V_{i+1}^+ + \Delta V_{i+1}^-}{2} \tag{6.16}$$

and is given by

$$\Delta V_{under} \leq \Delta V_i^- + \Delta V_i^+ + \frac{\Delta V_{i+1}^+ + \Delta V_{i+1}^-}{2} \tag{6.17}$$

With Eqn. (6.11) and (6.16) the underestimate error results to:

$$\Delta V_{under} \leq V^* \left(1 \mp \varepsilon\right) \frac{\left(e^{\Delta(1\pm\rho)} - 1\right)\left(e^{\Delta(1\pm\rho)} + 2\right)}{e^{\Delta(1\pm\rho)}\left(e^{\Delta(1\pm\rho)} + 1\right)} \tag{6.18}$$

and similarly for the maximum overestimate:

$$V^* = \hat{V}_i^* - \Delta V_i^+ - \frac{\Delta V_{i-1}^+ + \Delta V_{i-1}^-}{2} \tag{6.19}$$

$$\Delta V_{over} = \Delta V_i^+ + \Delta V_i^- + \frac{\Delta V_{i-1}^+ + \Delta V_{i-1}^-}{2} \tag{6.20}$$

which gives:

$$\Delta V_{over} \leq V^* \left(1 \mp \varepsilon\right) \frac{\left(e^{\Delta(1\pm\rho)} - 1\right)\left(2e^{\Delta(1\pm\rho)} + 1\right)}{\left(e^{\Delta(1\pm\rho)} + 1\right)} \tag{6.21}$$

It turns out the relative overestimate error (Fig. 6.1 (d)) is larger than the relative underestimate error (Fig. 6.1 (c)) and therefore we use Eqn. (6.21) to determine an upper boundry for Δ. The total luminance error because of the finite DAC resolution of an exponential DAC is given by:

$$\left(L_{PWM}\left(k\right) - L_{\min}\right) \frac{\Delta V_{over}}{V^*} \leq L_{PWM}\left(k\right) \frac{\Delta V_{over}}{V^*} \tag{6.22}$$

With Eqn. (6.21) this results to:

$$\left(1 + \varepsilon\right)\left(\frac{e^{\Delta(1+\rho)} - 1}{e^{\Delta(1+\rho)} + 1}\right)\left(2e^{\Delta(1+\rho)} + 1\right) \leq d \tag{6.23}$$

$$\Rightarrow \Delta \leq \frac{S\left(\varepsilon, d\right)}{1 + \rho} \tag{6.24}$$

with the worst case sign of the errors used. Eqn. (6.23) has a single real solution given by Eqn. (6.24) $S\left(\varepsilon, d\right)$. Combined with Eqn. (6.14) a constraint for the DAC resolution can be given:

$$NOB_V \geq \log_2 \left[\left(\frac{1+\rho}{1-\rho}\right) \frac{\ln\left(\left(\frac{\beta+\varepsilon}{1-\varepsilon}\right)\left(\frac{1+\kappa}{1-\kappa}\right)\right) + 2\eta}{S\left(\varepsilon, d\right)} + 1\right] \tag{6.25}$$

With Eqn. (6.25) the required NOB_V can be found and with Eqn. (6.24) and (6.14) a maximum Δ can be chosen. Again, in Eqn. (6.25) the gain errors ρ and κ can be up to 10% due to technology variations.

Once more the output voltage should also remain within the dynamic range of the circuit:

$$V_\epsilon + D\,(1+\kappa)\,e^{\eta}\cdot e^{\Delta\cdot(1+\rho)\left(2^t-1\right)} \leq V_{dd} - V_{DS,sat} \tag{6.26}$$

This puts a very stringent condition for the input offset η. From (6.26) and Eqn. (6.13) we find an upper and lower limit:

$$D\cdot e^{\eta} \leq \frac{(V_{dd} - V_{DS,sat} - V_{os})}{1+\kappa} = D_{\max} \tag{6.27}$$

$$D\cdot e^{-\eta} \geq \frac{(\beta+\epsilon)}{1+\kappa} V_{min} = D_{\min} \tag{6.28}$$

Due to the stringent condition from Eqn. (6.26) the allowed input offset η is very small. It is easily seen that it is maximised by chosing

$$D = \sqrt{D_{\max}\cdot D_{\min}} \tag{6.29}$$

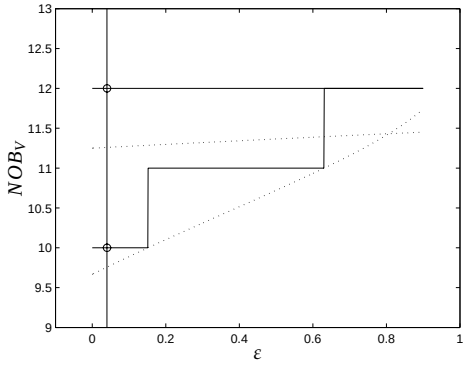
and thus given by:

$$\eta = \ln\left(\sqrt{\frac{D_{\max}}{D_{\min}}}\right) \tag{6.30}$$

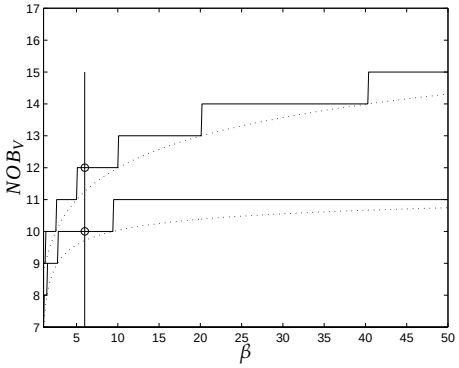
Table 6.2 shows the actual input offset can only be $\approx 250\mu V$, making clear this should be adressed in the design.

6.2.3 Comparison between linear and exponential conversion

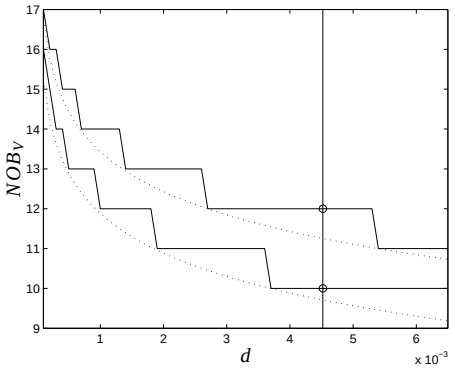
Figures 6.3(a)-(c) give a comparison between a linear adjustment of the charging voltage and an exponential adjustment based on Eqn. (6.9) and (6.25). Figure 6.3(a) shows the dependency of both approaches on the input offset ε. We see that the sensitivity towards ε is higher for an exponential DAC than for a linear DAC. This is easily



(a) Influence of ε with $beta = 6$ and $d = 0.0045$



(b) Influence of β with $\varepsilon = 0.04$ and $d = 0.0045$



(c) Influence of d with $beta = 6$ and $\varepsilon = 0.04$

Figure 6.3: NOB_V required for a linear and exponential DAC. The line that starts lowest is always the exponential approach. Sensitivity towards ε, β and d is plotted.

understood: without any offset $V_{\min}$ is the smallest value to be created. However, when positive offset ($\varepsilon < 1$) occurs $(1-\varepsilon)\,V_{\min}$ is the smallest value to be created. More so, the precision that is required for $V_{\min}$ (see Eqn. (**??**)), must now also be met for $(1+\varepsilon)\,V_{\min}$ in case a negative offset occurs. In case of a linear conversion, the stepsize ΔV remains constant so the offset is merely a very small range extension and doesn't influence the number of bits. In case of an exponential conversion, the stepsize ΔV decreases with a lower value of V. Thus, because of the exponential nature this small range extension requires more steps with decreasing magnitude. That way, the number of bits grows faster. However, as long as β is not too large, $V_{\min}$ is large enough and the influence of ε is neglectible.

Figure 6.3(b) shows the sensitivity towards the measure of pixel to pixel variation β. For lower β it is clearly not advantagious to use an exponential amplifier. For higher inter pixel variations β will be higher and the NOB_V keeps rising for a linear approach, whereas it stays constant for an exponential approach.

The sensitivity towards the other parameters (κ, ρ and η) turns out to be very low in both approaches and does not significantly increase the required NOB_V.

With the design values from Table 6.1, Table 6.2 lists the design specifications for the on chip DAC with exponential amplifier. In comparison a fully linear DAC approach is also given. The maximum allowed relative error is only 0.452% based on the numerical calculations that are also shown in Fig. 6.2. We designed the exponential DAC for gain errors of 10% and a output offset of $20mV$. We see that the stepsize Δv_{lin} for the linear DAC before the exponential amplifier is only $66.875\mu V$, which is rather small. Also the small input offset parameter η results in a very small allowed input offset voltage of only $332\mu V$. This is much lower than typically expected opamp offset and input offset compensation will be required.

Table 6.2: Specifications for an exponential and a linear DAC

	Linear	Exponential	Remarks
NOB_V	12	10	
$V_{charge,\min}$	$499.025mV$	$499.025mV$	
$V_{charge,\max}$	$2.994152V$	$2.994152V$	
V_{OS}^{output}	$20mV$	$20mV$	$\varepsilon = 0.04$
d	0.452%	0.452%	
ρ	0.1	0.1	10% variation allowed on Δv_{lin}
κ	–	0.1	10% variation allowed on D
D	-	$3.42V$	
Δv_{lin}	$839\mu V$	$66.875\mu V$	
V_{OS}^{input}	-	$105\mu V$	$\eta \approx 4.97 \cdot \Delta v_{lin}$
$V_{DAC}^{\min}$	$487.936mV$	$147.002mV$	
$V_{DAC}^{\max}$	$3.8V$	$3.8V$	

6.2.4 DAC circuits

Linear DAC

As mentioned a 10bit linear DAC is needed as a first stage to drive the exponential amplifier. Figure 6.4 shows the linear DAC circuit. The upper half of the circuit shows the reference current circuit and the less significant bits, the lower half the more significant bits and the output stage.

A low bandwidth opamp driving a transistor stage provides a stable reference current by steadying the voltage over a high ohmic resistor. The reference voltage $V_{ref} = V_T$ and is generated by the circuit in Fig. 6.5(b). By chosing $I_{M_{N3}} = 4I_{M_{N2}}$ it is easily shown that $V_{ref} = V_T$.

The reference current is mirrored to each bit-stage. To reduce the DAC's silicon area, the least significant bits use a R-2R network. The currents flowing through these resistors result however in a voltage drop. Therefore the bit-stage current sources should have sufficient output resistance and a cascode stage is used. On the other hand, the common rail of the R-2R network is kept to $V_{ref} = V_T \approx 1V$ and therefore the drain voltage of the cascode transistor should be allowed below V_T. Focussing on the first bit stage shown in Fig. 6.4 it is clear that the lowest possible output voltage $V_{casc,out} = 2V_{DS,sat}$ for both transistors to remain saturated. This means the desired difference between $V_{bias} = V_T + 2V_{DS,sat}$ and $V_{reg} = V_T + V_{DS,sat}$ is only $V_{DS,sat}$. This is done by the left side of the biasing circuit in Fig. 6.5(a). Transistor M_{N4} is diode connected and it's gate-source voltage is the same as the gate-drain voltage of M_{N3}. This means that if M_{N4} conducts, a channel exists at it's source and therefore also a channel will exist at the drain of M_{N3}, forcing it in the triode region. By chosing

$$\left(\frac{W}{L}\right)_{M_{N3}} = \frac{1}{3}\left(\frac{W}{L}\right)_{M_{N4}} \tag{6.31}$$

it can easily be shown that $V_{DS}^{M_{N3}} = V_{DS,sat}$, bringing $V_{b,n2} = V_T + 2V_{DS,sat}$. Transistor M_{N2} is not really necessary to create the desired biasing voltage, yet we used this circuit too for driving cascode current mirrors in opamps. M_{N2} makes sure the drain source voltage of

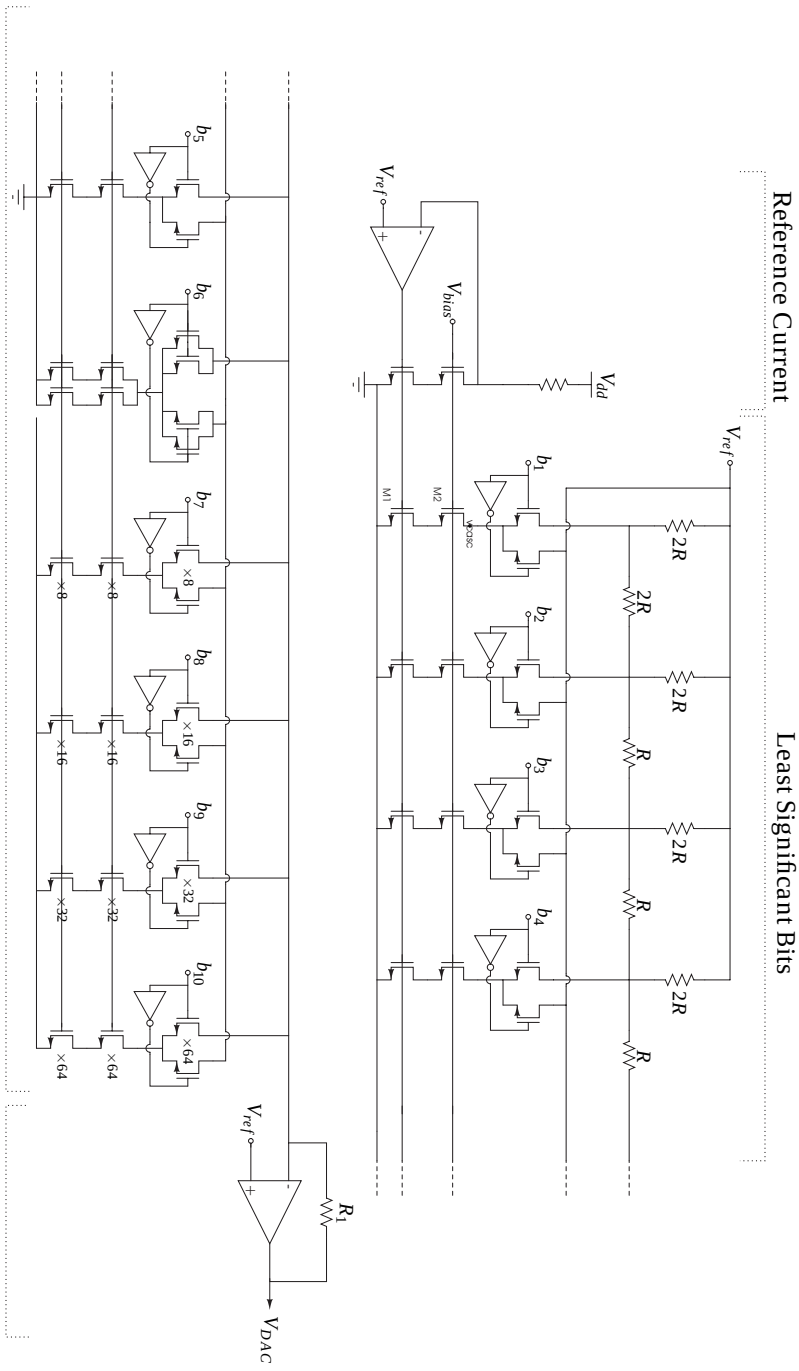


Figure 6.4: Linear voltage DAC schematics. To clarify the schematics bit-wise stages were split in two.

M_{N1} is kept to $V_{DS,sat}$ to reduce the current error when mirroring to M_{N5} and M_{N6}.

On Fig. 6.4 the more significant bits of the linear DAC use scaled current sources where the voltage over the cascode current source is kept to V_{ref} by the output stage. This way the voltage drop over the resistors in the R-2R network remains low enough.

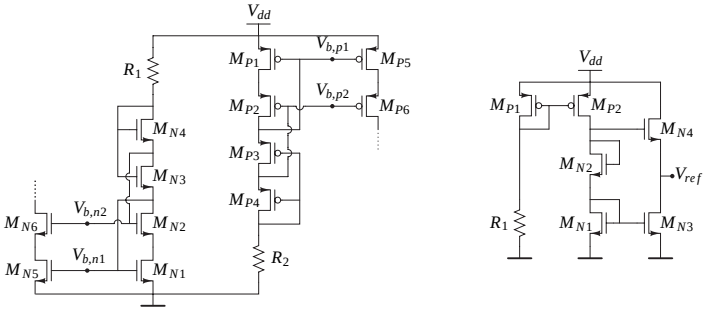


Figure 6.5: Biasing circuit for the DAC.

Figure 6.6 shows the simulated and measured datapoints for the 10 bit linear DAC that is driving the exponential amplifier. As the DAC is only used in a static way, we only did a static measurement. The shown output characteristic is before a scaling and inverting stage to adapt the linear stepsize to the one necessary for the exponential amplification. We clearly see some deviation from the simulated graph.

An important parameter to determine the static behaviour of the DAC is the differential non-linearity error (DNL) given by:

$$DNL_j = \frac{V_j - V_{j-1}}{1LSB} - 1 \tag{6.32}$$

This gives a measure for the difference between two adjacent levels and measures the difference for each step from an ideal step of $1LSB$. A DNL which always remains between $\pm 1LSB$ gives a monotonic DAC with a sufficient low noise level from a static point of view [42]. Figure 6.7 shows the DNL values found for the simulated DAC and the actual measured output characteristics. We see

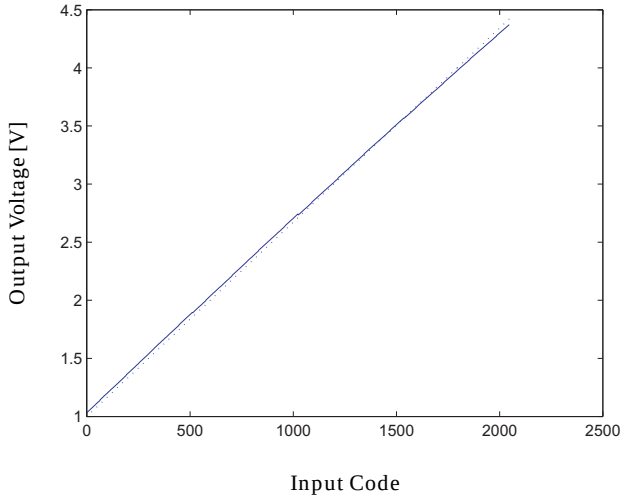


Figure 6.6: Output of the linear DAC. The dotted line represents the simulation data and the solid line the measured datapoints

that the simulated DAC gives a very good result with a maximum DNL of only $0.5\% \cdot LSB$ (upper graph). This simulation was done in transient mode with $20\mu s$ between each consequetive code.

The actual measured DNL graph is given in the lower graph and was measured with a 18 bit ADC from the microcontroller (ADU847) with a much larger sample time of $180ms$ ($\approx 5.5Hz$). As can be seen the DNL error is almost always smaller than $\pm 1/2LSB$, but not at the switching of the more significant bits. With the $5.5Hz$ sampling rate and the fact that the following transitions are again below $\pm 1/2LSB$ in mind, this is probably not a dynamic error.

Figure 6.8 shows another important static characteristic: the integrated non-linearity error (INL) which is given by:

$$INL_j = \frac{V_j - V_j^{fit}}{1LSB} \tag{6.33}$$

It gives a measure for the deviation from a best fitted linear approximation of the output characteristic. If the INL stays within $\pm 1/2LSB$

the DAC stays very close to the ideal fitted curve. As can be seen the designed INL given from simulation data seems very good, with INL below $0.5\% \cdot LSB$. However the large errors on stepsize that occur by changing the more significant bits show on the INL and give a rather large deviation from the $\pm 1/2LSB$ region. What is remarkable is that the INL first increases steadily but then starts to decrease gradually and not only due to the most significant bit changes. Also lower bit stepsize is diminished for larger input codes as the DNL's are constantly lower than $1LSB$ and the INL decreases constantly.

Figure 6.9 shows the schematics of the DAC, but repositioned roughly as they are physically layouted. The reference voltage that is used to construct the reference current is distributed via the thick line. What is important is that this physical metal track is conducting current. Indeed, each bit's current source is either switched towards the output stage or switched towards V_{ref}. This is done to keep the current source in a steady operation point which improved transient response. However, this means the thick V_{ref} track will conduct a current with a magnitude proportional to $((2^{10}-1)$-input code). Input code 0 gives a worst case scenario where all the current is flowing through this metal track. Unfortunately we designed this track minimum width, but very large. This causes a voltage drop and consequently the reference current is too large. When the input code increases the current through the track decreases, causing the reference current to decrease as well: the DNL_i's become smaller and the INL will decrease again. Figure 6.10 shows the INL from a simulation with the added series resistance of the thick track from Fig. 6.9. It shows indeed the INL starts falling more rapidely with increasing input code and overall has a very similar behaviour as the measured INL.

With this discussion of the INL the reason of the"erronous" DNL points is understood. However this is ultimatly not very important from our point of view. The 10 bit linear DAC is only used to drive the exponential DAC and we are only interested in the relative error that is made at the exponential DAC's output between two consecutive output values (see Eqn. 6.22). Therefore let us first describe the exponential amplifier.

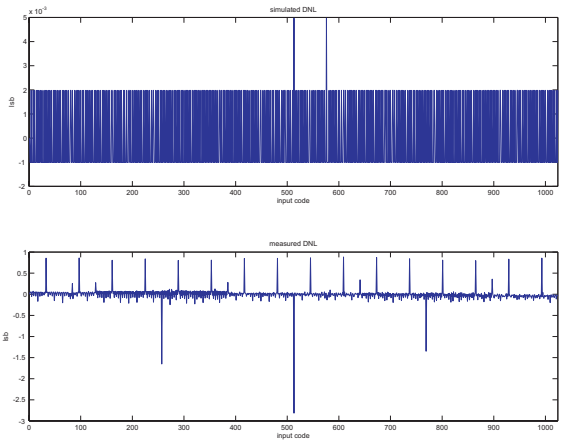


Figure 6.7: DNL from the linear DAC for the simulated data (above) and the measured data (below)

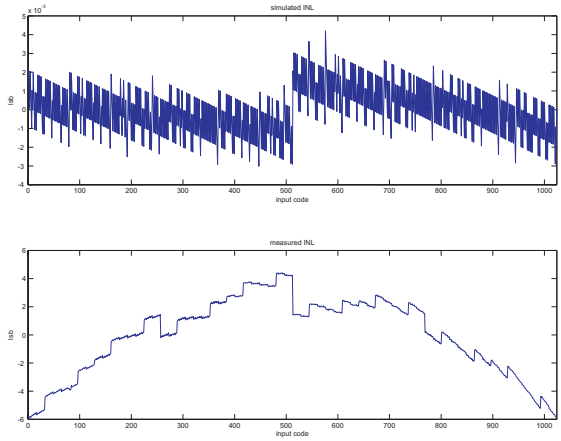


Figure 6.8: INL from the linear DAC for the simulated dat (above) and the measured data (below)

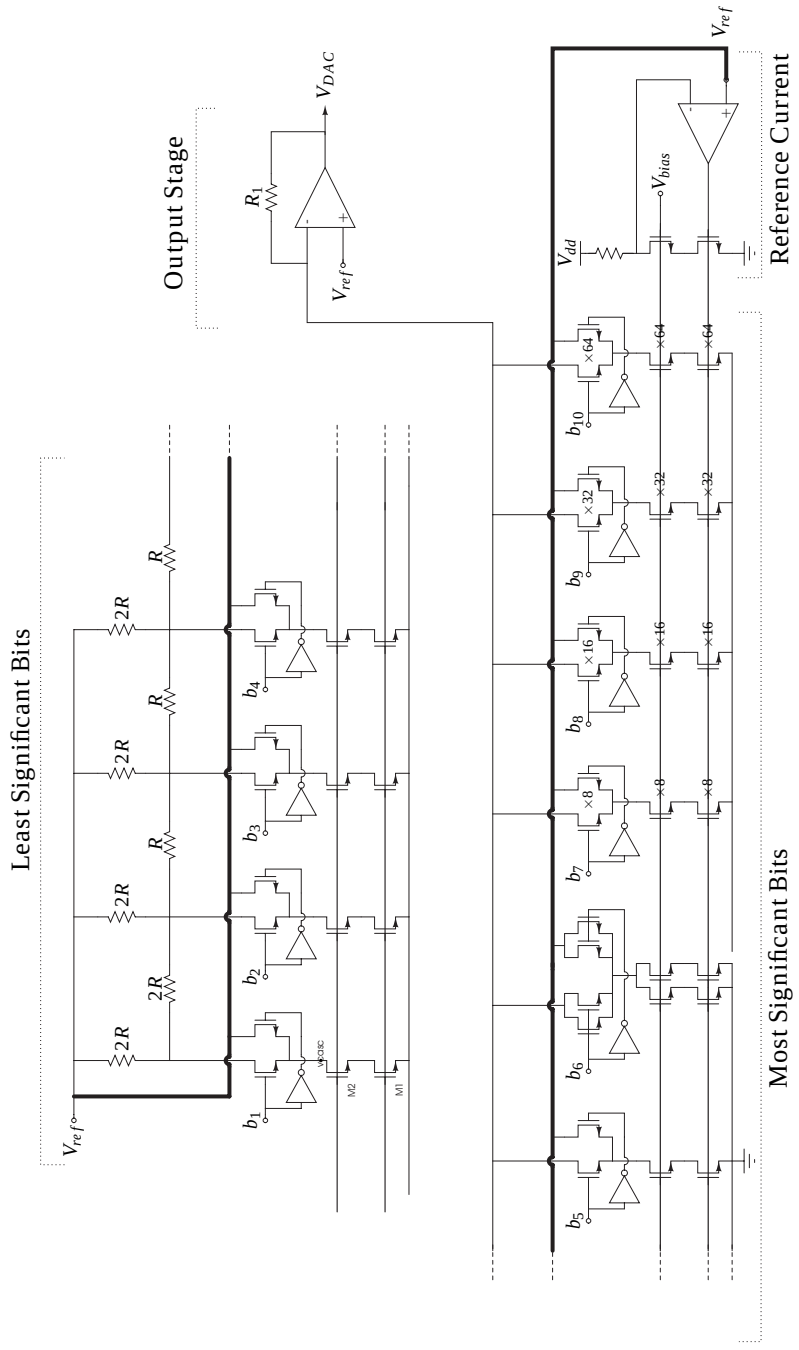


Figure 6.9: Linear voltage DAC schematics "as layouted". The thick line represents the V_{ref} bus that was badly layouted.

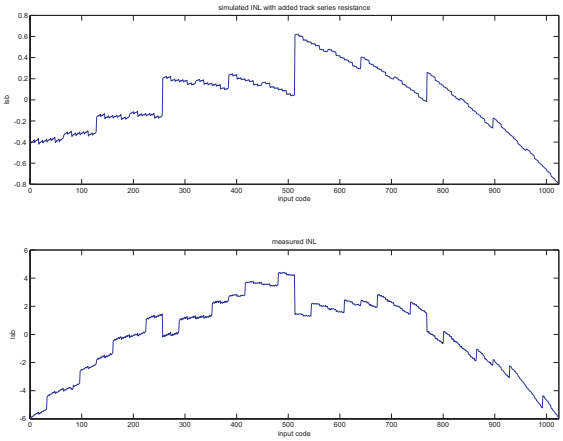


Figure 6.10: INL from the linear DAC for the simulated data (above) and the measured data (below). For the simulated data the series resistance of the metal track towards the reference current source was modelled.

Exponential Amplifier

General description Figure 6.11 shows the circuit of the basic exponential amplifier. The exponential gain is realised by using the exponential dependency of a pnp bipolar transistors current to its V_{be}. I^2T100, the technology used for this test IC, has as a BCD technology a pnp transistor available with the normal parasitic pnp (pdiff-nwell-pepi) to the substrate blocked by a burried layer.

R_1 sets the current through Q_1:

$$I_{R_1} = \frac{V_{ref} \pm V_{os1}}{R_1} = \frac{V_{ref}}{R_1}\left(1 \pm \kappa'\right) = I_s \cdot e^{\frac{V^* - V_{in}}{kT/q}} \tag{6.34}$$

Where V_{os1}, the offset of opamp A_1, leads to a gain error κ'. When both pnp transistors are matched the output voltage V' of A_2 is given by:

$$V' = V_{ref} \pm V_{os2} - R_2 I_c^{Q_2} = V_{ref} \pm V_{os2} - R_2 I_s e^{\frac{V^* - V_{ref}}{kT/q}} \tag{6.35}$$

$$= V_{ref} \pm V_{os2} - \frac{R_2}{R_1} V_{ref}\left(1 \pm \kappa'\right) e^{\frac{V_{in} - V_{ref}}{kT/q}} \tag{6.36}$$

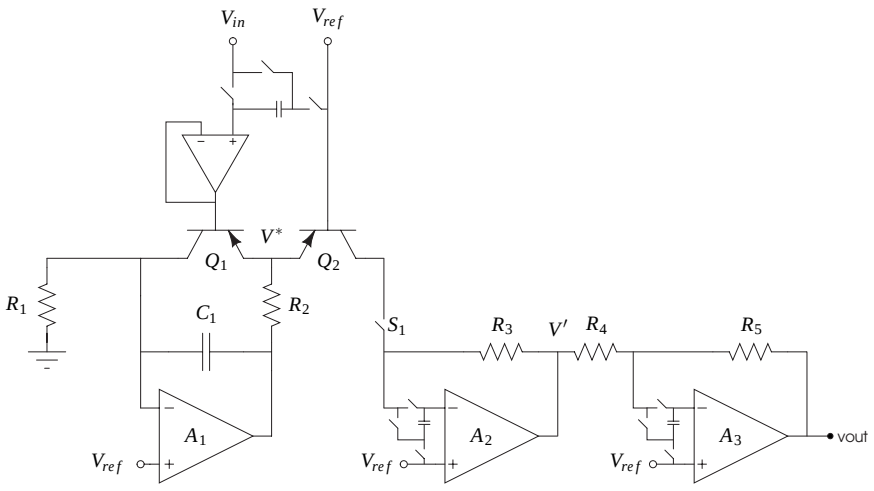


Figure 6.11: Exponential Amplifier

The post amplifier sets the desired gain and with $R_4/R_5 = \eta$ and V_{in} given by Eqn. , the output voltage is given by:

$$V_{out} = V_{ref} \pm (\eta V_{os2} + (1+\eta)\, V_{os3}) + \frac{R_5}{R_4}\frac{R_2}{R_1} V_{ref} \left(1 \pm \kappa'\right) e^{\frac{V_{in}-V_{ref}}{kT/q}} \tag{6.37}$$

As we did not use a differential approach, compensation of the input offset is necessary. This can be done by means of a switched capacitor. The offset is stored on the capacitor C_2 which is then placed in anti-series to the buffer's input. Because of the post amplifier, the offsets V_{os2} and V_{os3} are multiplied as well and can become high. Therefore the same offset compensation technique could be used for A_1 and A_2 as well. On our test IC however, we were able to override these reference voltages externally.

Stability Figure 6.12 shows the AC small signal representation of the feedback loop with A_1 and Q_1 in the feedback path. Without C_1 and R_2 and neglecting r_0 the open loop gain is given by:

$$OLG = -\frac{g_{m1} \cdot R_1}{1 + sR_1\left(C_{par} + C_{in}\right)} \cdot A_1(s) \tag{6.38}$$

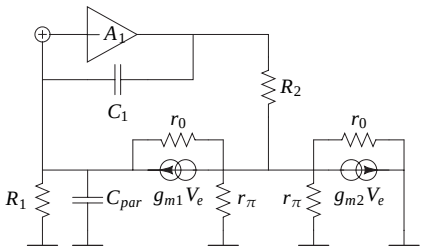


Figure 6.12: AC small signal scheme of exponential amplifier

With g_{m1} found from the DC point we find in the worst case where g_m1 is highest:

$$OLG = -\frac{\overbrace{V_{ref}/\left(kT/q\right)}^{B}}{1+sR_1\left(C_{par}+C_{in}\right)} \cdot A_1(s) \tag{6.39}$$

Here C_{par} is the combination of the opamp imput capacitance and C_{BC} from Q_1. The DC feedback factor $B \approx 40$ is much more than unity gain due to the transistor in the feedback path. Together with phase shift from the parasitic pole at higher frequencies (low C_{par}), this can easily rend the loop unstable. Therefore we added an emitor feedback resistor R_2 to reduce the gain in feedback path and a capacitor C_1 to annihilate the pole. With R_2 and C_1 included (again r_0 and r_π neglected), the open loop gain is given by:

$$\begin{aligned} OLG &= \frac{R_1}{1+\left(g_{m1}+g_{m2}\right)R_2}\frac{g_{m1}+sC_1\left(1+\left(g_{m1}+g_{m2}\right)R_2\right)}{1+sC_{tot}R_1} \\ &\approx \frac{R_1}{mR_2}\frac{1+s\left(mR_2C_1\right)}{1+sR_1C_{tot}} \end{aligned} \tag{6.40}$$

Note that in our application the current through Q_2 will an exponentially scaled down version of the current through Q_1. Therefore $g_{m2} \leq g_{m1}$ and $1 < m < 2$ in the above equation. By chosing $R_2 > R_1$ and $C_1 \gg C_{par}$ we make sure the feedback factor is always smaller than unity gain and the parasitic pole is closely matched by the zero, thus solving stability problems.

Simulations and measurements Figure 6.13(a) shows the exponential amplifier without compensation from C_1 and R_2 yields unstable behaviour. In Fig. 6.13(b) the pole is compensated by the added zero, resulting in a very large phase margin.

Figure 6.14 shows the simulated and measured datapoints for the 10 bit exponential output DAC. As mentioned we were able to regulate the input offset by changing the bias voltage of the second bipolar transistor externally. Good resemblance with the simulated characteristic is percieved.

The most important question is however if the relative error made by the exponential DAC always remains low enough. With Eqn. 6.20:

$$\Delta V_{over} = \Delta V_i^+ + \Delta V_i^- + \frac{\Delta V_{i-1}^+ + \Delta V_{i-1}^-}{2} < V_{i+1} - V_{i-1} \quad (6.41)$$

The condition for the allowed relative error was given by:

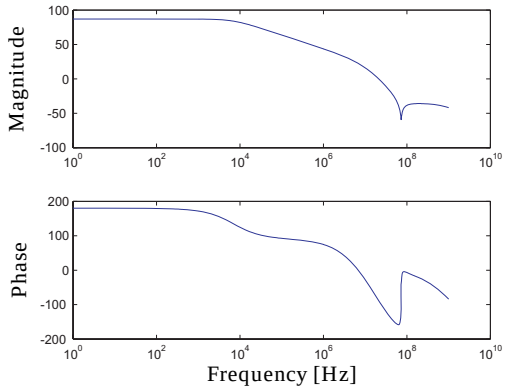
$$\frac{\Delta V_{over}}{V^*} < 0.452\% \quad (6.42)$$

with V^* being the optimal DAC voltage that was needed for the pixel and the boundry of 0.452% was found based on the calculations from previous chapters (see Fig. 6.2). We also started from a parameterized equation for the DAC's output and found a maximum relative error given by:

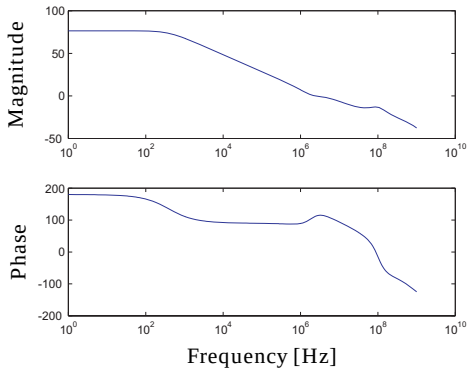
$$(1+\varepsilon)\left(\frac{e^{\Delta(1+\rho)}-1}{e^{\Delta(1+\rho)}+1}\right)\left(2e^{\Delta(1+\rho)}+1\right) \leq d \quad (6.43)$$

To focus the mind: an ideal implementation without any offset ($\varepsilon = 0$) or input gain error ($\rho = 0$) of the DAC that was designed ($\Delta = 66.875\mu V/(kT/q)$) would give a maximum relative error of $0.389\% < 0.452\%$. To quantify the relative error of the simulation and measurement of the exponential DAC, we will examine an overestimate of the error by plotting

$$Error_i = \frac{V_{i+1} - V_{i-1}}{V_{i-1}} \quad (6.44)$$



(a) AC behaviour of the exponential amplifier without compensation



(b) AC behaviour of the exponential amplifier with compensation

Figure 6.13: Exponential amplifier AC behaviour

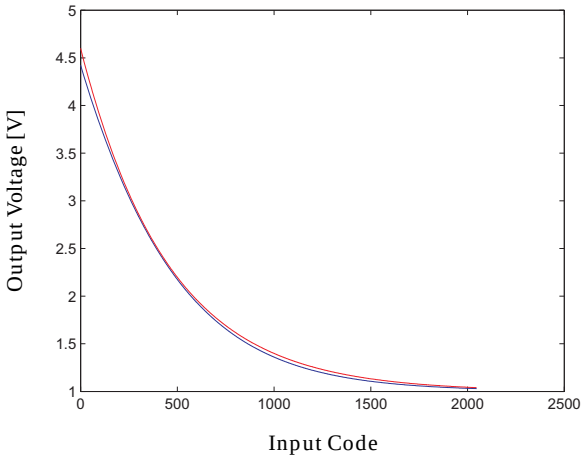


Figure 6.14: Output characteristic of the exponential DAC

because we have no actual measured information on $\Delta V_i^+, \Delta V_i^-, \ldots$ as shown in Fig. 6.1 and only the measured values can be used. Fig. 6.15 shows this relative error compared to the same calculations for an ideally designed output characteristic with:

$$V_{out}^{ideal} = 1V + 3.42V \cdot e^{\frac{-66.875\mu V}{\frac{kT}{q}} \cdot \sum_{i=0}^{n} b_i \cdot 2^i} \tag{6.45}$$

Also indicated is the upper boundry of 0.452% as defined in Table 6.2. Figure 6.15 shows the simulated output both without (a) and with (b) added series resistance as mentioned above and (c) the actual output measurement. We see that the relative error never exceeds the allowed error boundry.

6.3 Optical Feedback Circuit

6.3.1 General description

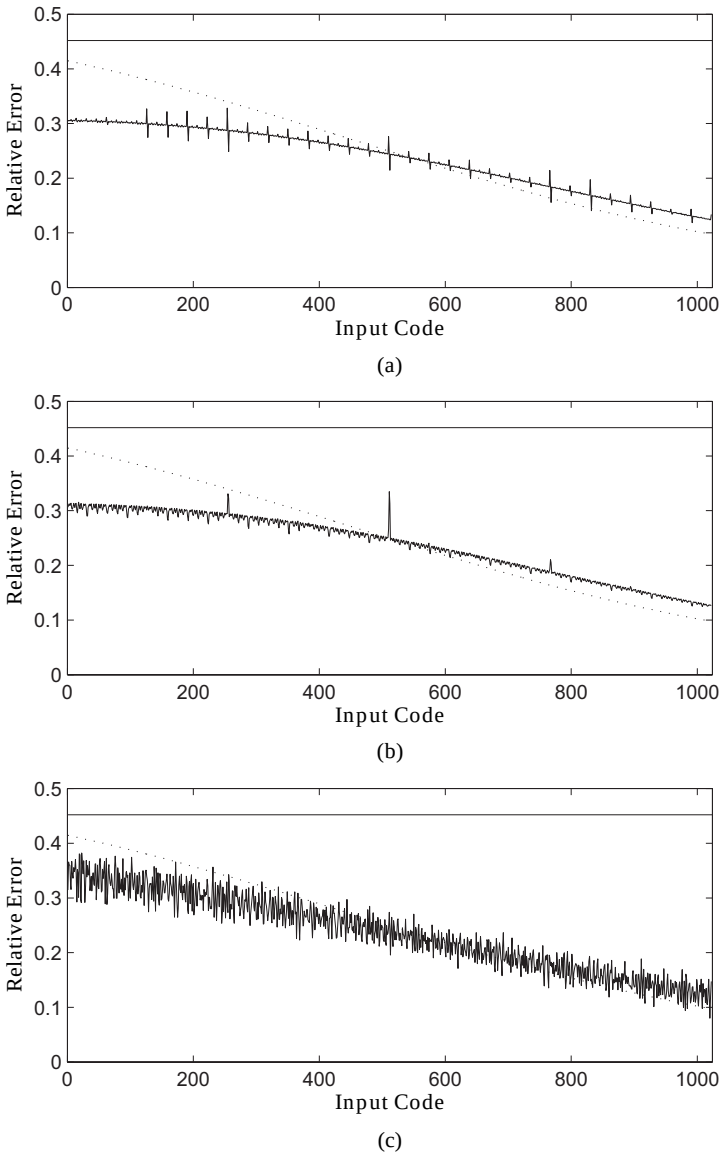


Figure 6.15: Relative error for the exponential DAC. The relative error for the ideal characteristic is always plotted in dashed line and compared to (a) the simulated data, (b) the simulated data with added series resistance and (c) the measured data.

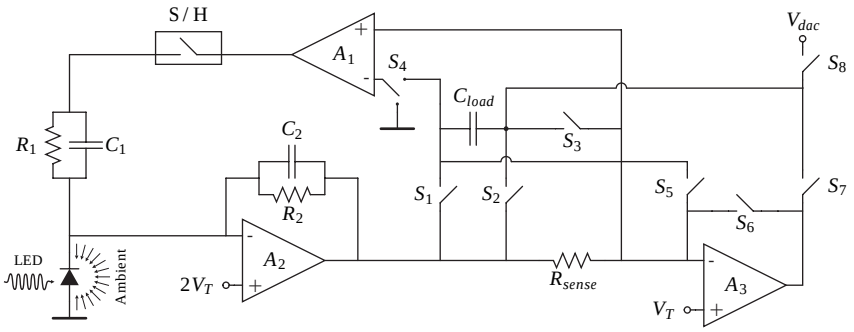


Figure 6.16: Optical feedback circuit

Ambient Light Feedback Figure 6.16 shows the final OFC[4] as implemented on the test IC. This is basically the same circuit as shown in Fig. 3.9 (p.73). The operation of the circuit is shown in figures 6.17(a)-(d).

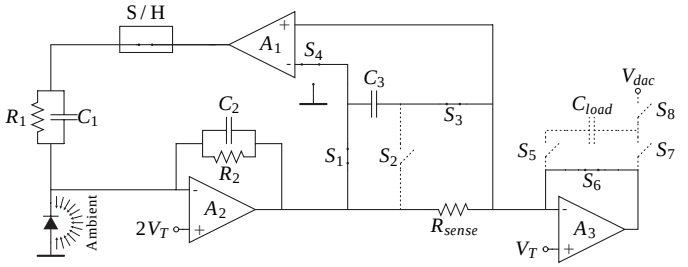
In Fig. 6.17(a) and (b) the first phase of the optical feedback is shown: the ambient light correction. As explained before, the current through R_{sense} is forced to zero by the gain of A_1. Thus, the current through R_1 matches the ambient light photocurrent. Also possible offsets from amplifiers A_2 and A_3 are compenstated for. However, the offset of amplifier A_3 comes directly over the sense resistor, basically nullifying the goal of the feedback loop. Therefore we must compensate for this offset. This is done with capacitor C_3. In Fig. 6.17(a) C_3 is placed parallel with R_{sense}, sampling the voltage over R_{sense}:

$$V_{C_3} = V_{os,A_3} + V_{\pm,A_3} \tag{6.46}$$

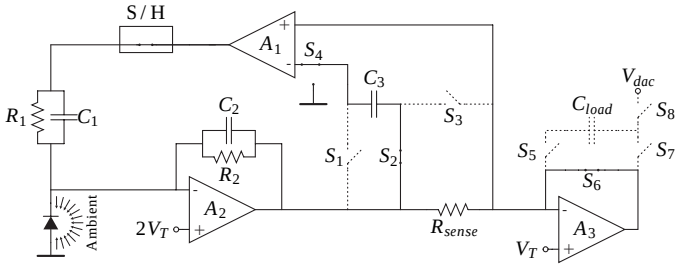
with $V_{\pm}$ the necessary voltage between the inputs of A_3. In Fig. (b) C_3 is placed in anti series with the negative input of A_3, meaning the voltage drop over R_{sense} is ideally compensated for.

However, due to charge injection from the switches, some voltage drop may still occur, resulting in an error current. When the switch transistors are switched, channel charge has to be evacuated

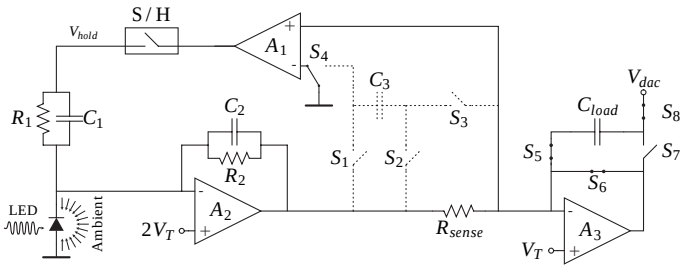
[4] Optical Feedback Circuit



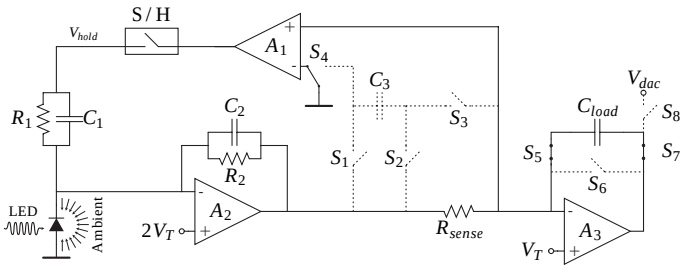
(a)



(b)



(c)



(d)

Figure 6.17: Explenation of the OFC operation principle

and gate-drain and gate-source capacitances need to be charged or discharged. This results in a netto charge ΔQ that is injected or extracted from C_3. Also other leak currents will change C_3's charge. Clearly a higher capacitance C_3 will reduce the resulting voltage drop, yet a large capacitor requires large silicon area. As the charging capacitor C_{load} is a large capacitor and is not yet needed during the ambient light correction, Fig. 6.16 shows how C_{load} can be used as offset compensation capacitor by opening S_5,S_7 and S_8, thus saving a capacitor. In Fig. 6.17(a)-(d) we deliberatly showed a seperate capacitor C_3 for easier explanation.

Sampling and capacitor charging With $V_{s/h}$ generating the adequate current through R_1, the sample and hold circuit will lock down this voltage. The ambient light feedback is no longer needed and C_{load} can now be used as charging capacitor as shown in Fig. 6.17(c). The capacitor is charged with the desired voltage and the pixel is activated not to have any transient behavior when the measurement starts.

Measurement When C_{load} is fully charged, it is used as a precharged integrator with opamp A_2 and discharged by the pixel's photocurrent as shown in Fig. 6.17(d).

6.3.2 Detailed Description

When looking at Fig. 6.16, the photodetector in biased to $2 \cdot V_T$. For a photodiode this increases its efficiency and for a phototransistor tis makes sure the emittor base voltage is always large enough(see Chapter 5). The integrator opamp A_3 on the other hand keeps one side of R_{sense} to V_T. This is to allow a large swing of the capacitor voltage and thus simplifing the DAC design. During ambient light rejection the current through R_{sense} is nullified, meaning over R_2 a voltage drop of V_T will appear and opamp A_2 will have to source a certain current. With $R_{sense} = R_2 = 2M\Omega$ this current is $500nA$. This current must also flow through R_1. We chose R_1 $1M\Omega$, meaning the output of the S/H circuit will be $2.5V$ at least. This leaves room

for $\approx 1.5\mu A$ to compensate for ambient light contribution. As the maximum pixel photocurrent contribution is expected to be $I^0_{pix} \cdot \gamma \cdot \beta_{max} = 1.5\mu A$, meaning a similar ambient light contribution seems realistic.

As mentioned already there are very stringent noise and leakage current demands. In Sect. 3.3.3 we introduced the error current Δi_a and the resulting error on the output energy (see Eqn. (3.50)):

$$\Delta E = \pm E^*_{ph} \frac{\Delta i_a}{I^0_{pix} \gamma a \beta^*} = \pm E^*_{ph} \frac{\alpha}{a\beta^*} \tag{6.47}$$

We showed that the worst case scenario where $\beta^* = 1$ resulted in a very low ALRR[5] $\alpha = 1e^{-3}$. The proof of concept IC was designed for an error current $\Delta i_a = 250pA$. However, the same argumentation as with the voltage DAC can be made: for higher β^* the error current can be larger or the allowed α rises. The major causes for error current are listed below:

switch charge injection For the sample and hold circuit as well for the offset compensation, charge injection from the switches will lead to error currents.

switch leakage currents Finite off state resistance of the switches results in leakage currents.

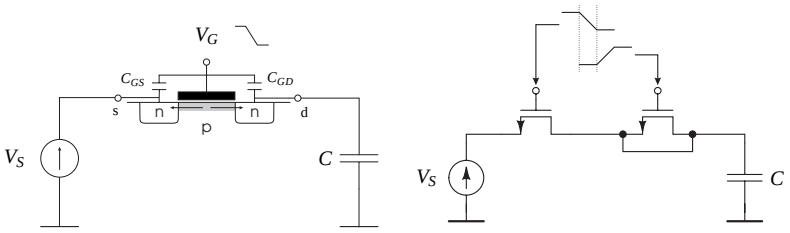
opamp input voltage Finite gain and offsets will result in non-ideal behavior, introducing error currents.

In the next sections we will discuss each of these causes in depth.

Switches and S/H circuit

Charge injection Figure 6.18(a) shows a single n-channel mosfet used as a switch when charging a capacitor, for example C_{load} when used as offset compensation capacitor. In the on-state the nmos is

[5] Ambient Light Rejection Ratio



(a) Nmos switch charges

(b) Dummy transistor charge injection compensation

Figure 6.18: Switch Considerations: (a) charge injection and (b) dummy compensation

used in the linear region with high V_{gs} and very low V_{ds}. Due to the inversion layer there is some charge in the channel of the transistor:

$$Q_{ch} = -C_{ox}WL \cdot \left(V_g - V_s - V_{th}\right) \tag{6.48}$$

Basically this is the charge in the gate-channel capacitance when operating in linear region. Furthermore, there are gate-source and gate-drain overlap capacitances which hold charge as well.

When switching the gate voltage from $V_{G,high}$ to $V_{G,low}$ the change in charge in each overlap capacitor is given by:

$$Q_{OL} = -C_{OL}\left(V_{G,high} - V_{G,low}\right) \tag{6.49}$$

When the transistor is switched off, all this charge has to be evacuated, either to the source side or the drain side where the capacitor is. Clearly the drain side fraction will be inserted in the charging capacitor and thus cause a voltage error.

It is well known[43, 44, 45] that a fast switching clock edge will result in the worst case scenario where the charge reaching the capacitor is maximum and given by:

$$\Delta Q_{cap} = \frac{1}{2}Q_{ch} + Q_{OL}^{GD} \tag{6.50}$$

with Q_{GD}^{OL} resulting from the gate-drain overlap capacitance only. This means maximum half the channel charge is injected and all the

gate-drain charge. A Slower switching clock edge will result in more charge being evacuated to the source side, yet still charge injection occurs.

We used a well known remedy to this charge injection: the placement of a half width dummy transistor which is driven with an inverted clock signal. This is shown in Fig. 6.18(b). As the dummy has only half the width of the switching transistor $C_{ch}^{d} = 1/2C_{OL}^{sw}$. When the switch transistor is switched off with a fast edge, half of it's channel charge reaches the capacitor. However, this is exactly the charge needed in the dummy transistor's channel. Therefore, when switching fast, the channel charge injection is compensated. The same reasoning goes for C_{gd} overlap capacitance charge injection. A half width dummy transistor with source and drain short circuited, $C_{gd}^{d} + C_{gs}^{d} = C_{gd}^{sw}$. In [**?**, 46] it is shown that:

1. the switching clock's edge should be very fast as mentioned above.
2. the dummy transistor should be switched on after V_{gs}^{sw} drops below V_{th} in order to compensate the charge injection regardless of V_s.

To obtain fast switching clock edge, a cascade of several minimum size inverters was used, each one steepening the edge. The delay for the dummy switch is easily added with an inverter with much larger transistors (larger gate capacitance) driving a smaller inverter.

Figure 6.19 shows the charge injection into $C_{load} = 42pF$ during the offset compensation. We simulated using the provided I^2T100 BSIM3 models for Spectre with CAPMOD=2. An offset of $5mV$ was simulated for opamp A_3. As switches single NMOS transistors were used.

The dotted line shows the voltage over C_{load} for uncompensated switches. We see that the switching S_1, S_2 and S_3 have an influence on the charge. The voltage changes $\approx 450\mu V$. As this voltage drop comes over $R_{sense} = 2M\Omega$, this would lead an error current $\approx 250pA$ which is unacceptable. Note that unexpectedly the switching of S_2 and S_3 also results in voltage drops: after S_1 has opened there is no current path anymore to discharge C_{load}. However simulations

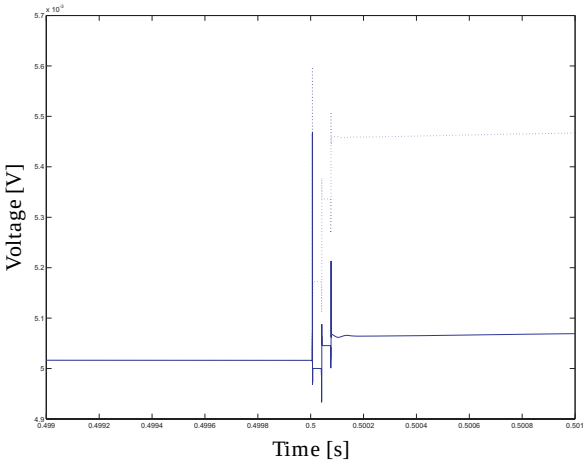


Figure 6.19: Offset compensation with and without dummy transistors for fully integrated loop

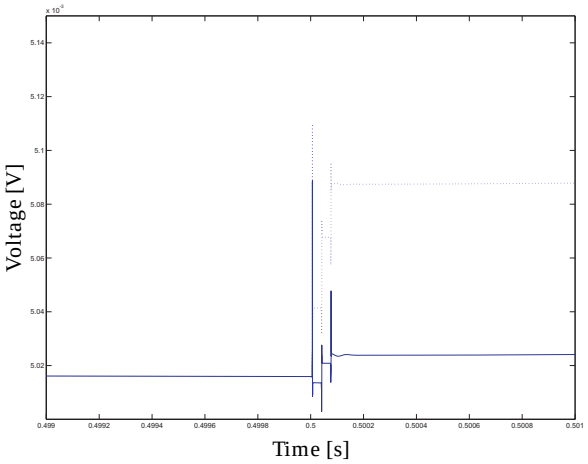


Figure 6.20: Offset compensation without and with dummy transistors for semi integrated loop

showed that over the gate drain capacitance of S_1 this current could still escape. Adding dummy transistors in S_2 and S_3 and tweaking their sizes resulted in optimum behaviour shown with the solid line. The voltage drop is now only $50\mu V$. We simulated for different switching clock edge speeds, all with good result.

For the loop with an added external capacitor the same charge injection will result in roughly 6 times smaller voltage deviation. This is shown in Fig. 6.20. The dotted graph shows the simulated voltage change without dummy transistors which is already acceptably low ($70\mu V$ yields $35pA$). With the dummy transistors, the behaviour is excellent ($8\mu V$ or $4pA$).

Leakage currents The two most important contributions to the leakage current in a (relatively) large channel technology as I^2T100 are drain to well pn junction leakage current and the subtreshold leakage current. Note that there are many other leakage current mechanisms in a MOS device, many of which are related to the gate oxide. However, these contributions only become important for newer, short channel technologies with very thin gate oxide and very high electric field. [47] gives a very good overview.

pn junction leakage current The pn junction existing between drain and well should be inversly biased when the switch is closed to reduce these leakage currents. I^2T100 is a p-epi technology, thus the NMOS pwell (bulk) should be connected to ground at all time. Because all switches in the schematic of Fig. 6.16 have source and drain voltages $\geq V_T$ thus for an NMOS switch the drain-bulk junction is always inversly biased.

For a PMOS switch, the nwell bulk voltage can be freely chosen up to V_{dd}. In normal operation the circuit has no switch drain or source voltages higher then $4V$, thus also for the PMOS switch, pn junction leakage current is minimum.

Subtreshold leakage current When $V_{GS} < V_T$ as is the case when the transistor is switched off, the mosfet works in weak inversion with very little channel. Therefore V_{DS} drops over the drain bulk pn junction and the drift component of the current is

neglectible. The current is diffusion driven and the NMOS can be seen as an npn bipolar transistor. It can be shown[47, 48] that:

$$I_D = \mu C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q}\right)^2 e^{\frac{V_{gs}-V_{th}}{m\frac{kT}{q}}} \cdot \left(1 - e^{\frac{-V_{ds}}{\frac{kT}{q}}}\right) \tag{6.51}$$

with $m \geq 1$ a factor depending on the depletion layer capacitance. As expected an exponential dependance on V_{GS} means the transistor should be switched off with negative V_{GS} if possible. On the other hand, also the drain source voltage V_{ds} is important. Indeed, ideally the subtreshold current can be reduced to 0 with $V_{ds} = 0V$. For $V_{DS} \geq 3\frac{kT}{q}$ the leakage current becomes independent from V_{DS}! However, in general current trough all parasitic resistances between the two nodes the switch is connecting will decrease with smaller V_{DS}.

As mentioned for all switches the source or drain nodes of the switching transistors have $4V \leq V_d, V_s \geq 1V$ and therefore $V_{gs} < -1V$ for NMOS switches when switched off. This results in very small leakage currents.

However during phase 2 (Fig. 6.17(b): ambient light correction with compensation for A_3's offset), leakage currents will reduce / augment the offset compensation charge on C_{load}. This means that the leakage current contribution is "integrated" by C_{load} during phase 2 and it is in our interest to reduce this time (or increase the loop bandwidth). Especially for an integrated capacitor, the allowed leakage is very small. With a measurement time of $0.5ms$ a resulting integrated error current of $50pA < \Delta i_a = 250pA$ gives:

$$42pF \cdot \frac{2M\Omega \cdot 50pA}{0.5ms} = 8.4pA$$

$$262pF \cdot \frac{2M\Omega \cdot 50pA}{0.5ms} = 52.4pA$$

Fig. 6.21 therefore shows the V_{ds} voltages for all switches. As the offset compensation reduces the voltage over R_{sense} to a few μV most (opened) switches only see a few μV as V_{ds} and leakage currents of any kind should be extremely low! Only S_1 has a V_{ds} of a few mV

which is still low enough. Switches S_4 and S_8 as presented in Fig. 6.17(b) would have much higher V_{ds}. Therefore Fig. 6.21 shows how we introduced some changes to reduce the V_{ds} of these switches by simply bringing the drain voltage to V_T. Simulations showed a very stable voltage over C_{load} with leakage currents of $1pA$.

However it is quite important to mention that we found out only after production of the IC that MOS subthreshold behaviour is not modelled correctly in the I2T100 design kit, so simulation data is of little value here.

Note that during actual discharge of the capacitor, leakage currents through switches S_1 and S_6 and the series of S_3 and S_5 are contributing to the current towards C_{load} (see Fig. 6.17(d)). V_{ds} over these switches will now be much higher than a few mV's because C_{load} is charged with V_{DAC}. However this contribution is not integrated over time and therefore remains sufficiently low.

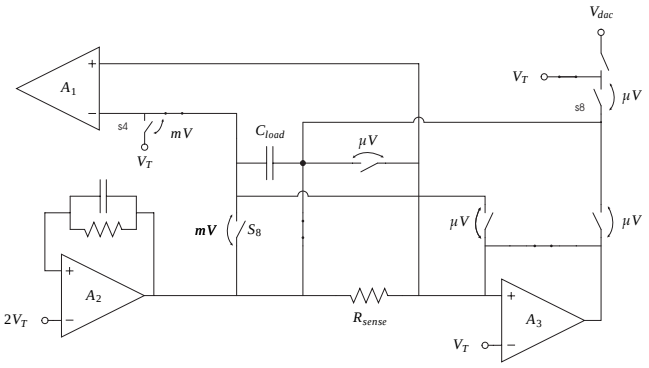


Figure 6.21: Order of magnitude of V_{ds} of the different switches. S_4 and S_8 were altered so their V_{ds} would be low enough.

Sample and Hold Figure 6.22 shows a basic sample and hold circuit that can be used to drive R_1 in Fig. 6.16 and provide ambient light correction. The input voltage V_{in}, being the output voltage of opamp A_3, charges the capacitor C_h which drives an emittor follower. During hold mode the switch transistor cuts off and the voltage on C_h is kept. In normal operation $3.5 \geq V_h \geq 1.5V$, so the

gate source voltage can become high enough to fully open a PMOS switch.[6] As a PMOS gives lower leakage current, we chose a PMOS switch. Again a well sized dummy transistor is used for charge in-

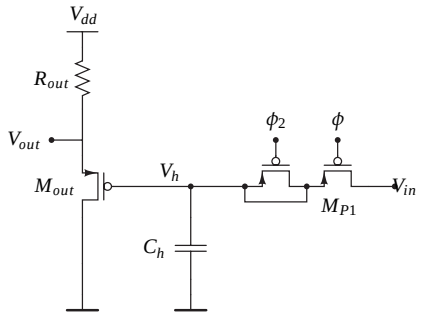


Figure 6.22: Simple S/H circuit

jection compensation. The voltage V_h should be stored for the entire measurement, meaning any leakage current towards C_h will result in an integration over time of the error current, similarily as with the offset compensation. The "integration time" during which V_h should remain stable, is now the sum of the charging time of C_{load} and the measurement time. Therefore C_{load} should be charged in a time of the same magnitude as the measurement time. We simulated with $T_{DAC}^{load} = 0.5ms$, comparable to the $256\mu s$ and $1.5ms$ measurement time for a $42pF$ or $262pF$ C_{load} respectively. Furthermore the allowed leakage current is very dependent on the size of C_h as

$$\Delta i = \frac{\Delta V_{hold}}{R_1} = \frac{I_{leakage} \cdot \left(T_{measure} + T_{DAC}^{load}\right)}{C_{hold} \cdot R_1} \tag{6.52}$$

If we would allow an error current to appear of $50pA$, the feedback loop with integrated $C_{load} = 42pF$ with an equally large S/H capacitor would allow only very small leakage currents:

$$C_h \cdot \frac{50pA \cdot R_1}{T_{measure} + T_{DAC}^{load}} = 42pF \frac{50pA \cdot 2M\Omega}{0.5ms + 8 \cdot 32e-6} \approx 5.5pA$$

[6] Note that for the previous switches source voltage was around $V_{T,n}$, which did not allow PMOS transistors as switches.

As mentioned however, simulation results showed very small leakage currents of $< 1pA$ through the switches. To reduce the chip size and be able to put different testing circuits on the IC we decided indeed to use a very small S/H capacitance of only $21pF$. Obviously this is a very poor judged choice. Luckely also this capacitor was brought externally and could be augmented.

For the feedback loop with added external capacitor the measurement time is larger and thus the S/H capacitor should be much larger as well to achieve the same error. When choosing a $470pF$ capacitor (simulations showed that a too large S/H capacitor gave rise to unstable behaviour of the loop) placed in parallel this still results in a small allowed leakage current of the S/H circuit of:

$$C_h \cdot \frac{50pA \cdot R_1}{T_{measure} + T_{DAC}^{load}} = 512pF \frac{50pA \cdot 2M\Omega}{0.5ms + 48 \cdot 32e-6} \approx 25pA$$

The same considerations as with the offset compensation capacitor are valid here: leakage currents should be minimized at all cost. In the off state the source bulk junction of the pmos switch is always inversly biased as $V_h \leq 3.5V$. V_{gs} and V_{gd} should be positive (PMOS) during off state to make sure no channel is formed. As the hold capacitor holds V_h, V_{gs} is positive. However when the ambient feedback loop is broken, the output of A_3 might go to V_{dd} and V_{gd} becomes $0V$, which is not optimal or go to ground. Either way V_{ds} of the PMOS switch is quite high: up to $3.5V$, possibly resulting in high leakage currents.

Fig. 6.23 solves the issue by actively keeping the voltage over the switch very small using an additional opamp A_{ex}. When M_{P1},M_{P2} and M_{P3} are switched off, M_{P4} opens as well. With the slightly delayed clock for the dummy transistors, M_{P5} can now be closed. The opamp will make $V^* = V_h \pm V_{os}$, where V_{os} is the opamp offset and the needed input voltage at its inputs. Thus only a very small voltage is seen over the switch, resulting in smaller leakage currents. One should note that the added feedback circuit still allows allows V_h to drift away. If $V^* = V_h + \Delta v$ due to A_{aux} offset and input pin voltage, this will charge C_{aux}^2 through the parasitic resistance of M_{P3}. Similarly both C_{aux}^1 and C_h will (slowly) be charged. As V_h rises, so will V^*, due to A_{aux}. The difference between V_h and V^* will always

remain $\approx \Delta v$, resulting in a (very slow) linear rising/falling of V_h. This added opamp feedback is another extra feedback loop within the overall feedback loop. For this reason we decided not to implement this idea on the test IC but found it worth mentioning nevertheless.

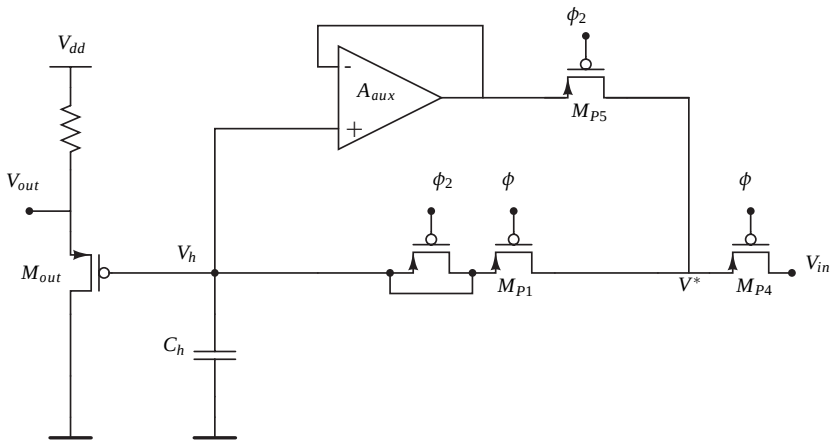


Figure 6.23: Improved S/H circuit: V_{ds} over the switch is kept low actively by A_{aux}

Another possible circuit is shown in Fig. 6.24: the drain voltage of the switching transistor is kept to V_h as well with a smaller capacitor $C_{aux}^{1,2} = 10pF$. Because this is a small capacitor, a small leakage current might discharge C_{aux}^1 rather fast, again resulting in larger V_{ds} for M_{P1}. Therefore a second stage was added keeping V_{ds} of M_{P2} low.

Opamp and loop design

The optical feedback circuit (repeated in Fig. 6.25) basically consists of a transimpedance amplifier (A_2) and an integrator (A_3). The transimpednace amplifier sets the voltage over R_{sense}, which reconverts the voltage back to a current, charging the capacitor. We already mentioned that opamp offset might result in an unwanted voltage drop over R_{sense} and consequently a current error. However, the am-

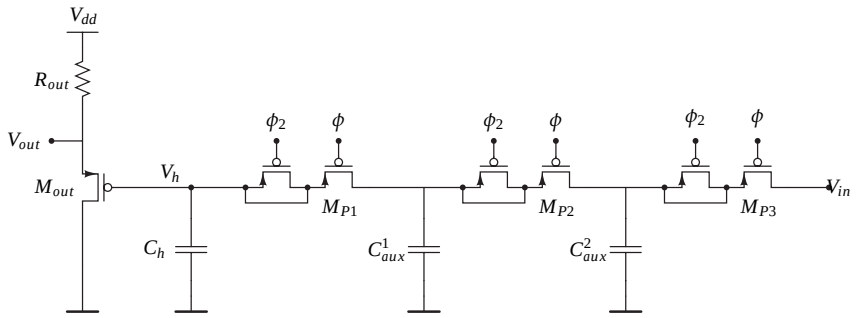


Figure 6.24: Improved S/H circuit: V_{ds} over the main switch is kept low by buffering with $C^{1,2}_{aux}$

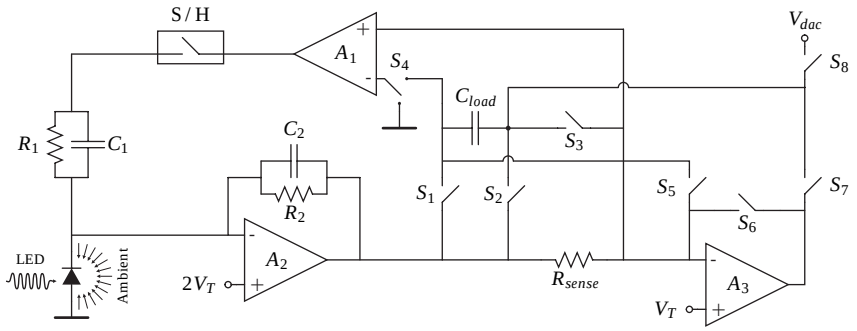


Figure 6.25: Optical feedback circuit

bient light feedback took care of the offset contributions of A_2 and A_3. Only for A_1 an offset compensation was required. Beside offset, the finite gain of the opamps will introduce a small voltage drop.

Opamp A_1 In the ambient feedback loop the input voltage ε_1 of opamp A_1 is given by:

$$\varepsilon_1 = \frac{R_2 I_{amb}}{\frac{R_2}{R_1}A_1 - 1} + \frac{\frac{R_2}{R_1} + 1}{\frac{R_2}{R_1}A - 1} \tag{6.53}$$

This voltage comes directly over R_{sense}, resulting in an error current. With the maximum error current in our design to be $250pA$ and already allowing some error by the leakage currents, designing this contribution to be $\leq 50pA$:

$$\frac{\varepsilon_1}{R_{sense}} < 50pA \Rightarrow A_1 \geq 89.5dB \tag{6.54}$$

This is a rather stringent gain requirement for the opamp. Luckily the offset compensation will also sample the required input voltage at the pins of A_1 while compensating for a possible offset. This means the error due to the finite gain of A_1 is nullified and a lower gain for A_1 is allowed.

Opamp A_2 For the transimpedance amplifier the relation between the input photocurrent and the output voltage of opamp A_2 is given by:

$$V = \frac{R_2 A_2 I_{ph}}{A_2 + \left(\frac{R_2}{R_1} + 1\right)} \tag{6.55}$$

The error current due to finite A_2 is given by:

$$\Delta i = \frac{R_2 I_{ph} - \frac{R_2 A_2 I_{ph}}{A_2 + \left(\frac{R_2}{R_1} + 1\right)}}{R_{sense}} \tag{6.56}$$

In our design, the pixel photocurred is expected $250nA \leq I_{ph} \leq 1.5\mu A$. We already mentioned at the beginning of Sect. 6.3.2 that

the allowed error current is inversly proportional to β^* or otherwise said to I_{ph}. For minimal I_{ph} we once more allowed an error current contribution of $50pA$ and find:

$$A_2 > 83.5dB \tag{6.57}$$

Note that I_{ph} consists of the pixel contribution and the ambient contribution. However, the ambient contribution and according error due to the finite gain A_2 was cancelled out by the ambient light feedback. This is why only the pixel contribution has to be taken into account here.

Opamp A_3 Similarly for the integrator opamp, the error current resulting from finite A_3 is given by:

$$\Delta i = \frac{V_{DAC}}{A_3 R_{sense}} \tag{6.58}$$

$V_{DAC} = 3V$ and again chosing this contribution to be smaller than $50pA$, results in

$$A_3 > 89dB \tag{6.59}$$

Opamp design Previous paragraphs showed that quite high gain opamps are needed to obtain the desired accuracy. Obviously very high gain/accuracy cuts into the bandwidht of the system. This is the main reason why in Chapt. 3 we proposed sampled optical feedback where the pixel was lit in advance of the measurement so no high bandwidth transient measurements were required. Figure 6.26 shows the three stage opamp circuit that was used. Capacitor C_1 (and C_2 to a lesser degree) is a miller capacitor used to pinch off the bandwidth by placing a pole at very low frequencies. For the different opamps the transistor sizes were slightly adapted to achieve optimal gain and bandwidth.

Figure 6.27 shows the AC characteristics of the designed opamps for both discussed loops. For the left side graphs A_3 is loaded with the circuit with $C_{hold} = 21pF$ and $C_{load} = 42pF$. The right side graphs show the characteristics for the second discussed loop with

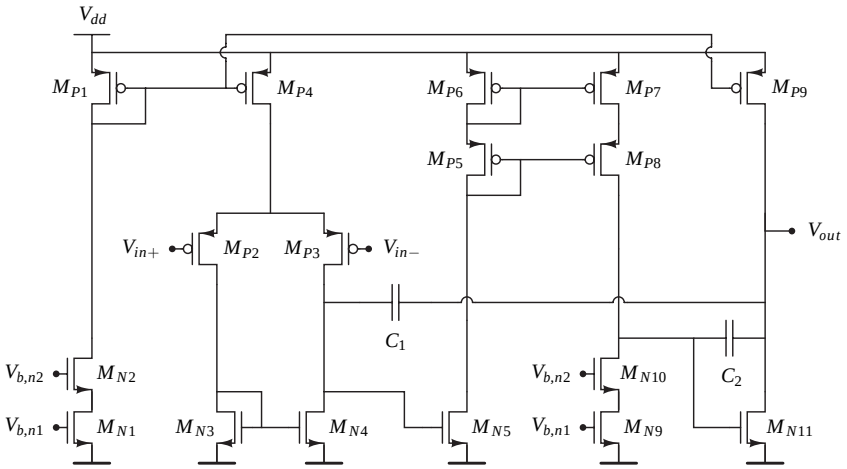


Figure 6.26: Opamp schematics

$C_{hold} = 21pF + 470pF = 491pF \approx 500pF$ and $C_{load} = 262pF$. As can be seen in both situations a high gain opamp with $\approx 90dB$ DC gain was designed with sufficient phase margin.

Figure 6.28 shows the AC behaviour of A_2. A DC gain of 94.62 dB was simulated with adequate phase margin. Figure 6.29 shows the AC behaviour of A_3. We designed an opamp with $\approx 100dB$ gain to be sure.

Photodetector Load and loop stability Opamp A_2 functions as a transimpedance amplifier for the photocurrent input by means of R_2. For the S/H voltage it is used as an inverting opamp via R_1 and R_2. The negative input of A_2 is however loaded with the photodetector which, as previously mentioned, can be a quite large capacitive load due to the large size of the photodetector. This capacitive load introduces an extra pole for the open loop gain of the inverting opamp circuit of A_2 because of it's decreasing impedance with increasing frequencies compared to R_2. This gives added phase shift, yielding unstability. Not only the AC behavior of opamp A_2 is changed by the photodetector's capacitive load, but the behavior of the ALF loop changes as well.

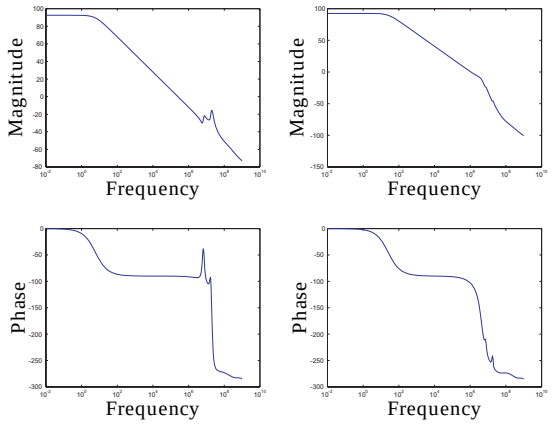


Figure 6.27: AC behaviour of the feedback opamp A_1

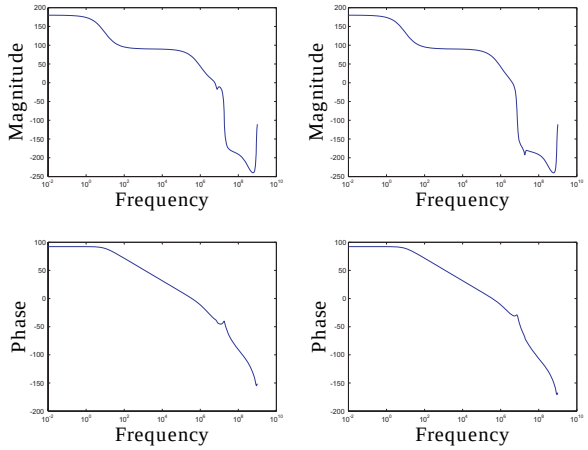


Figure 6.28: AC behaviour of transimpedance opamp A_2

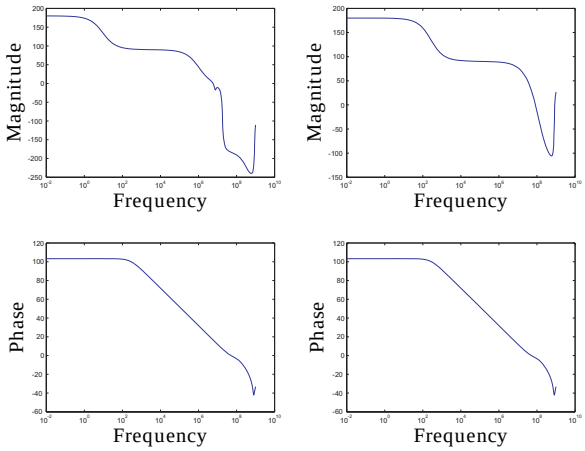


Figure 6.29: AC behaviour of integrator opamp A_3

Figures 6.30 and 6.31 show the loop gain of the ambient light feedback loop for the two discussed loops. On the left side graph the AC behaviour of the loop without any detector load is shown. For both loops the behaviour is stable. The middle graph shows the loop gain with a $500pF$ load on the input of the transimpedance amplifier. It is seen this messes up loop stability.

To counter this capacitors C_1 and C_2 were added to reduce the AC impedance in the feedback path. With C_2 the feedback impedance of opamp A_2 is reduced and C_1 reduces the R_1 path in AC. The right side graph in figures 6.30 and **??** shows the resulting AC behaviour which is stable.

At last figures 6.32 and 6.33 show the behaviour of the ambient light feedback loops under different photodetector load. We simulated up to $500pF$ detector load and the loops remain stable. Yet for the SIFL the phase margin melts away rather fast. As mentioned the photodetectors that were used are much smaller than is strictely necessary because of the limited chip area and thus the photodetecotr capacitive load will always be small enough for our measurements. However the graphs show in an actual application this is an impo-

rant parameter in the design process.

Comparator

As mentioned the output of the integrator (A_3) is monitored by a comparator. When the integrator's output voltage drops below V_T the comparator will switch off. This comparator output drives a counter which samples the duty cycle as shown in Fig. 3.9 on p.73. Obviously the comparator's fall time should be fast enough compared to the sampling periode. This corresponds to a worst case voltage swing at the comparator's input

$$\Delta v \ll \frac{I^0_{pix} \cdot \gamma \cdot 8 \cdot T_{sfr}}{C \cdot 2^{11}} \approx 750\mu V \tag{6.60}$$

Allowing an input voltage of e.g. $75\mu V$ requires a comparator gain of $99dB$. Figure 6.34 shows the used schematics for the comparator. We used a three stage amplifier with positive feedback in the last stage to obtain sufficient gain and speed. The different stages are framed in Fig. 6.34. M_{N1},M_{N2},M_{P1} - M_{P4} form a simple differential pair amplifier which voltage output drives a second differential pair (M_{P7} and M_{P8}). The currents from this second stage are mirrored into M_{N5} and M_{N7} which drives the positive feedback stage.

When $V_{in+} > V_{in-}$ M_{P7} will conduct and M_{P8} will be cut off. Therefore i_1 is sourced by M_{P10} making sure M_{P11} will conduct too. This pulls v^* high (as no current flows through M_{N7}) thus cutting M_{P13} and M_{P14} off. When V_{in+} falls clearly the current through M_{N7} will rise and M_{P11} will source more current which will reduce v^*. As soon as v^* is low enough, M_{P13} will start to take over the current i_1 from M_{P10}. This will lower the gate source voltage of M_{P11}, creating a positive feedback situation. Because v^* will only vary by V_T an inverter output stage is added and transistor M_{P14} lowers v^* so the inverter will switch correctly.

Making $M_{P10} = M_{P12} = A$ and $M_{P11} = M_{P13} = B$ [49] shows hysteresis can be added by chosing different W/L for these transis-

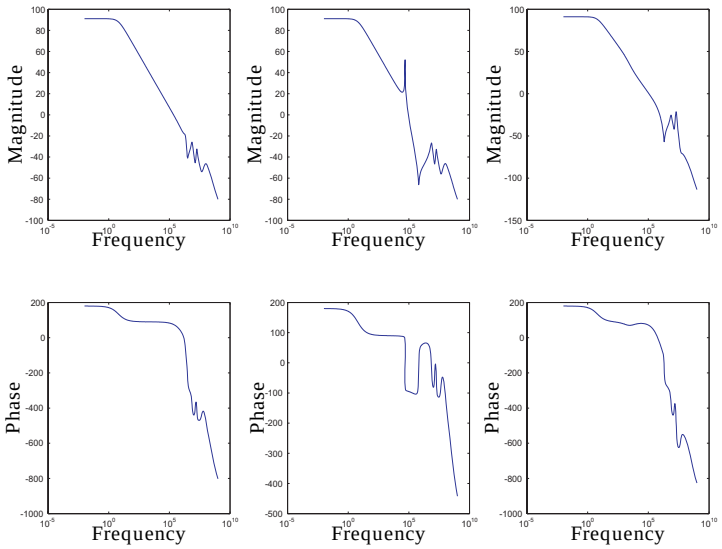


Figure 6.30: Feedback loop stability FIFL with 500pF photodetector load. Compensation is required over R_1 and R_2.

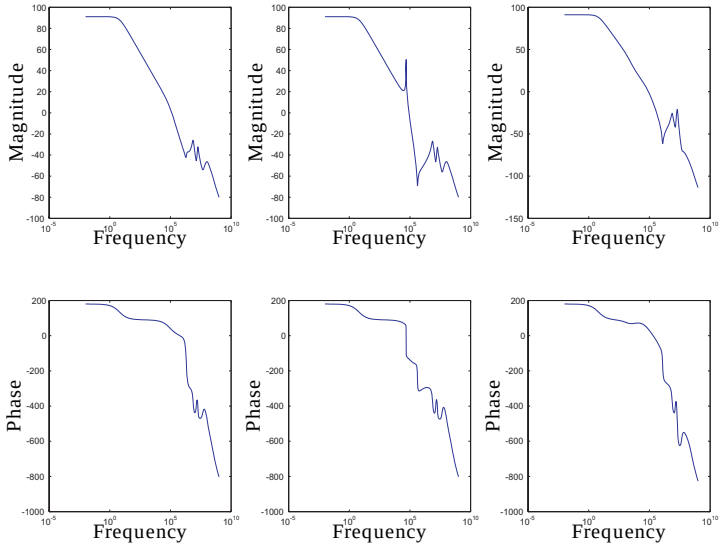


Figure 6.31: feedback loop stability SIFL with 500pF photodetector load. Compensation makes the loop stable again.

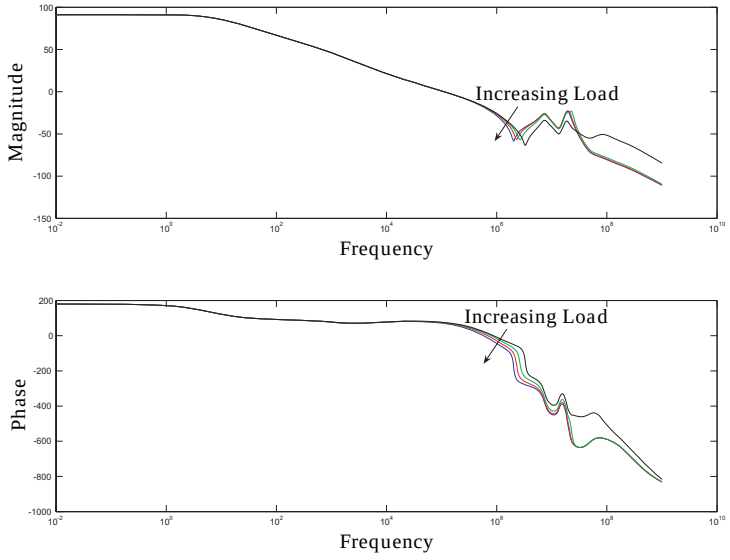


Figure 6.32: FIFL with changing photodetector load. no load, $100pF$, $250pF$, and $500pF$.

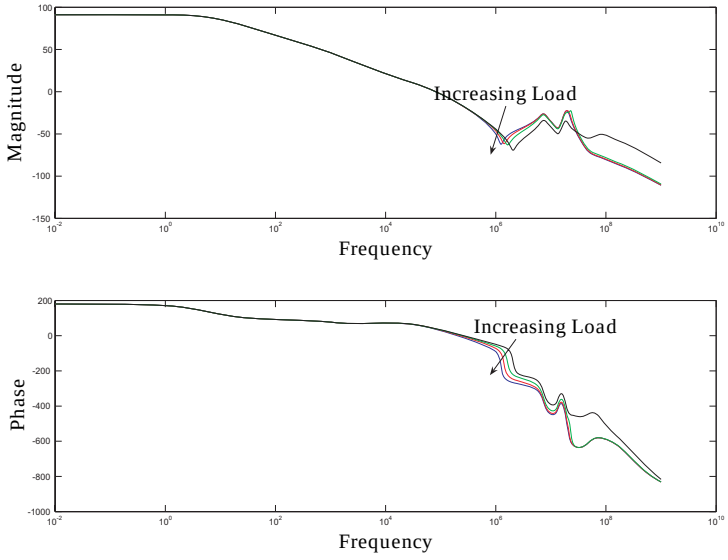


Figure 6.33: SIFL with changing photodetector load. no load, 100pF, 250pF, and 500pF are shown.

tors. The trip point is then given by:

$$V_{\pm} = \pm \frac{I_{M_{P9}}}{g_m} \frac{\frac{\beta_B}{\beta_A} - 1}{\frac{\beta_B}{\beta_A} + 1}, \qquad \beta = \frac{W}{L} \tag{6.61}$$

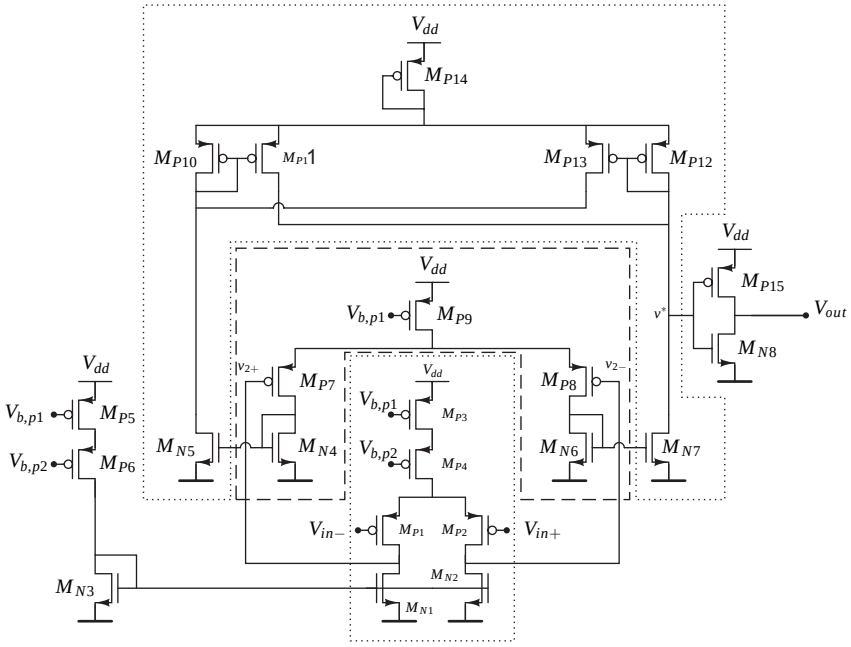


Figure 6.34: Biasing circuit for the DAC. Low voltage

Figure 6.35 shows a switching simulation of the comparator which is sufficient for our application.

Transient behaviour

Figure 6.36 shows the simulated error current during a transient simulation of the two different loops. The loops were simulated without ambient light contribution and with $375nA$, $750nA$, $1.125\mu A$ and $1.5\mu A$ ambient light contribution and $250nA$, $375nA$, $750nA$, $1.125\mu A$ and $1.5\mu A$ photodetector current, with a $500pF$ detector capacitive load. The lower graph is the second loop ($C_{load} = 262pF$,

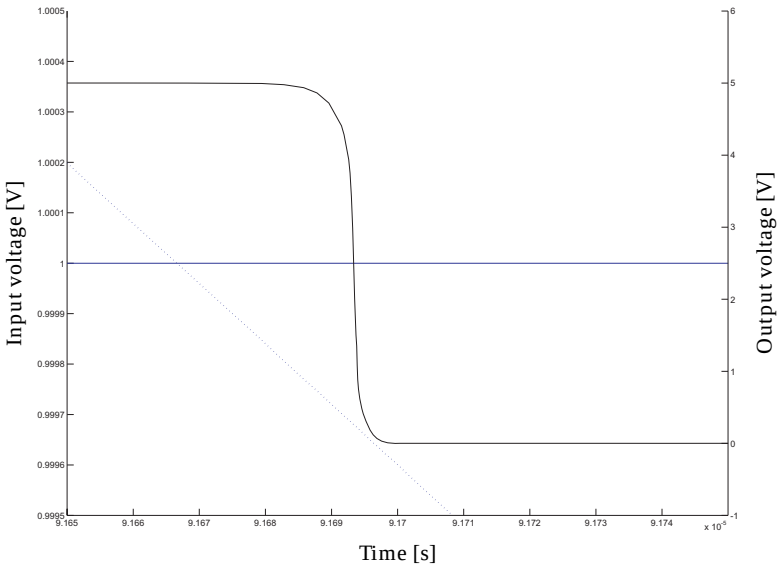


Figure 6.35: Switching behaviour of the comparator

$C_{hold} = 512pF$) and the upper graph represents the first loop ($C_{load} = 42pA$ and $C_{hold} = 21pA$). We added the dotted line which represents the maximum allowed error current $I_{ph} \cdot \alpha = I_{ph} \cdot 1e-3$. As can be seen the different datapoints are very similar for the different ambient light contributions. The first loop however does not succeed to stay below the $250pA$ minimum error condition. Keeping in mind that this is an ideal simulation without noise error contribution, the behaviour will not be optimal for low input currents. The second loop on the other hand shows excellent behaviour.

Figure 6.37 shows the most important transient waveforms. In the upper graph the dotted line represents the input current: first a $750nA$ ambient current is applied, which is measured by and compensated for by the ambient light feedback loop. The compensation current is the dashed line and the solid line represents the current through R_{sense}. As can be seen it is $1.25\mu A$ because $500nA$ is needed to obtain the $1V_T$ voltage drop over R_2. After $500\mu s$ the offset compensation takes place and after $1ms$ the pixel is turned on an starts generating a photocurrent of $1\mu A$. At this time the DAC also charges C_{load}. After $1.5ms$ C_{load} is placed over the integrator. The lower graph shows the comparator input and output (dotted line). Clearly the photocurrent starts discharging C_{load} until it reaches the comparator threshold. The dynamic behaviour of the feedback loop is very slow. This is of course expected based on the very low bandwidth of the opamps. Taking a time larger than $0.5ms$ between the switching phases did not noticably reduce the error, so measurements were also done with this value.

6.4 Measurements

6.4.1 Measurement setup

The measurements on the test IC were performed as shown schematically in Figure 6.38. We used a DAC to drive the LEDs with a resistor in series. Because the DAC was only able to provide low output current on its channels, high gain buffers were needed to drive the LEDs. The LED output is then measured by the integrated

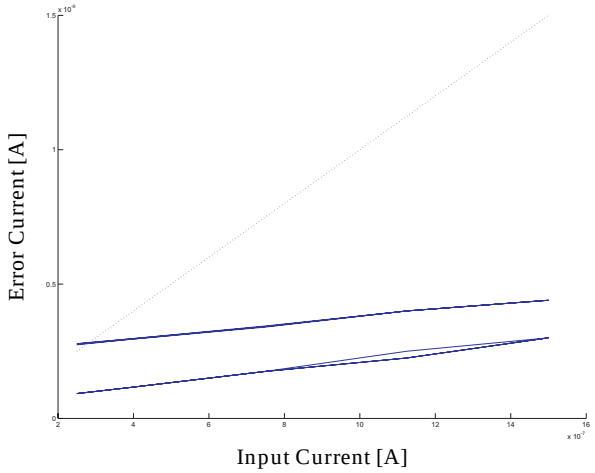


Figure 6.36: Simulated transient error current

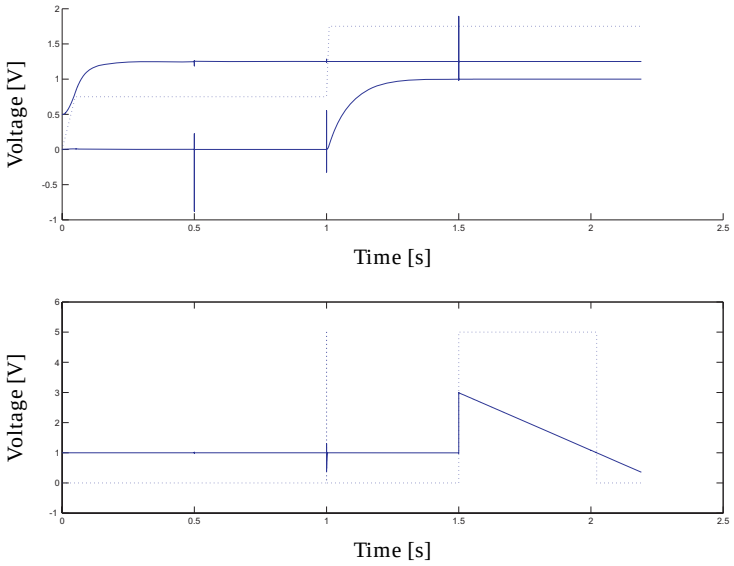


Figure 6.37: Transient waveforms of the optical feedback circuit

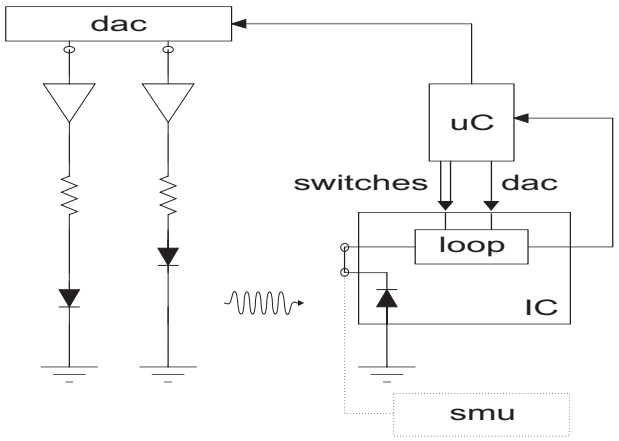


Figure 6.38: Schematical presentation of the measurement setup

photodetector and the measurement loop will generate a comparator output signal with a width T_{on}^{comp}. The loop switches are driven from the microcontroller (uC) and the uC also samples this output with its 12MHz clock. Not to introduce an extra error, we used the microcontroller 12bit DAC to apply the DAC voltage for C_{load}. As is discussed in previous chapters, this is the required resolution for a linear DAC corresponding to our 10bit exponential DAC.

The LEDs were placed on a thick aluminium holder to provide temperature stability and were placed arching the IC. This was needed because of the small size of the integrated detectors and large incident optical power was needed to obtain the required photocurrent. We used a 10 bit DAC to drive the LEDs to have a steady light output. The LED output power was measured with the on-chip photodiode and a high precision SMU as a reference measurement. The measured curve is shown for the red LED, which we used as "pixel", in Figure 6.39. As the LED is not perfectly current driven in this setup obviously a slightly nonlinear V-I characteristic is found. For our measurement we are only interested in the photocurrent vs. T_{on}^{comp}, so this is not a problem.

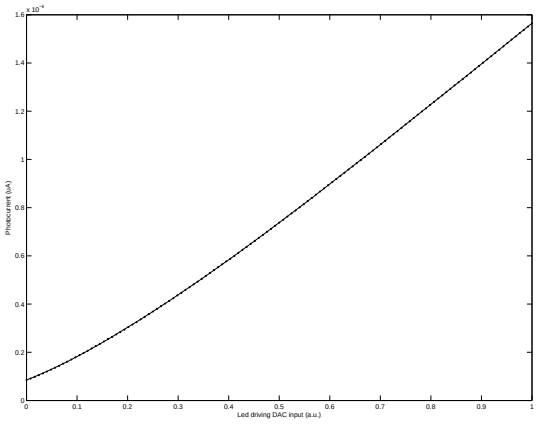


Figure 6.39: Reference measurement on the "pixel": measured photocurrent vs. swept DAC input

6.4.2 General Functionality

Functional proof of concept

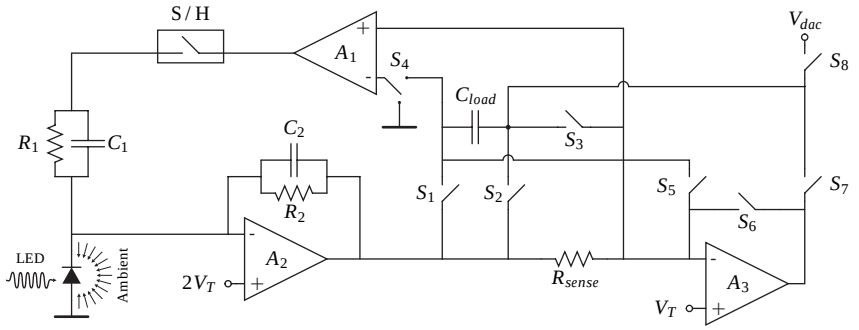


Figure 6.40: Optical feedback circuit

Figure 6.40 retakes the optical feedback loop schematic. To visualise the transient behaviour of the loop there is a problem: most nodes are very sensitive to leakage currents and actually only the

comparator output can be measured safely. For example measuring on the external C_{hold} would introduce large leakage currents, resulting in loop failure. The same holds for C_{load} as it is used for offset compensation and a continuous measurement is unacceptable. However for C_{load} there is a way around this: the DAC is also an external pin. When switch S_8 is open the load on this pin obviously does not influence the circuit and the ambient light correction feedback works. Then the capacitor C_{load} is charged with V_{DAC} by closing S_8. Normally after the loading time S_8 opens again and S_7 opens. By keeping S_8 open at that time, we can measure the discharging waveform of the capacitor (=input of the comparator). Note that at that time the measured node is driven by the integrator output and is no longer very sensitive. Of course this means the DAC output should be switched off. Therefore we used an external DAC with enable / disable function for our measurements. Before S_7 is closed and the capacitor starts discharging, the DAC output is switched off.

Figure 6.41 shows the output of the integrator for the loop with external capacitors with $V_{DAC} = 2V$ for a photocurrent of $\approx 475nA$ with similar ambient current. The voltage indeed decreases linearily as is to be expected. The comparator output is plotted as well. We measure $\approx 550\mu s$ on the (rough) scope data, which corresponds roughly to the expected value.

This scope plot merely shows the loop is functionally working as expected, yet does not quantify a measurement. Therefore we did an automatic measurement where we swept V_{DAC} and the photocurrent and measuring the comparator output for each combination.

Fully integrated Feedback Loop

Figure 6.42 shows the measured discharge time as a function of the applied photocurrent with $V_{DAC} = 2.266V$ (making the voltage over $C_{load} = V_{DAC} - V_T$). We swept the photocurrent over the entire expected range: $I_{ph} \in [85nA, 1.5\mu A]$. Several identical measurements were plotted and compared to the ideally expected discharge time

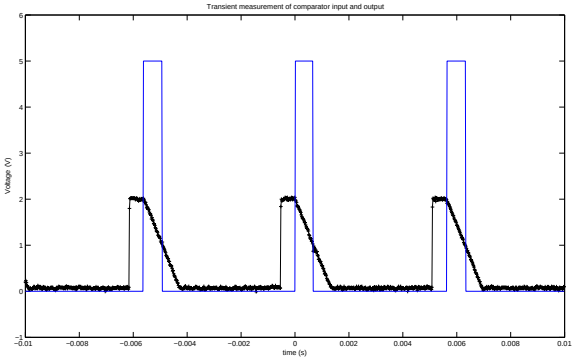


Figure 6.41: Transient measurement of the comparator input and output. C_{load} is linearily discharged by the photocurrent.

(dotted line):

$$T_{on}^{id} = C_{load}\frac{V_{DAC} - 1V}{I_{ph}} \tag{6.62}$$

A few things are clear: the general trend is definitely correct: the measured T_{on} is inversely proportional to the applied photocurrent. For lower photocurrent on the other hand, the measured T_{on} is completely wrong. The measured value jumps up and down without any trend. Figure 6.43 shows the comparator input when no photodetector is connected to the loop: we see the capacitor discharges with varying speed. Note that the measurement time for this loop is $8 * 32e - 6 = 256\mu s$. Based on the scope data we estimated the error current responsible for the capacitor charging / discharging: up to $250nA$ error current is found. We found mostly positive error current contributions (discharging capacitor). A possible explanation seems the poor choice of $C_{hold} = 21pF$. Larger then expected charge injection and leakage currents might easily offset the sampled voltage and cause a significant error current.

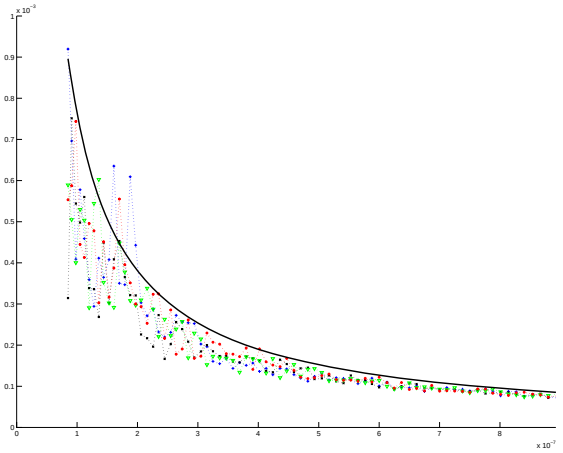


Figure 6.42: Integrated loop measured discharge time vs. photocurrent

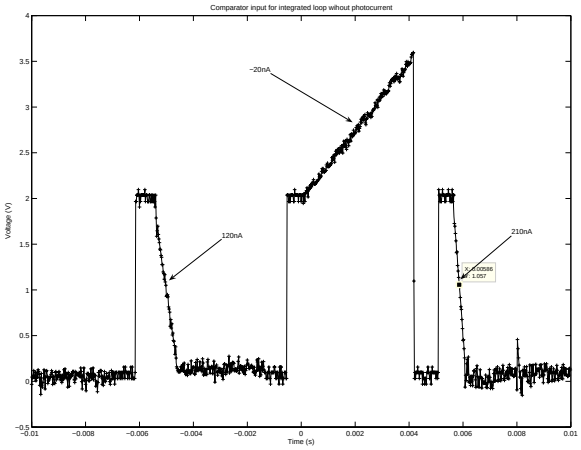


Figure 6.43: Transient measurement of comparator input for loop 1 without any photocurrent. We see a large error current exists.

Semi integrated loop

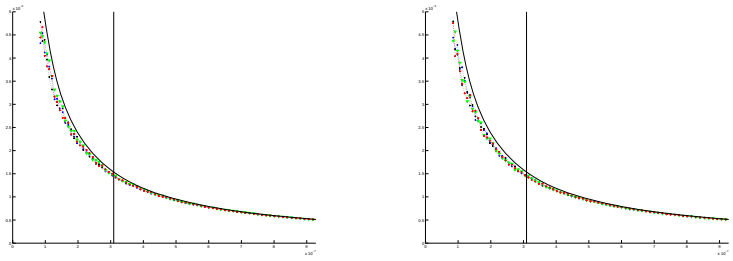
Figure 6.44(a) shows the measured T_{on} for the semi integrated feedback loop with $C_{hold} = 500pF$ and $C_{load} = 262pF$. A DAC voltage of $2.813V$ was applied and the photocurrent was swept over the entire range without ambient light contribution. Ideally a photocurrent of $930nA$ should discharge C_{load} in T_m / γ. Therefore the graph only shows the part up to this current. The vertical line represents an input current three times smaller, corresponding to the maximum ageing factor. It can be seen that the measured waveforms follow the ideal line, as was the case with the previous loop. Here too at smaller input photocurrents we see a deviation from the ideal line, yet not as dramatically in Fig. 6.42. Though it is clear a much larger error current than designed for is still present. In Fig. 6.44(b) the same measurement is shown, but now with an ambient light contribution of $\approx 750nA$. The graph still follows the ideal line, yet the error has become larger. Based on the graphs presented we can conclude that ambient light is indeed rejected, yet not as well as we would hope.

6.4.3 Quantification

Based on the graphs from above we decided not to look into the fully integrated loop measurements any further because the error current contribution has the same order of magnitude as the minimum photocurrent and results are very poor. The following results are therefore those of the SIFL with added external capacitors.

Relative T_{on}

Figures 6.45 to 6.47 show the extend to which the optical feedback is capable to keep the light output constant. This was simulated by keeping the DAC voltage constant and decreasing the input photocurrent. We show 3 different initial input photocurrents with corresponding ideal DAC values as listed in Table 6.3. Each set was measured without ambient light,$\approx 375nA$ and $\approx 750nA$ ambient light. For each situation the measurement was repeated 4 times. We



(a) No ambient light contribution. (b) $\approx 750nA$ ambient light contribution

Figure 6.44: Measured T_{on} vs. photocurrent for semi integrated loop with $V_{DAC} = 2.813V$

can define an ageing factor for the applied photocurrent:

$$a = \frac{I_{ph}}{I_{ph}^{init}} \tag{6.63}$$

Figures 6.45 to 6.47 plots the measured T_{on} relative to the ideal $T_{on} = T_m/3$. For lower photocurrent (Fig. 6.45) the deviation is actually quite large and goes up to 5%. For increasing ambient light the deviation even becomes larger. For higher input current (and higher V_{DAC}) the deviation is less, which is expected as noise and error currents become relatively smaller. Still the seen deviation is quite large and up to 2% at best.

I_{ph}^{init} (μA)	V_{DAC}
$470nA$	1.953V
$919nA$	2.813V
$1.347\mu A$	3.672V

Table 6.3: Photocurrents and corresponding optimal DAC value used for simulations

Relative error

In chapter 3 we provided the general equations to design a circuit that allows a pixel deviation smaller than the "just noticeable difference" from the DICOM curve. The ideal (desired) output energy for the kth grayscale was given by:

$$E_d(k) = \frac{k}{2^r - 1}\left(\frac{T_m}{\gamma}\cdot L\cdot\gamma + L\cdot\gamma\frac{\Delta t_{fr}}{2}\right) \tag{6.64}$$

with γ the initial overdrive factor, L the pixel luminance and Δt_{fr} the difference between pixel fall and rise time.

The sampled optical feedback measures during a time T_m and "replays" this measured time by concatenating several subframes as shown in Fig. 3.11 on p. 76. Normally an initial calibration is done to determine the correct DAC voltage to make sure $T_{on} \approx \frac{T_m}{\gamma}$. This would require a very precise external measurement system and was not made during the course of this research. To qualify the measurement non the less, we will consider the output energy of a pixel as follows:

$$E_{pixel}(k) = k\cdot\left(x\cdot\frac{T_m}{2^s}\cdot\frac{T_{sfr}}{T_m}\cdot L\cdot\gamma\cdot a\right) + L\cdot\gamma\cdot a\frac{\Delta t_{fr}}{2} \tag{6.65}$$

with x being the number of clock cycli counted by the sampling clock from the uC, set at a periode of $T_m/2^s$. As mentioned this would be rescaled to a subframe and replayed k times. The rise and fall error is also contributing. With this in mind, the relative error can be found.

$$\Delta E_{rel} = \frac{\left|E_d(k) - E_{pixel}(k)\right|}{E_d(k)} < \frac{1\ JND\cdot T_{frame}}{E_d(k)} \approx \frac{\frac{T_m}{\gamma} - x\cdot\frac{T_m}{2^s}\cdot a}{\frac{T_m}{\gamma}} \tag{6.66}$$

Note that for $\Delta t_{fr} = 0$ this obviously corresponds to the relative error on the measured time. In Figures 6.48 to 6.50 we show the relative error found based on the measurement results as a function of the ageing parameter where we took $\Delta t = 170ns$ as designed for. We plotted the DICOM border and the "2% rule" from Weber's law as

well. For low photocurrent it is clear the relative error is much too high and has a very large noise contribution. For higher photocurrent the results are a bit better, yet the DICOM condition is hardly met and when the pixel "ages" the error rapidly rises.

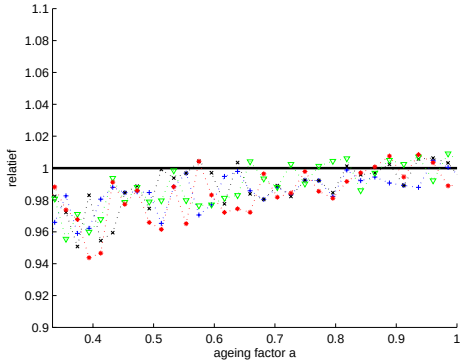
6.5 Discussion and remarks

From a functional point of view the results are rather good. The feedback loop actually scales the duty cycle according to the incident light and provides ambient light correction. The measured values as presented show a quite large error contribution. For a fully integrated feedback loop this contribution is very large and totally messes up the system. For the semi integrated loop there is an improvement, yet the errors are still much higher than expected.

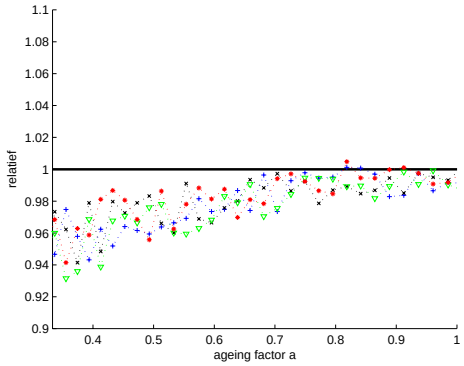
We suspect the main problem for the integrated loop lies in the charge injection of the switches, both in the sample and hold and the offset compensation mode. A poor choice of a much too low sample and hold capacitor introduces a very high error, comparable to the smaller photocurrents. Besides charge injection also noise contributions are sampled at that time, yielding rather large errors on a smaller capacitor. Adding external capacitors improved the behaviour significantly.

Another cause of the noisy measurements is probably the measurement setup. During each measurement the photocurrent was supposed to be identical. Though we used a 10 bit DAC to drive the LED, error contributions from this system were not defined: noise, temperature behaviour,... might influence the measurement profoundly. The LEDs were driven with quite large a current, up to $500mA$. Though attached to a thick aluminium holder, we still noticed heating of the LED. However all measurements were plotted based on the same measured characteristic from Fig. 6.39. Also the buffer driving the LEDs showed severe heating. This means the voltage applied to the resistor driving the LED might also shift from measurement to measurement.

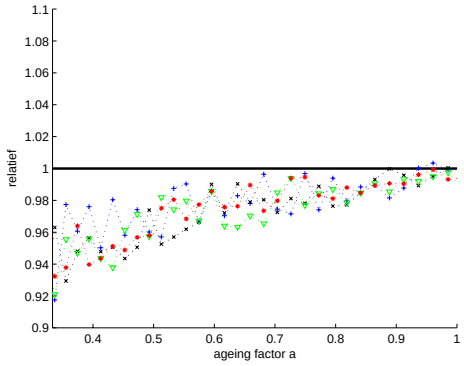
Thirdly we should mention the test IC was opened to allow incident light. As mentioned in 5 photocurrents start flowing eas-



(a) No ambient light contribution

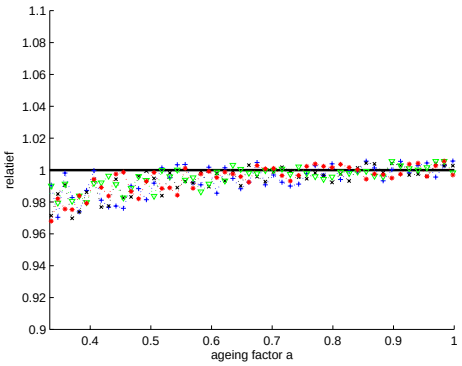


(b) $\approx 375nA$ ambient light contribution

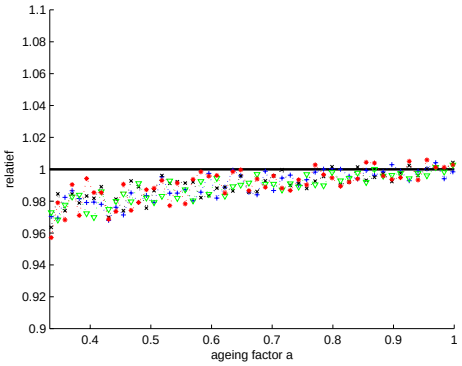


(c) $\approx 750nA$ ambient light contribution

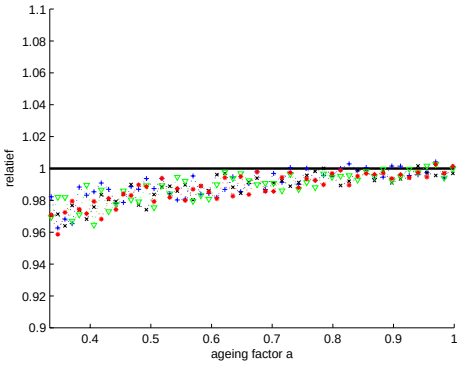
Figure 6.45: Measured relative T_{on} vs. ageing factor of the photocurrent. $V_{DAC} = 1.953V$ and $I_{ph}^{init} = 470nA$



(a) No ambient light contribution

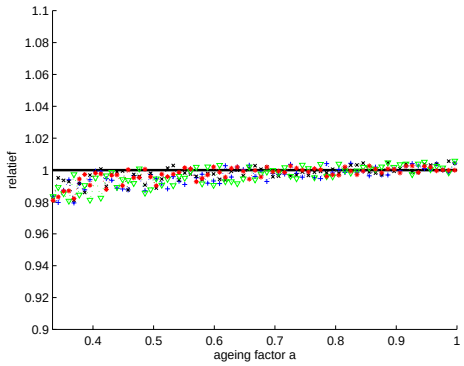


(b) $\approx 375nA$ ambient light contribution

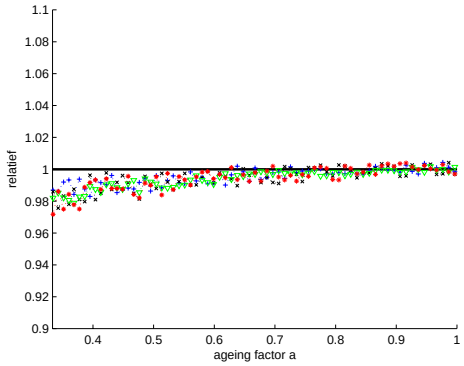


(c) $\approx 750nA$ ambient light contribution

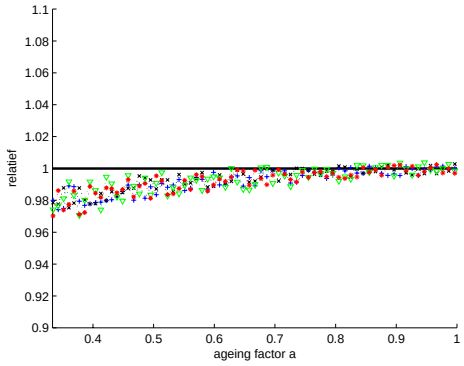
Figure 6.46: Measured relative T_{on} vs. ageing factor of the photocurrent. $V_{DAC} = 2.813V$ and $I_{ph}^{init} = 919nA$



(a) No ambient light contribution

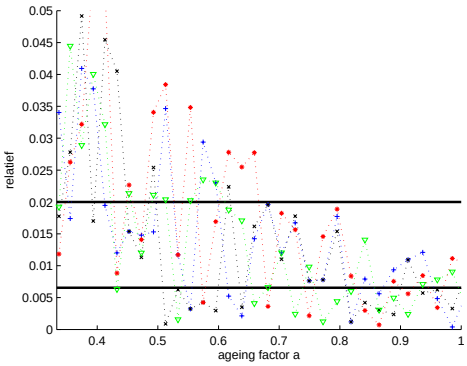


(b) $\approx 375nA$ ambient light contribution

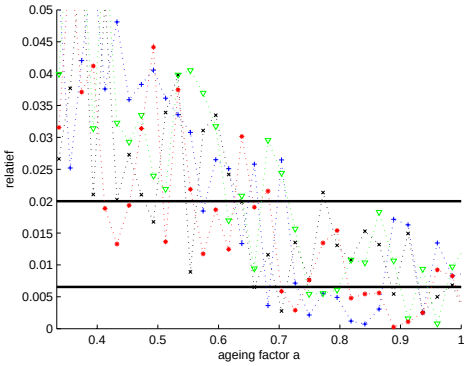


(c) $\approx 750nA$ ambient light contribution

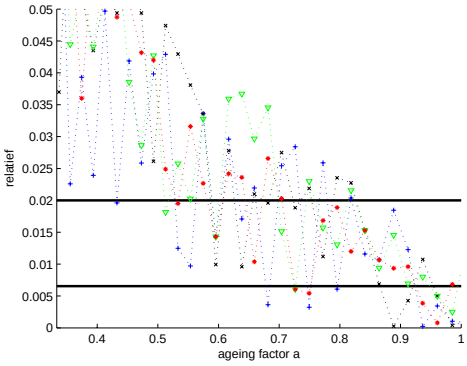
Figure 6.47: Measured relative T_{on} vs. ageing factor of the photocurrent. $V_{DAC} = 3.672$ and $I_{ph}^{init} = 1.347\mu A$



(a) No ambient light contribution

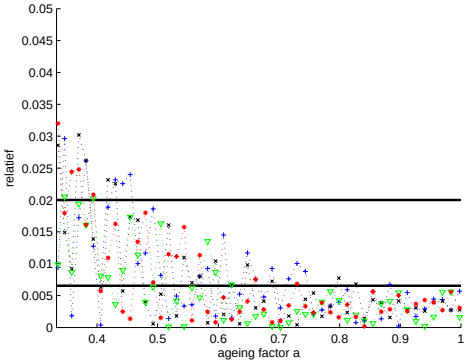


(b) $\approx 375nA$ ambient light contribution

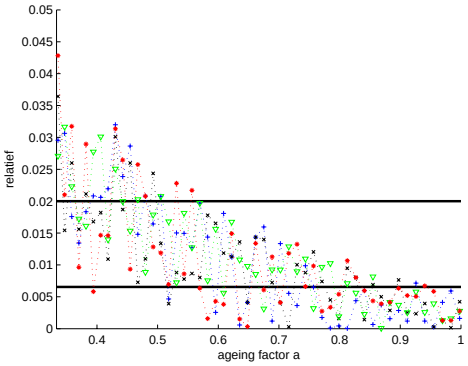


(c) $\approx 750nA$ ambient light contribution

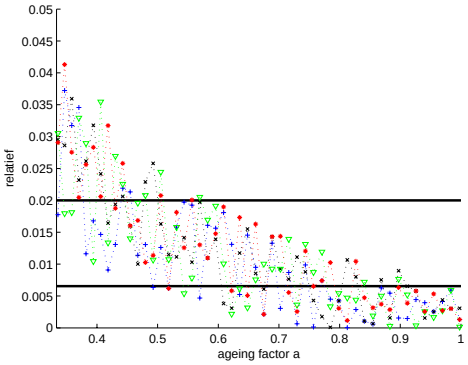
Figure 6.48: Measured relative error vs. ageing factor of the photocurrent. $V_{DAC} = 1.953V$ and $I_{ph}^{init} = 470nA$.



(a) No ambient light contribution

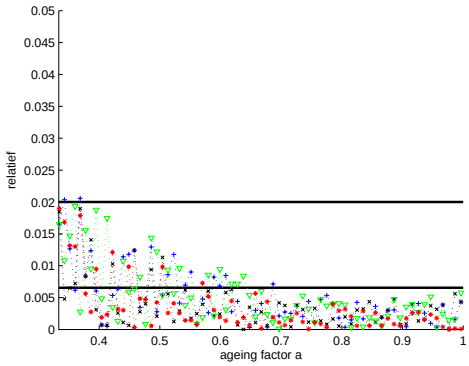


(b) $\approx 375nA$ ambient light contribution

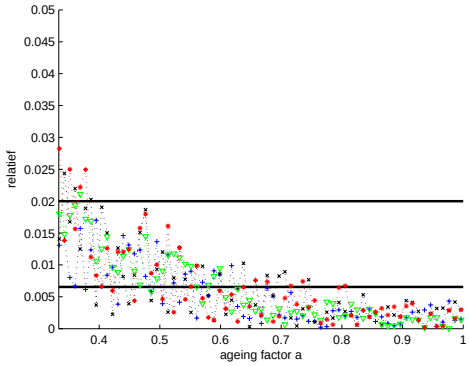


(c) $\approx 750nA$ ambient light contribution

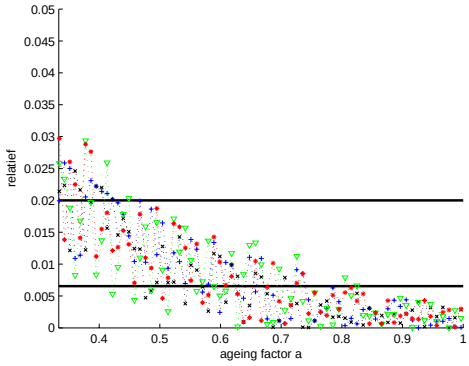
Figure 6.49: Measured relative error vs. ageing factor of the photocurrent. $V_{DAC} = 2.813V$ and $I_{ph}^{init} = 919nA$.



(a) No ambient light contribution



(b) $\approx 375nA$ ambient light contribution



(c) $\approx 750nA$ ambient light contribution

Figure 6.50: Measured relative error vs. ageing factor of the photocurrent. $V_{DAC} = 3.672V$ and $I_{ph}^{init} = 1.347\mu A$.

ily in non shielded silicon and give current contributions from $>$ $100\mu m$. Though most of the designed circuits was covered with on-chip metal, this was not done rigorously to block all incident light. Error contributions from this light in the IC wil also contribute to noise on the measurement.

7 Conclusions

7.1 Synopsis and main results

The first chapter of this work familiarizes the reader with perceptual equidistant grayscale levels and its influence on the display driving waveforms. Based on the data from the DICOM measurements of the human visual system the ideally required driving resolution for a linearly driven display are calculated and presented in Tables 1.1 and 1.2. Furthermore the rationale of this work is discussed: a calibrateable optical feedback loop for emissive displays to compensate ageing characteristics.

The second chapter justifies the choice for a PWM driven display when trying to implement the optical feedback. It is shown to the reader the constant working point and small complexity of the driver electronics allow an easy implementation of the optical feedback. This compared to AM driving of a display where very large dynamic range of the feedback signal prohibits easy implementation. In this chapter the importance of optical feedback is also calculated based on available ageing models for several types of emissive

displays. Table **??** shows the reader optical feedback can indeed augment the lifetime of a display, but also show the result can be much less than initially anticipated.

Based on these results several implementations of a optical feedback circuit are discussed in the next chapter. We slowly show an increasing complexity of the optical feedback circuit is necessary to achieve uniformity constraints. We show that the choice for an integrated photodetector requires a sampled optical feedback circuit to be able to used the same detector for several pixels. We also show a very large photodiode would be necessary to obtain a feasable feedback signal for all pixels and introduce the possibility of a phototransistor as a detector. Furthermore the problem of ambient light contribution to the feedback is discussed. Figures 3.9 and 3.10 present a circuit capable of sampled optical feedback with full calibration possibilities and ambient light rejection.

Before continuing to the actual IC implementation a short overview of a possible full scale driver implementation is given in Chapter four. Addressability, data stream and synchronisation are briefly discussed. The actual implementation of the proposed circuits and detectors is discussed in the last two chapters. Chapter five presents the layout, simulations and measurement results for several photodiodes and phototransistors in the used I^2T100 technology. It is noticed that the actual measurements of the photodetectors are quite distorted by photocurrent generated from surrounding silicon. As this contributions can easily be influenced by other substrate currents and signals from other parts of the IC, multiple guardrings are needed to block this contribution.

The last chapter describes the implementation of the circuit schematics in I^2T100. The implementation of an 10 bit exponential DAC, corresponding to its 12 bit linear counterpart, is presented. Statical measurements show a monotonic characteristic with indeed sufficient relative error between consequetive values. The measurement results on the optical feedback circuit are however possessed with a large noise and error contribution, but generally show a functional circuit.

7.2 Future work

Based on the theoretical and practical work, we propose several extra research possibilities and improvements to the existing circuit.

1. The ambient light rejection circuit should be rethought. As is seen from the test IC results, the choice for an analog S / H was probably not a good one. Digitalising this is adviceable.

2. The measurements on the test IC showed that the measurement setup needs to be tought of. In this light the necessary initial display calibration problematic should also be investigated. The influence of this measurement system on the overall performance of the display is subject to some thought and specifications should be defined.

3. The design of the photodetector learned that a higher bias voltage increases the photodetector's gain. It would be very interesting to design the optical feedback system with this in mind. As the current system was designed in a high voltage technology, the design of a high voltage input stage might be considered.

4. As mentioned an actual display implementation of the proposed driver circuit introduces new, not yet discussed error contributions. Influences of chip to chip variations on reference voltages, clock frequency,... and variations over time of these parameters should be investigated.

5. The main problem of any system that tries to equalise independent different nodes is obvious: after calibration each node will react independently and thus variations will occur by definition. The optical feedback simply shifts the problem from a very time dependent and very stressed component, the emissive pixel, to a more robust and steady system, in casu the IC, possibly resulting in a better performance. This work showed the demands to such a system are nevertheless very high. Future research should in our opinion try to create a system

where each node is able to recalibrate itself based on a distributed absolute parameter. This way no external calibration of the display is necessary.

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