Ontwikkeling en karakterisatie van technologie voor interconnectie van aanstuurelektronica met vlakke beeldschermen

Technology Development and Characterization for Interconnecting Driver Electronic Circuitry to Flat-Panel Displays

Jonathan Govaerts

Promotor: prof. dr. ir. J. Vanfleteren
Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen: Elektrotechniek

Vakgroep Elektronica en Informatiesystemen
Voorzitter: prof. dr. ir. J. Van Campenhout
Faculteit Ingenieurswetenschappen
Academiejaar 2008 - 2009

UNIVERSITEIT GENT

ISBN 978-90-8578-243-8
NUR 959
Wettelijk depot: D/2009/10.500/1

Technology Development and Characterization for Interconnecting Driver Electronic Circuitry to Flat-Panel Displays

Promotor:

Prof. Jan Vanfleteren (Cmst-ELIS-UGent / IMEC)

Board of Examiners:

Prof. Luc Taerwe (Foreman)

Dr. Ir. Tom Bert (BARCO)

Prof. Herbert De Smet (Cmst-ELIS-UGent)

Prof. Robert Mertens (SLT-IMEC / KULeuven)

Prof. Peter Van Daele (Cmst-INTEC-UGent)

Prof. Dries Van Thourhout (Photonics-INTEC-UGent)

The work described within this doctoral thesis has been supported by the University of Ghent, department of Electronics and Information Systems (ELIS), and IMEC, and was carried out at the Centre for MicroSystems Technology (Cmst), a research institute affiliated with both IMEC and Ghent University.

Contents

"Time is money, so you better have loads of it."

— Jodie Buyle (1983 - ...)

Nederlandse Samenvatting
Dutch Summary

"Een mooi boek zaait vraagtekens met milde hand."

— Jean Cocteau (1889 - 1963)

V*óó*r alles zou ik graag beginnen met een korte verontschuldiging voor het feit dat dit boek grotendeels in het Engels is geschreven: sorry, pardon ende excuseer. De reden hiervoor is niet zozeer dat de Nederlandse woordenschat ontoereikend zou zijn, en nog minder dat ik het Nederlands geen warm hart toedraag, maar eerder dat het mijn doctoraat toegankelijker maakt voor een ruimer publiek[1], alsmede dat het minder werk betekende voor mij, zowel op gebied van tijd als van moeite die ik erin zou moeten steken. Bij dit laatste punt hoort toch nog een beetje verduidelijking: aangezien het inhoudelijke van mijn werk voornamelijk in het engels gerapporteerd is geweest[2], ben ik gewend geraakt aan de engelse terminologie, en leek het bijgevolg efficiënter om het reeds gerapporteerde werk rechtstreeks in het engels te recycleren in dit boek, zonder tijd te moeten investeren in de vertaling. In mijn ogen was dit een aanvaardbare beslissing, omdat ik van mening was en nog altijd ben dat de taal hier ondergeschikt is aan de inhoud van het doctoraat[3].

Beginnende bij het begin, kan de titel het best vertaald worden als "Ontwikkeling en karakterisatie van technologie voor interconnectie van aanstuurelektronica met vlakke beeldschermen", of kortweg "Verbinden van aanstuurelektronica met beeldschermen". Beeldschermen zijn sedert de laatste vijftig jaar fel in opmars, zowel in absoluut aantal en geografische verspreiding als in de ontwikkeling van nieuwe en verbeterde technologieën. Deze ontwikkelingen laten ook de wereld van de interconnectie, die het verbinden van verschillende componenten beoogt, niet onberoerd. Een goede illustratie hiervan is bijvoorbeeld de relatief recente commercialisatie van de zogenaamde "high definition" televisietoestellen (HDTV), met als voornaamste kenmerk het beduidend grotere aantal beeldlijnen. Dit groter

[1] zowel voor geïnteresseerden als voor critici

[2] enerzijds aan Europese industriële partners en de Europese Commissie, anderzijds in internationale tijdschriften en conferenties

[3] onder de voorwaarde dat het geen invloed heeft op de (subjectieve) leesbaarheid van het boek, wel te verstaan

aantal beeldlijnen heeft immers implicaties voor de interconnectie, die vanzelfsprekend moeilijker wordt al naargelang de beeldlijnen dichter bij elkaar liggen en over een grotere oppervlakte verspreid liggen. Anderzijds ontluikt er een probleem bij de ontwikkeling van flexibele beeldschermtechnologieën: nu de beeldschermen zelf langzaamaan flexibel gemaakt kunnen worden, zelfs al op commerciële schaal, begint de belemmering in flexibiliteit zich geleidelijk aan te verplaatsen naar de zone van de aanstuurelektronica. Gelukkig wordt ook hier de laatste jaren meer en meer aandacht aan besteed, zodat het concept van flexibele en zelfs rekbare elektronica tegenwoordig al grotendeels verhuisd is van de gedachten van dromers en visionairen naar de labotafels van de meer geavanceerde onderzoekscentra, en er actief fundamenteel en toegepast onderzoek op wordt verricht.

Het eerste hoofdstuk is bedoeld en uitgewerkt als een introductie tot de wereld van beeldschermen. Eerst worden verscheidene courante beeldschermtechnologieën besproken, meer bepaald de effecten waarop ze gebaseerd zijn en hoe ze gefabriceerd worden. Daarnaast komen ook de belangrijkste methoden aan bod voor het elektr(on)isch aansturen van zulke beeldschermen, en het belang dat het type substraat heeft waarmee vlakke beeldschermen worden gefabriceerd. Hierna schetst het tweede hoofdstuk een eerder bescheiden doch relatief brede achtergrond van het begrip "interconnectie", meer bepaald elektrische interconnectie in de wereld van de elektronica en micro-elektronica. Het begrip interconnectie, in dit opzicht, kan opgedeeld worden in een aantal deelaspecten. Eerst wordt de dragerstructuur besproken, ook wel substraat genoemd in deze context, die het mechanisch gedrag van de verbinding grotendeels zal bepalen. Daarna komt het geleidend materiaal zelf aan bod, dat de elektrische stroom zal moeten geleiden over het substraat, en volgens een bepaald patroon. Tenslotte worden enkele veel voorkomende assemblagetechnieken voorgesteld, nodig om functionele componenten te kunnen verbinden met het aangebrachte interconnectiepatroon op het substraat. Na deze voornamelijk theoretische uitleg, worden een hele reeks praktische voorbeelden van beeldscherminterconnectie aangehaald en uitgewerkt, de ene al grondiger uitgediept dan de andere. Hoofdstuk 3 illustreert de assemblagemogelijkheden voor de huidige, commercieel beschikbare, vlakke en glasgebaseerde beeldschermen, terwijl Hoofdstuk 4 dieper ingaat op technieken voor assemblage van elektronische componenten op flexibele substraten, met het oog op toepassing in meer geavanceerde, flexibele plastic-gebaseerde beeldschermen. Zoals hierboven al eens vermeld, wordt het van hieraf stilaan duidelijk dat de flexibiliteit van het beeldscherm dreigt belemmerd te worden door de beperking in flexibiliteit van de aanstuurelektronica. Dit reële en groeiende probleem wordt uitgediept in Hoofdstuk 5, alwaar ook enige mogelijke oplossingen worden aangereikt. Naast de meer voor de hand liggende mogelijkheden, zoals het gebruik van flexibele substraten als dragers voor de aanstuurelektronica, het zoveel mogelijk herleiden van de interconnecties naar één zijde en plaats, en het lokaal verstevigen van de meest kwetsbare punten in het flexibel geheel, wordt het inbedden van de componenten in de flexibele substraten zelf naar voren geschoven als een meer drastische oplossing voor dit fundamentele probleem. Vanzelfsprekend

maakt een dergelijke oplossing alles aanzienlijk complexer, zowel qua ontwerp als wat betreft verschillende bijkomende fabricagestappen, maar potentieel kan zulks een doorbraak betekenen naar echt volledig flexibele elektronica. Eén zo'n mogelijke technologie werd in onze labo's ontwikkeld en behelst het extreem verdunnen en inbedden van elektronische chips in flexibele substraten. Als meest veelbelovende oplossing voor beeldschermtoepassingen, wordt één variant van deze zelf-ontwikkelde technologie tenslotte uitgewerkt in Hoofdstuk 6, de vlakke ultradunne chipverpakking, waar de verdunde chips ingebed worden in een vlakke en symmetrische sandwich van polymeerlagen. Naast de te gebruiken materialen en het ontwerp en de opbouw van de testverpakkingen komt ook het fabricageproces en de karakterisatie van de resulterende verpakking uitgebreid aan bod. Daarbovenop worden een aantal mogelijke optimalisaties uitgewerkt, zowel wat betreft het fabricageproces, als volgende stappen in het ontwikkelingsproces, meer bepaald het overschakelen op functionele chips i.p.v. testchips, het inbedden van meerdere chips in hetzelfde substraat, een nodige voorwaarde voor massaproductie en dus ook industrialisatie, en het assembleren van testverpakkingen op andere substraten.

Na het laatste technische hoofdstuk, rond ik af met een soort naschrift, waar er een beknopt overzicht wordt gegeven van wat de voornaamste resultaten, die voortvloeiden uit het gevoerde onderzoek. Daarna wordt het beschreven onderzoek in een breder kader geplaatst, waarbij de onderzochte technologieën gebruikt zouden kunnen worden in tal van andere toepassingen in de micro-elektronica, naast de wereld van de beeldschermen. Tenslotte wordt een overzicht gegeven van hoe de verkregen kennis verspreid is geweest naar de rest van de wereld[4]: nieuwsbrieven, thesissen, artikels en conferenties.

Ik wens u zo veel mogelijk leesgenot, en dank u bij voorbaat,
Jonathan

"Prijs de dag niet voor het avond is,
Een vrouw niet voor ze kwaad geweest is,
Een zwaard niet voor het gebruikt is,
Een meisje niet voor ze in het huwelijksbed is,
IJs niet voor het geproefd is,
En bier niet voor het gedronken is."

— Vikingspreuk

[4]of toch naar de geïnteresseerden in de rest van de wereld

Preface

"The secret of a good sermon is to have a good beginning and a good ending, then having the two as close together as possible."

— George Burns (1896 - 1996)

First off (obviously, since this is the preface), I would like to make a confession to you, the reader, partly for the sake of honesty and clarity, but more importantly, it might allow you to better understand how this thesis has grown from different angles. Although the thesis might seem logically built up, the sequence of topics as they have been reported herein, does not always respect the chronological order in which the research behind it was carried out.

The doctoral thesis lying in front of you is titled "Technology Development and Characterization for Interconnecting Driver Electronic Circuitry to Flat-Panel Displays", or somewhat shorter "Interconnecting Drivers to Displays". However, this is not the title that was initially intended, which was, "Electrical Interconnection by Means of Conductive Adhesives and Inks". Although most of my research can easily be classified within this title, it seemed too broad, so I gathered it would make my thesis far more understandable if the title could be narrowed down a bit to something more specific and, more importantly, to a subject that appeals more to the imagination[5]. This is also the reason you will find a lot of pictures accompanying each section: in my opinion one good picture can say more than what I can tell you in 2-pages-worth of writing[6]. I truly hope that this will broaden the audience for this book, and will rouse people's interests both to open it and to read it, if not completely, at least partly. After all, this thesis reflects what I have been working on in the last four years of my life (so far). This said, I will switch to the more content-related part...

More than half of the work was carried out in the framework of a European project called FlexiDis. As the name indicates, the project's main intention was advancing flexible display R&D in Europe, with the express purpose of strengthening (flexible) display manufacturing in Europe. The main benefits of this frame-

[5] ...how better to visualize a subject than with displays, the prime example of visualisation technology...

[6] ...which either learns you something about good pictures, or about my writing... Please find out for yourself

work, at least from my humble point-of-view, are the close links to industrial partners, providing information on the state-of-the-art, as well as feedback from more application-oriented businesses, and the introduction of a stimulating environment by showing how the investigated technologies could be usefully implemented. The FlexiDis project is also the main responsible behind shifting the more general nature of my research to a more focused approach as confessed above, although the theses I supervised also had a part in that. Finally, it was interesting to witness the difference between the enthousiasm of the -mostly younger- research-oriented people and the more down-to-earth attitude of the -on average more experienced- industry-oriented people within the project.

The first chapter gives a concise introduction to the world of displays. Different kinds of display effect types are discussed, together with their working principles and fabrication technologies. Also, the most common driving methods are explained and the importance of the type of substrate used for flat-panel displays is elaborated. After this, the second chapter provides a basic background for interconnection, what it means, why it is necessary and how it is achieved within electronics in general and in micro-electronics in particular. The topic of interconnection is broken down into several aspects. Starting from the mechanical carrying structures, the substrates, the subject is shifted to the fabrication of routing layers on top of these substrates, and finally, assembly technologies are described for mounting components on those patterned substrates. If the first two chapters can be considered as a theoretical background based mostly on a study of the available literature[7], Chapters 3 and 4 are intended as elaborated examples of actual display assembly, of which some are more elaborated than others. Chapter 3 illustrates the rigid display assemblies, mainly interconnecting an electronic interface to glass-based displays, while Chapter 4 focuses on examples of technologies for assembly of electronics on flexible substrates, that might be suitable for flexible display applications. At this point, it becomes clear that the flexibility of any flexible display with current technologies is hampered significantly by the rigidity of the driving electronics, and the interconnection in between such a display and its driving electronics. The underlying issues are brought up in Chapter 5, as well as some possible solutions, so as to further advance display technology development. Next to the more obvious possibilities, incorporating flexible substrates for the driving electronics, switching to one-sided interconnection and reinforcing the more fragile interconnection areas, embedding is proposed as a more radical solution towards fully integrated flexibility. This is definitely one of the more complex possibilities, but at the same time an innovative route towards electronic system integration and the current hype in microelectronics of what is nowadays referred to as 3D-packaging. Amongst others the principle of Ultra Thin Chip Packaging (UTCP) is introduced as an interesting embedding option. In this option, the chip is thinned down and embedded in a flexible substrate. This then culminates in Chapter 6 elaborating one possible UTCP variant, the so-called flat UTCP tech-

[7] although some hands-on experiments are also included

nology, whereby the thin chip is embedded in a flat and symmetrical sandwich of polyimide layers. The process flow is described and the results are characterized, together with some important design and fabrication issues. As UTCP technologies have only recently been developed, and are currently on the brink of emerging, Chapter 6 also gives some possible optimizations and improvements for the flat UTCP technology, as well as some promising trials indicating the next steps and an outlook on what implications this technology might have in the future of displays.

After the final technical chapter, I end with a sort of postscript chapter, where I first give a brief overview in retrospection of the achievements made as part of this doctoral research. Then, I try to fit the research described in this book in a wider frame, since many of the topics here can obviously be used in a wide range of applications within the field of micro-electronics interconnection. Lastly, a summary illustrates how the achieved results were made available to the research community, mainly the display and packaging societies, mostly through newsletters, theses, articles and conferences[8].

Finally, and perhaps most importantly, I hope you enjoy leafing through, if not reading, this book as much as I enjoyed finishing it...

Happy reading,
Jonathan

[8] apart from this doctoral thesis, of course

1
Introduction to Displays

"pixel: A mischievous, magical spirit associated with screen displays. The computer industry has frequently borrowed from mythology: witness the sprites in computer graphics, the demons in artificial intelligence, and the trolls in the marketing department."

— Jeff Meyer

A display device is an output device for the presentation of information for visual or tactile reception, acquired, stored, or transmitted in various forms [1]. An etymology search quickly teaches that the word originates from the latin verb "displicare", meaning "to unfold". It is used later on, in the 14^{th} century, in the meaning of "reveal/exhibit", with regards to sails and flags, showing that it is unconnected with -play, but instead is derived from -ply, or fold [2].

All the same, in the modern world, this is a very, nearly uncomfortably wide definition, as practically anything can in this way be considered as a display. Nowadays however, and more practical, the term is used as abbreviation for electronic display, where the input is supplied as an electrical signal. These signals are generated by electronic circuitry, the so-called driving electronics. The whole system, incorporating the display and its driving electronics in a casing, is often referred to as a monitor.

Displays, and monitors, are all around us, from the most high-tech to the most basic human environment, and the rapid technological progress in the last fifty years would have been unthinkable without them. The first major and worldwide

breakthrough for electronic displays was obviously due to the gaining popularity of television but display presence in everyday-life has only continued to grow since then. Some of the more obvious examples are displays being used in public advertising and signage and of course cellphones and computer screens. Their increasingly important part in modern-day life can be mostly attributed to the technological advancements that have been made and are still being made in the display manufacturing area. Starting from rather bulky monitors, with relatively limited display area and resolution, in the first PCs and television sets, numerous developments transformed these in much thinner, sleek flat panel displays of possibly enormous sizes with very high definition resolutions. Also the improvements in compactness, lightness and power consumption allowed for several mobile "killer" applications, e.g. watches, portable music players, cellphones and GPS devices.

In this chapter, first a standard display buildup is discussed. After this, the most common display technologies are briefly discussed, explaining their working principle and most important features. Then, the methods for driving a display are discussed, and finally the importance of the choice of display substrate is brought up.

1.1 Display Buildup

References: [1]

A standard display module assembly, or rather disassembly in this case, is illustrated by the pictures in Figure 1.1. This laptop screen shows the display itself, and the interconnection mechanism with the driving electronics that is the display interface. A display module can thus be broken down into several aspects. First there is the display effect, the visible aspect of the display. Second the backplane technology, with or without integrated transistors, forms the addressing/interconnection layer, and delivers the electrical signals for exciting the display effect. Finally, an interface for the user is provided by the driving electronics.

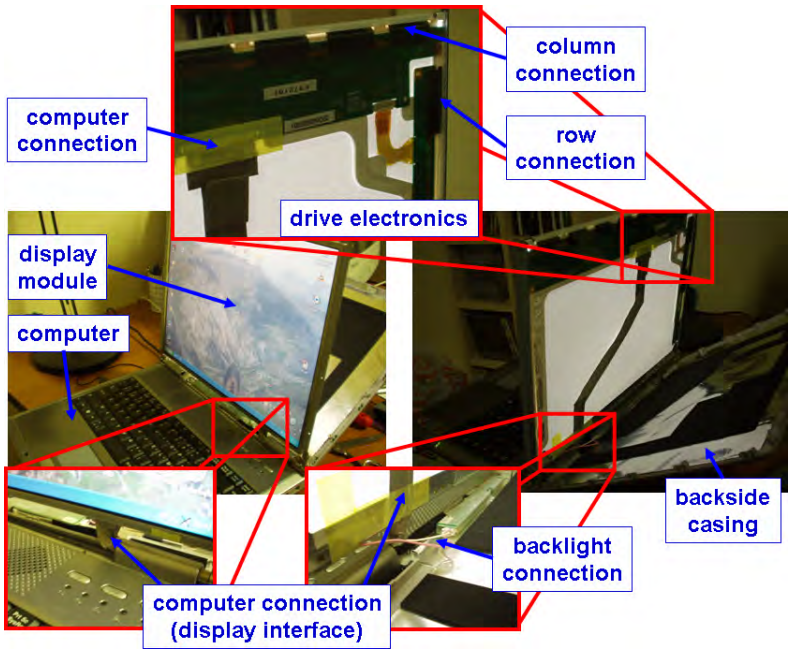

Figure 1.1: A disassembly of a laptop reveals the display module and its interconnection mechanism: the driving electronics are integrated at the back of the display (on top of the backlight), the display interface is connected to the computer by a single wiring foil

Manufacturing displays is a complex business, and a lot of different aspects have to be considered before, during and after fabrication. Each display consists of several (from a basic few up to millions) pixels or segments, that each can be individually programmed to be on, off or partly on (so-called grayscales). The physical mechanism on which this activation relies, is called the "display effect", and the programming of the pixel is referred to as "driving" a pixel (also used for a complete display). All technologies described below, except for one, are flat-panel technologies, and are based on material being contained in-between two electrodes. It is this material that is responsible for the display effect, generating light (in emissive displays), or modulating incoming light (in transmissive, reflective and transflective displays) that is externally generated (sun, backlight,...).

The term "pixel" itself is short for "PICture ELement" and is commonly used to represent the smallest component in the image on the display, although the term subpixel is often used in the case of color displays. A segment is basically the name given to a large pixel. With this in mind, pixels are commonly arranged in a matrix with rows and columns, while the term "segment" is more often used when each pixel is driven individually. This is illustrated in Figure 1.2. Depending on the arrangement, the display is active- or passive-matrix-driven, in case of rows

and columns, or directly driven in the case of segment displays.

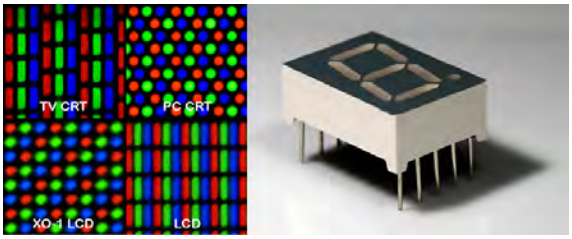

Figure 1.2: Pixel geometry of various CRT and LCD displays (left), and a typical 7-segment LED display component, with decimal point (right)

1.2 Display Effect Technologies

1.2.1 Electromechanical Technologies

References: [1]

The idea behind this kind of display, a very basic one, was used early on in many game shows, as large-scale puzzle-boards, probably the most famous being the one used in "The Wheel of Fortune". While initially being operated manually, this type of display was soon developed further to more advanced, electrically-driven devices. Today, two types of such displays are often found in train stations and airports, where they typically display departure and/or arrival information, split-flap displays and flip-dot displays. Some pictures illustrate the principles in Figure 1.3.

Figure 1.3: (a) an early "mechanical" display, (b) a picture of a split-flap display and (c) a drawing showing the principle, (d) a flip-dot display

In split-flap displays, each character position or graphic position has a collection of flaps on which the characters or graphics are painted. These flaps are precisely rotated to show the desired character or graphic. Sometimes the flaps are large and display whole words, and in other installations there are several smaller flaps, each displaying a single character. The former method is of course limited on the words it can display by what is on the flaps, whereas the latter system is not and output messages can be changed without the need for the addition or replacement of flaps, although images cannot.

As for flip-dot displays, they consist of a matrix of dots, each of which can be flipped to show either the colored or black side. The colored side is used to form characters. Once flipped, the disks stay in that state and no further power is needed to maintain it.

The advantages of these kinds of displays are, from an optical point-of-view, high visibility and wide viewing angle in most lighting conditions and electrically, they consume little or no power while the display remains static, as well as fault-tolerance during a power loss or disruption, meaning that the display will not normally reset. Another significant attribute is the distinct sound that draws attention to the board when the information is updated. Drawbacks include the maintenance needed for the moving parts, the low refresh rate and the limited display content, as compared to the size.

In this thesis, electromechanical displays will not be discussed further. Instead, the emphasis will be put on displays with display effects where the output is not dictated by mechanical movement, but rather technologies that are suitable for flat panel fabrication. This choice is made to enhance the possibilities for advancing the current displays towards lighter and more flexible ones.

1.2.2 Cathode Ray Tube (CRT) Technologies

References: [1]

The cathode ray tube (CRT) is basically an evacuated glass envelope containing an electron gun and a fluorescent screen and is the only non-flat-panel display technology described in this book. The electrons in the electron beam coming from the electron gun are accelerated and deflected, and when they strike the fluorescent screen, light is emitted. Modulation and deflection of the electron beam produces an image on the display. The principle is illustrated in Figure 1.4.

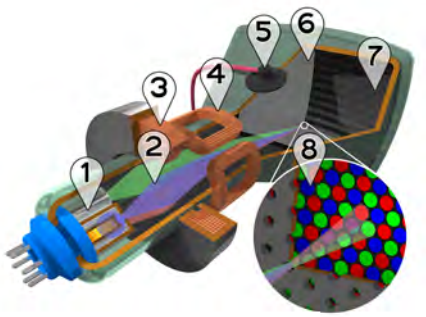

Figure 1.4: Principle of a color CRT: ***(1)*** *Electron guns* ***(2)*** *Electron beams* ***(3)*** *Focusing coils* ***(4)*** *Deflection coils* ***(5)*** *Anode connection* ***(6)*** *Mask for separating beams for red, green, and blue part of displayed image* ***(7)*** *Phosphor layer with red, green, and blue zones* ***(8)*** *Close-up of the phosphor-coated inner side of the screen*

CRTs, described as such, are retreating with the advance of flat panel displays, because they are large, deep, heavy, and relatively fragile due to the large glass envelope. However, several efforts have been made to upgrade CRT technologies: an early attempt was made in 1982 by Sony with flat CRTs in the Watchman series, and more recently, flat panel displays based on the CRT principle are making their appearance. A sort of micro-CRT, they are called field emission displays (FED), and they rely on the cold emission of electrons by various types of cathodes, ranging from matrix arrays of metal or silicon microtips, over carbon nanotubes to even a thin film diamond layer. Several variations (each with its own name) of this technology are under development at different companies: FED (Field Emission Display, Sony), SED (Surface-Conduction Electron-emitter Display, Canon), NED (Nano-Emissive Display, Motorola),... Some examples are shown in Figure 1.5.

Figure 1.5: "Advanced" CRT technologies: flat CRTs by Sony (left) and an SED by Canon (right)

1.2.3 Liquid Crystal (LC) Technologies

References: [1], [3], [4]

A liquid crystal technology typically consists of a layer of molecules aligned between two transparent electrodes, and two polarizing filters, with axes of transmission (in most of the cases) perpendicular to each other. With no liquid crystal between the polarizing filters, light passing through the first filter is blocked by the second (crossed) polarizer. The surface of the electrodes that are in contact with the liquid crystal material are treated so as to align the liquid crystal molecules in a particular direction. This treatment typically consists of a thin polymer layer that is unidirectionally rubbed using, for example, a cloth. The direction of the liquid crystal alignment is then defined by the direction of rubbing. Because the liquid crystal material is birefringent, light passing through one polarizing filter is rotated by the liquid crystal helix as it passes through the liquid crystal layer (it is said that the liquid crystal is twisted), allowing it to pass through the second polarized filter, and the structure appears transparent. Half of the incident light is absorbed by the first polarizing filter, but otherwise the entire assembly is transparent. When a voltage is applied across the electrodes, the liquid crystal molecules "untwist" and the polarization of the incident light is not rotated, so that the light is blocked by the second polarized filter and the assembly appears black. This mechanism is illustrated in Figure 1.6.

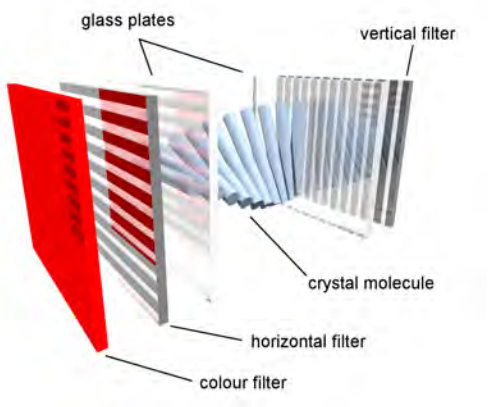

Figure 1.6: Working principle of liquid crystal technology

Liquid crystal displays (LCDs) are thus far the most successful in replacing CRT displays. Several variations of LCD technology have already entered the market: twisted nematic (TN), in-plane switching (IPS), vertical alignment (VA), polymer dispersed liquid crystal (PDLC) as well as several bistable technologies (zenithal bistable, cholesteric bistable,...). Bistability means that the technology has two stable states. Once a stable state is selected, by applying the right elec-

trical pulse, the device will remain in that state "forever" without consuming any additional power. Because of this property, such displays are often referred to as zero-power displays, or ePaper, short for electronic paper, see further on in Section 1.2.5.

1.2.4 Electroluminescent (EL) Technologies

References: [1], [5], [6]

Electroluminescence is the production of visible light by a substance exposed to an electric field without thermal energy generation, as opposed to incandescence. Usually, certainly in the case of displays the substance is a semiconductor, with one of the better known devices relying on this principle being LEDs, or light emitting diodes. These LEDs can be separately fabricated and assembled together, each LED representing a pixel. This is a common practice for large outdoor advertising displays (scoreboard, billboards, even giant outdoor TVs,...). Another, more advanced technology involves depositing the required thin film stack directly on the display substrate, obviously allowing finer features, and thus a far higher pixel density, than the above separate-LED approach. Recent developments within electroluminescent technology include blue, red and green emitting materials that offer the potential for long life and full color electroluminescent displays, as well as organic materials suitable for electroluminescent display (OLED displays), offering significant processing advantages[1] over the initial inorganic materials. An important advantage of electroluminescent technologies is that these produce emissive displays. A picture of a very recent OLED display is given in Figure 1.7.

Figure 1.7: The latest OLED display (Sony): very thin and with exceptional image quality

1.2.5 Electrophoretic Technologies

References: [1], [7]

[1] printing techniques can replace expensive vacuum thin film deposition techniques

Generally, electrophoresis is the motion of dispersed particles relative to a fluid under the influence of an electric field. Its most known and widespread application is in the field of molecular biology, where it serves for, amongst others, DNA analysis. In displays, the mechanism is exploited to arrange charged pigment particles in a liquid, by applying an electric field. The principle is illustrated in Figure 1.8.

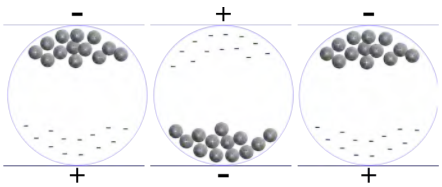

Figure 1.8: Principle of an electrophoretic display

In the simplest implementation of an electrophoretic display, titanium dioxide particles approximately 1 μm in diameter are dispersed in a hydrocarbon oil. A dark-colored dye is also added to the oil, along with surfactants and charging agents that cause the particles to take on an electric charge. This mixture is placed between two parallel, conductive plates separated by a gap of 10 to 100 μm. When a voltage is applied across the two plates, the particles will migrate electrophoretically to the plate bearing the opposite charge from that on the particles. When the particles are located at the front (viewing) side of the display, it appears white, because light is scattered back to the viewer by the high-index titanium particles. When the particles are located at the rear side of the display, it appears dark, because the incident light is absorbed by the colored dye. If the rear electrode is divided into a number of small picture elements (pixels), then an image can be formed by applying the appropriate voltage to each region of the display to create a pattern of reflecting and absorbing regions.

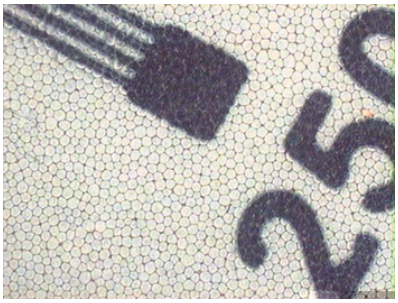

Figure 1.9: Close-up of an electrophoretic display

Electrophoretic displays are considered prime examples of the electronic paper category, because of their paper-like appearance and low power consumption,

thanks to their bistability. This is a promising technology, with already some consumer products available and under development, as shown in Figure 1.10.

Figure 1.10: Electrophoretic displays: a rigid eReader, already commercially available (left, IREX Technologies), and a flexible variant under development (right, Plastic Logic)

1.2.6 Plasma Technologies

References: [1]

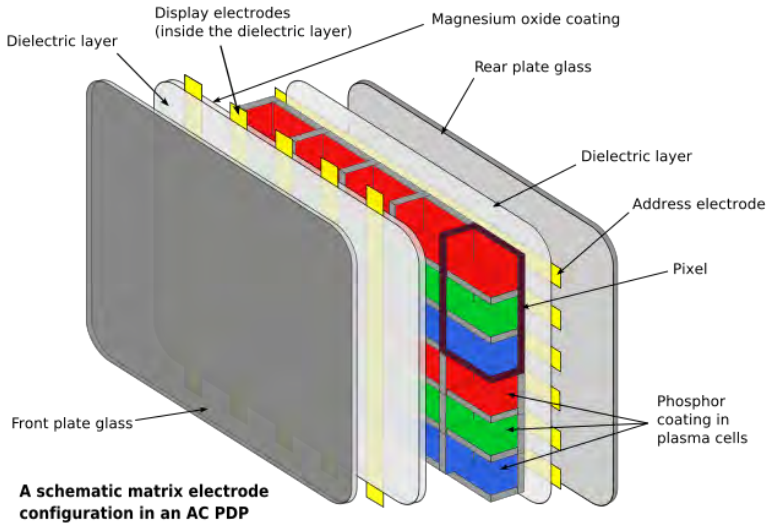

Figure 1.11: Composition of plasma display panel (PDP)

Plasma display panels (PDPs), another type of flat panel display, are now commonly used for large TV displays. Many tiny cells located between two panels of

glass hold an inert mixture of noble gases (neon and xenon). The gas in the cells is electrically turned into a plasma which then excites phosphors to emit light. The concept is shown in Figure 1.11.

The main advantage of plasma display technology is that a very wide screen can be produced using extremely thin layers. Since each pixel is lit individually, the image is very bright and has a wide viewing angle.

1.2.7 Electrochromic Technologies

References: [1], [7]

Electrochromism is the phenomenon displayed by some chemicals of reversibly changing color when a burst of charge is applied. As the color change is persistent and energy need only be applied to effect a change, electrochromic materials are sometimes used to control the amount of light and heat allowed to pass through windows ("smart windows"). The technology of an electrochromic cell is very similar to the LCD technology: the electrochromic material is sandwiched in between two transparent electrodes. The colouring of the electrochromic material results from changing the potential of the cell by charging the electrodes. Figure 1.12 gives an idea of the technology and the display effect.

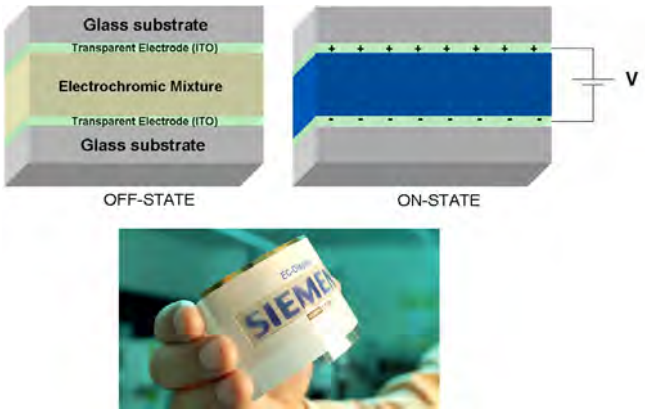

Figure 1.12: The electrochromic principle and an example of a display based on this principle (Siemens)

1.2.8 Electrowetting Technologies

References: [1], [8], [9], [10], [11]

The electrowetting effect is originally defined as "the change in solid electrolyte contact angle due to an applied potential difference between the solid and the electrolyte". In other words, with electrowetting a voltage is used to modify the

wetting properties of a solid material. The principle of such increased wettability is illustrated in Figure 1.13. A company involved in manufacturing electrowetting displays, is Liquavista. An example of what they make is shown in Figure 1.14.

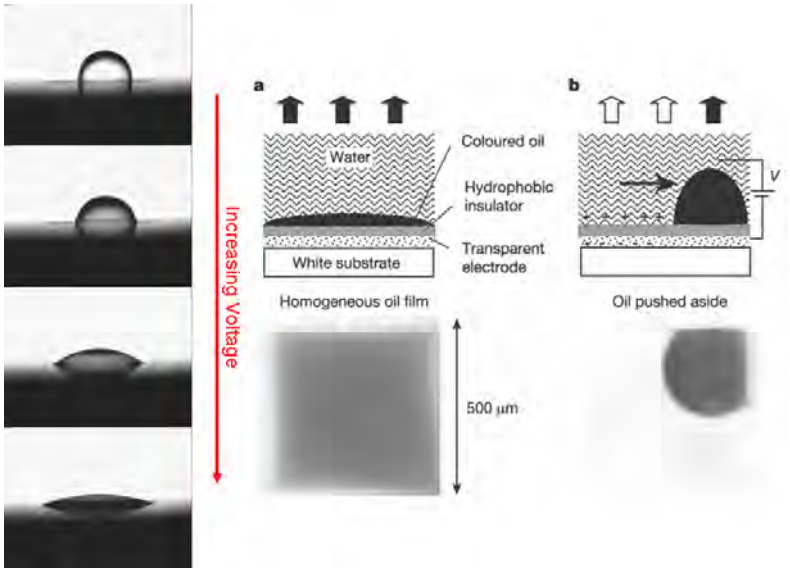

Figure 1.13: The principle of electrowetting illustrated (Liquavista): no voltage applied, therefore a coloured homogeneous oil film is present (a), DC voltage applied, causing the oil film to contract (b)

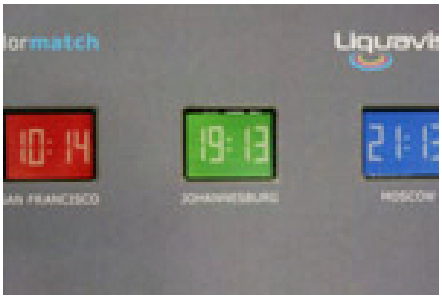

Figure 1.14: Some electrowetting displays (Liquavista)

1.2.9 Projection Technologies

References: [1], [12], [13], [14]

A completely different type of display can be fabricated by projection technologies. For completeness' sake, this type is added here, but not too much elab-

orated. The reason for this is that it is not a real display technology in itself[2]: the image is generated with one of the above display effect technologies and is subsequently, optically projected (mostly enlarged) on a separate surface. In this sense, these are rather optical technologies, requiring the handling and processing of light, than actual display effects.

The most common type of projectors are CRT, DLP, LCD and LCoS, abbreviations for Cathode Ray Tube, Digital Light Processing, Liquid Crystal Displays and Liquid Crystal on Silicon. Two of the four types, namely CRT and LCD, have already been explained in the above sections, and LCoS another type of Liquid Crystal technology (but directly with a silicon chip as backplane), only DLP requires a little more clarification.

In DLP projectors, the image is created by microscopically small mirrors laid out in a matrix on a semiconductor chip, known as a Digital Micromirror Device (DMD). Each mirror represents one or more pixels in the projected image. These mirrors can be repositioned rapidly to reflect light either through the lens or on to a heatsink, and this effect can in fact therefore be considered an electromechanical technology, Section 1.2.1. Figure 1.15 illustrates two types of microdisplay technologies used in projection technologies.

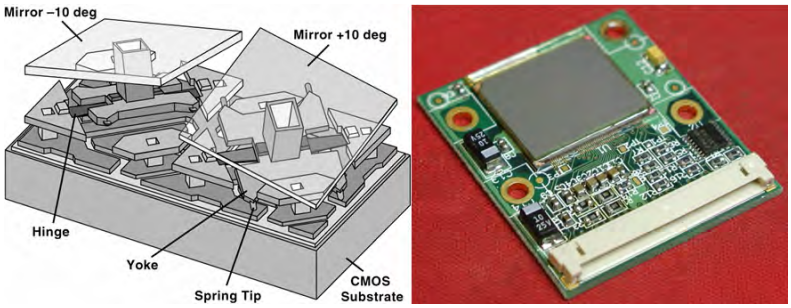

Figure 1.15: A schematic of a Digital Micromirror Device (left, Texas Instruments), and a microdisplay built with LCoS technology (right, TFCG Microsystems)

Advanced projector systems can provide images in focus on curved screens. One example is shown in Figure 1.16, where the $19,995 computer display, developed by the Elumens Corporation, introduces a sense of immersive 3D-viewing.

[2]except for DLP, see further on

Figure 1.16: The VisionStation (Elumens corp.) introduces 3D-vision by projecting the image on a parabolic screen

1.2.10 Comparison of Technologies

References: [1], [15], [16], [17], [18], [19], [20]

In this section, it should be clear that the comparison is made based on the current, publicly available state-of-the-art of each technology. This is an extremely important point to make, since most of the technologies here are constantly being revised and upgraded, so under ongoing development. Moreover, the degree of maturity is not the same for all technologies, both in the development and in the market stage. It is therefore, highly likely that this comparison may not be valid anymore within even only a few years' time...

To fairly compare different display effect technologies, a lot of properties have to be taken into account. Moreover, it is difficult to classify these properties into separate categories, as they can, more often than not, be interlinked to several of these categories. In spite of this, to keep it at least somewhat compact and easy to overlook, I distinguished three types of properties -and I take full responsibility for slightly abusing the terms in what follows-: optical, electrical and physical.

Basically, the purpose of a display is to show something, so in this view, the optical properties are most important. However, electrical behaviour is not to be neglected either, as the display should be able to change image content in a convenient -read: adequately fast and with limited energy resources- way. Finally, physical properties are definitely worth considering, as displays are meant to be a practical tool for a real-world environment...

1.2.10.1 Optical Properties

Brightness is by definition the perception elicited by the luminance of a visual target, and is therefore a subjective property. In displays however, this term is used as a substitute for luminance, the photometric measure of the density of luminous intensity in a given direction, expressed in candela per square meter. Although brightness measurements are by default only applicable for emissive technologies, they are also considered for LCDs, where a light source is incorporated at the back of the display (which is why it is called a backlight). Presently, PDPs are generally brighter, followed by DLP, then CRTs, LCDs and finally OLEDs.

The contrast ratio expresses the difference in brightness between the "on" state of a pixel and its "off" state. It is typically given as e.g. 100:1, meaning the pixel is 100 times brighter "on" than "off". This is illustrated in Figure 1.17. A standard way to measure display contrast is to use a black-and-white checkerboard test pattern and measure the luminance at the center of the white blocks and then the black blocks. The smaller the blocks, the greater the bleed, resulting in lower contrast values. This illustrates the "trickiness" of such measurements, resulting in discussions wherever technologies are under comparison. On average, it seems that PDP achieves the highest contrast ratios, then LCD, DLP, CRT, OLED and lastly electronic paper technologies.

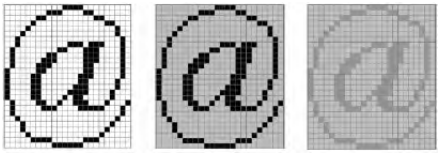

Figure 1.17: Illustrating the contrast ratio

Display resolution is commonly used to communicate the number of pixels, as opposed to optical resolution, making it a somewhat misleading term. Pixel pitch, the distance between the center of two neighbouring pixels, or the period of the pixel pattern, on the other hand is more related to the optical resolution. From these properties, the display area can be derived. The influence of these properties on the displayed image quality is illustrated in Figure 1.18. Display resolutions is generally highest for LCD and DLP, followed by CRT, PDP, electronic paper and OLED. Pixel pitch on the other hand is minimal for PDP, then electronic paper, OLED, CRT, LCD and DLP.

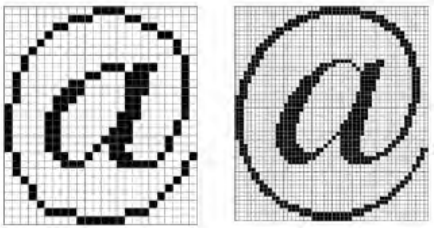

Figure 1.18: Influence of the display resolution on the image quality

Light transmission mode of the display is another important factor to consider. The display effect can be emissive, transmissive (requiring a light source behind the display), reflective (manipulating incident light shining on the front of the display), or a combination of the above. An emissive technology generates light (photons) of its own. This is the case for CRTs, electroluminescent technologies and PDPs. Reflective displays manipulate incident light shining on the front of the display. Examples are electrophoretic, electrochromic and electrowetting technologies. Transmissive technologies require a light source behind the display, and therefore the display material must be transparent at some point (either in the "off" state or in its "on" state). This is the case for LCDs. Reflective and transmissive LCDs, as well as the transflective hybrid are schematically given in Figure 1.19.

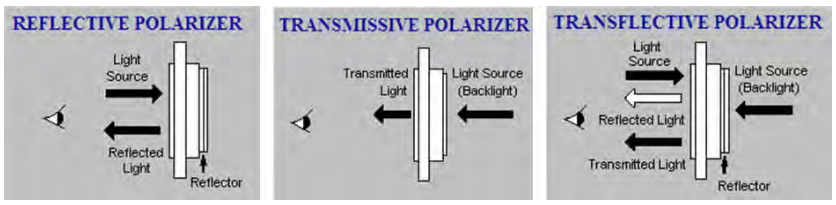

Figure 1.19: Light transmission modes for LCDs

The light transmission mode can have a huge influence on the viewability of the display, and should be considered carefully depending on the operating conditions. Another important property in this sense is the viewing angle. This is the angle at which the image quality of a displayed image degrades and becomes unacceptable for the intended application. As the observer physically moves to the sides of the LCD, the images on an LCD degrade in three ways. First, the luminance (brightness) drops. Second, the contrast ratio usually drops off at large angles. Third, the colors may shift. These phenomena are illustrated in Figure 1.20, by the company i-Tech, that, amongst others, integrates LCD panels, offering active and passive enhancements.

Figure 1.20: Viewability issues on LCDs: outdoor conditions and wide viewing angles pose problems for standard LCDs (left-sided displays), but can be passively and/or actively enhanced (right-sided displays)

In general, reflective and emissive displays have wider viewing angles as compared to transmissive displays, and reflective displays are better suited for outdoor (in the meaning of abundant ambient light) applications.

1.2.10.2 Electrical Properties

Considering electrical properties, the most important must be the power consumption, closely connected with output efficiency, and the response time.

Regarding power consumption in televisions, it seems that a lot of factors, next to the obvious display size, have to be taken into account to make a fair comparison: the brightness setting of course plays an important role, display content, driving electronics hardware and software, so-called phantom or standby power, measuring equipment,... On average, and worth mentioning is that there are several exceptions (to the more greedy displays as well as to the more power-efficient assemblies), the microdisplay rear-projector based TV is most power-efficient (0.14 watts per square inch), as compared to LCD (0.29), DLP, plasma (0.35) and CRT (0.54). OLED technology, although still in development for larger display sizes, promises even considerably lower consumption rates, due to its emissive character as compared to LCD technology, where a backlight is constantly on and the light output is modulated in intensity by the liquid crystal.

Power consumption is still drastically lower in the bistable electronic paper technologies, as there is only power consumed when the content is altered. At this point however, they unfortunately cannot compete with the other technologies in the TV industry, because they lack the fast refresh rates needed for video applications[3]. Response time is defined as the time required for an LCD pixel to change from fully active (black) to fully inactive (white), then back to fully active again. The response times are generally lowest for DLP and OLED, followed by PDP, CRT, LCD and lagging behind is electronic paper.

[3] although e.g. E-Ink is eagerly trying to overcome this disadvantage

1.2.10.3 Physical Properties

The first physical properties that leap to mind are dimensions and weight. Flat panel displays (FPDs) as LCDs, PDPs, OLEDs and electronic paper are of course, by definition, much thinner and, for comparable display size, therefore also much lighter. DLP technologies use a projector, which means the weight stays the same, independent of the image size projected. In absolute dimensions, the largest images are generally generated by projectors (DLP), then PDP, LCD, CRT, electronic paper and OLED. A comparison of display thickness in between the FPD technologies is rather irrelevant, as the thickness is mostly defined by the substrates at present, and all of the mentioned technologies are working toward thinner, flexible substrates.

Lifetime of a display is evidently important for commercial applications, where demonstration of the technology for just a few days or weeks is commonly not perceived as satisfactory, as opposed to research and development demonstrators. It is standardly indicated by the display's "half life" in operational hours, meaning that after that time it will emit 50% of its initial brightness. This property depends on the ruggedness of the display effect, the effectiveness of barrier layers shielding it from the outside environment, and the use of the display[4], resulting again in a highly complex property to compare. Worth mentioning though, are two phenomena: burn-in, and the isotropic stage in liquid crystal displays. Burn-in, also referred to as permanent image retention, is an effect of an after-image appearing on the screen after a still picture is displayed for an extended period of time. It is attributed to uneven wear of the phosphors in the display, affecting CRT and plasma displays alike. Screensavers derive their name from their original purpose, which was an active method of attempting to prevent screen burn-in: by ensuring that no pixel is left displaying a static image for extended periods of time, phosphor luminosity is preserved. The isotropic stage in liquid crystal is the point where the fluid heats or cools to where it is no longer in the twisted nematic state. Since the molecules can no longer twist light, all incoming light is absorbed. The phenomena are illustrated in Figure 1.21.

[4] both physical and electrical (mis)use

Figure 1.21: Illustrations of lifetime-limiting phenomena: phosphor burn-in, where an image is retained even when the display is off (left), and the isotropic stage, damaging liquid crystal so that the display effect is lost (right)

As for lifespan comparison, an overall estimation[5] could be that LCD is best, followed by DLP, PDP, CRT, electronic paper and OLED.

Finally, although not truly a physical property, it is impossible to avoid cost as it remains an, if not *thé* most important factor in deciding which display to choose. Heavily reliant on several aspects not directly linked with the technology itself (market demand, history and maturity of the technology, worldwide processing capacity,...), a possible current cost comparison could be that cheapest is still CRT, then LCD, electronic paper, DLP, OLED and PDP.

1.2.10.4 Overall

Unfortunately, this is a section that might leave you, understandably, with an unsatisfied feeling, because I feel an overall comparison is too complicated. Even a minutely considered objective comparison would probably not do justice to all the technologies, as each has its own advantages and any deliberation that can be made would depend highly on the application in mind. Therefore any such comparison would be influenced by the angle-of-viewing and the objectiveness would be lost.

1.3 Driving Methods

1.3.1 Scanning Technology

References: [1]

CRT display development is slowly being disbanded, partially due to reasons already explained in Sections 1.2.2 and 1.2.10[6], but also due the driving principle

[5] again, probably including quite some flaws and exceptions
[6] mainly their bulkiness, fragility and power greediness

around which CRTs have been built. The driving principle for CRTs uses scanning technology, explained in Section 1.2.2 and adequately illustrated by Figure 1.4. The main drawback of the scanning technology, is that it unavoidably suffers from flickering, causing eye strain and fatigue. Another considerable disadvantage of the electron beam scanning the display from afar, is its susceptibility to electromagnetic fields. This effect is especially important for military applications, but also has a broader impact, illustrated by the fact that degaussing (or demagnetizing) was developed and introduced in commercial products to counter the effect of the earth's magnetic field.

Due to the declining presence of CRTs, the driving methods discussed in the following sections, as well as the subsequent comparison, are focused on the flat panel driving methods.

1.3.2 Segment Driving

References: [1], [21], [22], [23]

Here, the principle is kept as basic as possible: each segment is individually addressed and driven, with a dedicated interconnection line to supply the segment with the required electrical input. This driving method is also referred to as "direct drive". In its most straightforward configuration, called static driving, the counterelectrode (the electrode on the frontpanel of the display) is shared by all segments, and the segments are basically driven by applying the required electrical signals to the electrodes. This means the number of needed contacts equals the number of segments plus one for the counterelectrode[7].

Figure 1.22 shows a typical segmented display together with the static driving waveforms for the segments. Note that the waveforms here ensure that the voltage over the segments is reversed periodically, so that the net applied voltage is zero. This is required for the liquid crystal material, to prevent it getting damaged. Furthermore, I'd like to stress that this is an example for LCDs, which are voltage driven, but a similar setup with currents instead of voltages is possible, and necessary for some other technologies, e.g. OLED.

[7] this electrode is sometimes referred to as COM, short for the common line, or BP, short for backplane

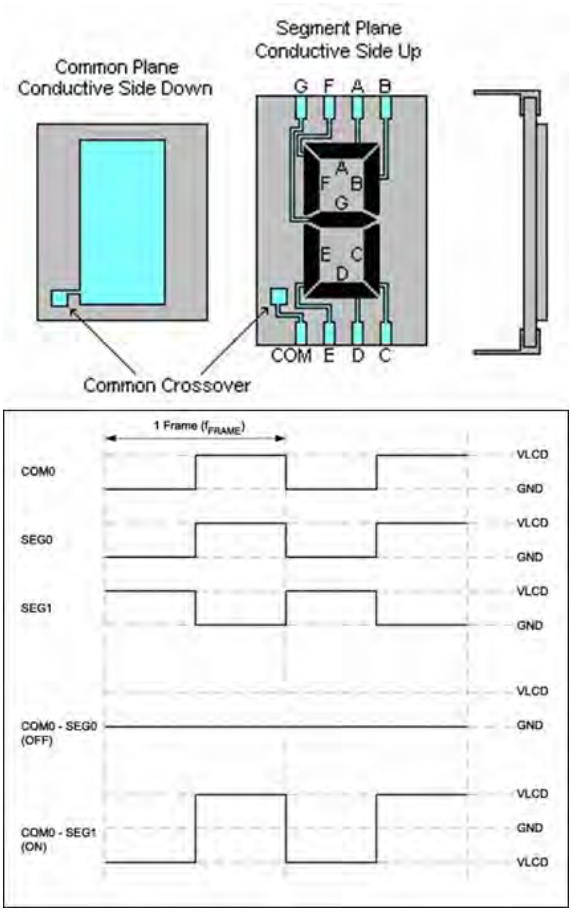

Figure 1.22: Implementation and waveforms for a static LCD

1.3.3 Passive-Matrix Driving

References: [1], [24], [23] , [15]

To lower the number of contacts, it is sometimes preferred to use a multiplexed driving method, where several common planes are divided over the total number of segments. This method encompasses time division multiplexing (TDM) with the number of time divisions equal to the number of common planes used in a given display buildup. An example of how this is an extension of the static driving method is shown in Figure 1.23. Note that, again, the waveforms given here are adapted to LCDs, their net voltages being zero.

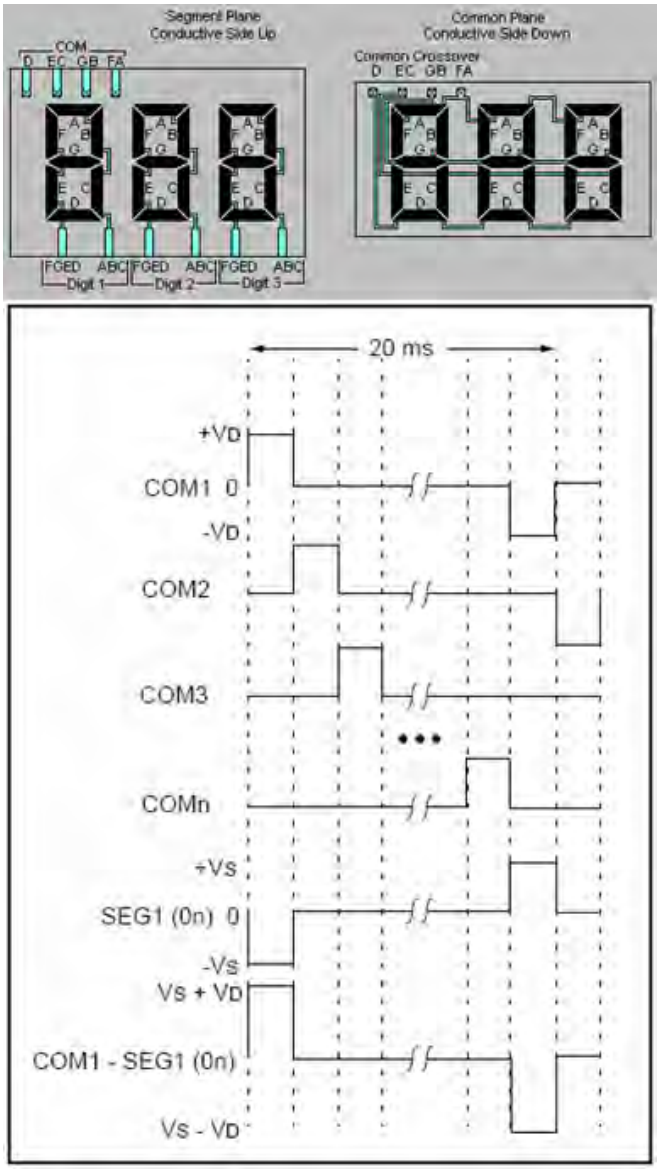

Figure 1.23: Implementation and waveforms for a multiplexed LCD

A better illustration of this technique, as well as more general, is given in Figure 1.24. At the same time, this effectively introduces “rows” and “columns” instead of “segments” and “commons”, illustrating why the term passive matrix is

an obvious choice for this type of driving[8].

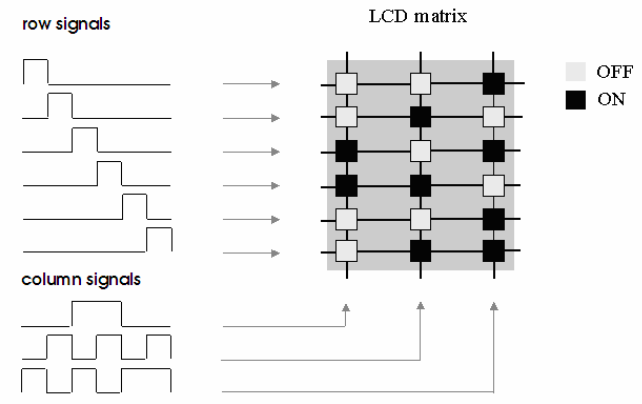

Figure 1.24: Principle of a passive-matrix driven display

1.3.4 Active-Matrix Driving

References: [1], [25]

Although they have a similar working principle of providing electrical signals to the pixels through row and column conductors, the important difference between active and passive matrix is that active displays have a transistor and a storage capacitor built into each pixel. This explains why, in the case of flat panel displays, active matrix is practically synonymous with TFT, short for thin film transistor. Schematically, an active matrix display can be represented as in Figure 1.25. For obvious reasons, the terminology slightly changes from "row" to "gate" and similarly from "column" to "source".

[8]at least the "matrix" part, the reason it is called "passive", is as opposed to active and should become clear in Section 1.3.4

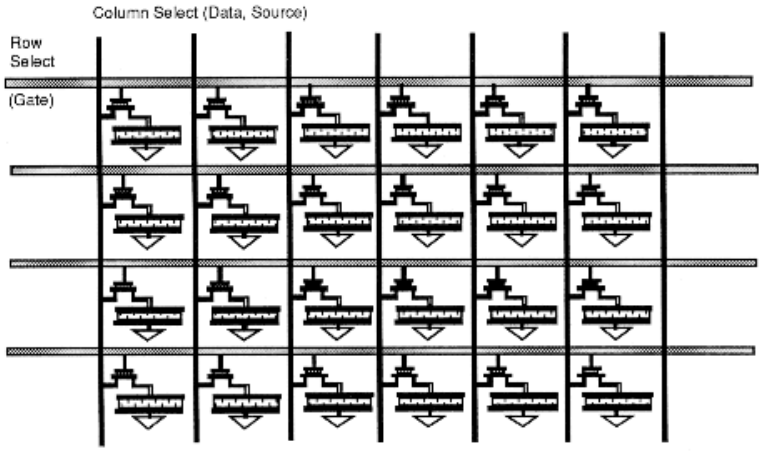

Figure 1.25: Schematic of an active-matrix driven display

The transistor acts as a switch, the capacitor as a memory: when the row is selected (gate activated, channel turned on), the capacitor is charged through the appropriate column. When the whole row has been "written", the row is deselected, and the capacitors maintain a constant enough voltage for the display effect until the next refresh cycle. Again, in the case of current driven display effects, this principle can be somewhat adapted. For example active-matrix OLEDs generally use an additional transistor to generate a constant current out of the quasi-constant voltage supplied by the capacitor.

1.3.5 Comparison of Driving Methods

References: [1], [26]

Each of the driving methods mentioned here have their benefits as well as their disadvantages. As always, much depends on the application for which the display is intended.

Relatively, segment driving is the most straightforward method, as each pixel is driven independently and no other pixels have to be taken into account when generating a driving signal for this pixel. On the other hand, just because each pixel is individually supplied, interconnecting all the pixels with their respective signal-generating drivers grows somewhat more complicated with the number of pixels on the display: the number of contacts needed equals at least the number of pixels plus one.

In a passive-matrix format, it is rather the other way round: interconnection is much easier, with only as much contacts as the sum total of the numbers of rows

and columns, but generating the driving signals is a lot more complex. Moreover, there is a limitation on the numbers of rows and columns, depending on the technology: more rows and columns lead to a loss of contrast due to increased crosstalk between rows and columns. This mechanism and the implicit limitation has been described by Alt and Pleshko, as early as 1974. The crosstalk can physically be considered as the parasitic influence of electrical signals in the neighbouring lines on the display material.

The active-matrix method, as its passive predecessor, has the same advantage of minimal contacts, as well as its disadvantage of complexer signals, but minimises the crosstalk issues: only one line at a time is selected to be active, and during this interval where the data is written (read: storage capacitor is charged), all the other lines are rendered inactive, significantly lowering any chance on interference from the neighbouring lines.

Lastly, and probably not too hard to imagine, hybrids of these types are possible. One type worth mentioning here is a thin film diode (TFD) variant, mainly because it nicely represents a compromise in performance and cost between passive- and active-matrix design. This compromise is commonly encountered in electronics, and, I guess, in any other consumer-related business.

1.3.6 Driver chips

Considering the above sections, it can be derived that generating the signals for driving a display can range from very simple and straightforward, to very complex and the most challenging part of the display. This is influenced by several factors.

First of all, each display effect requires a dedicated driving waveform -either current or voltage. AC signals are in most cases preferred over DC, for reasons of lifetime, most display media are damaged when driven in the same direction for extended periods, and power consumption, as less power is needed when the pixel supply can be switched off for short periods (sufficiently short so that the human eye cannot notice the difference). Both the shape and the amplitude of the driving signal are important in this respect.

Next, the physical size of the display has to be considered, together with the number of pixels/segments and the metal and layout used for electrical interconnection. These aspects have an influence on how the driving signals are affected-before arriving at the intended pixel, in terms of crosstalk, electromagnetic interference, parasitic resistance, capacitance and induction.

Finally, also the driving method has obvious implications for the driving signals. A so-called driving scheme commonly describes the needed signals for passive- and active-matrix displays.

To generate these signals, driver chips are implemented. These convert the (relatively simple) input signals, describing the intended image for the display, to suitable driving signals for each pixel/segment. Physically, they are fabricated as integrated circuits (ICs), and are then either used as bare dies, or packaged before further assembly. Packages can be standard through-hole (pin) and surface-mount packages, but display drivers are commonly packaged using tape automated bonding (TAB), tape carrier packaging (TCP) or direct flip-chip (FC) bonding on flexible substrates. The use of flexible substrates here is sensible, because it allows a maximum display area, when the packaged drivers are folded to the back of the display, as shown in Figure 1.1. Examples of separate driver chips, bare dies as well as packaged ones, are given in Figure 1.26.

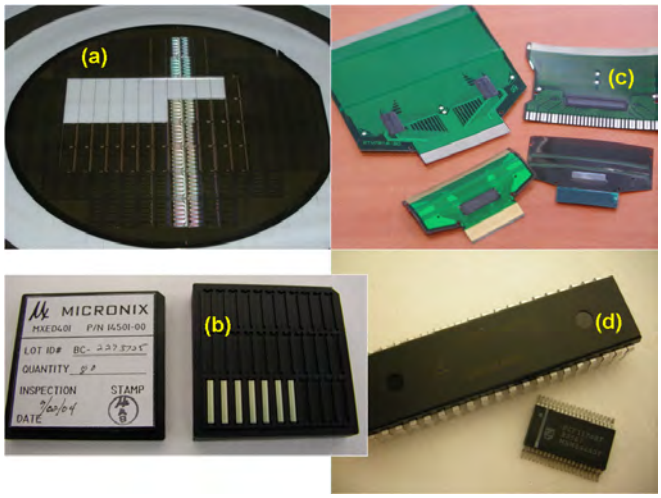

Figure 1.26: Examples of separate driver chips: (a) Mjöllnir (see further on in Section 3.4) bare dies for row driving diced on a wafertape, (b) bare die column drivers from Clare Micronix in a transport carrier, (c) driverchips from ST Microelectronics packaged as TCP, and (d) drivers in conventional through-hole and surface-mount packages

Nowadays, the input signals for the driver are commonly supplied by a microcontroller. This can be a separate package, but an interesting option is of course to embed the driving electronics on the supervising microcontroller chip. This increasing trend in integration minimizes interconnection, and the associated risks (yield), but on the downside, the microcontroller will be more application (display) specific, reducing its attractiveness for other applications, and testing will be more complex.

1.4 Substrates for Flat Panel Displays (FPDs)

The substrates used for manufacturing flat panel displays determine the final appearance and the processing window to a great extent. Of course at least one side of the display has to be visible, which implicates that for the technologies where the display medium is sandwiched in between two substrates[9], one substrate has to be transparent, but even with this restriction various types are still available.

1.4.1 Rigid Substrates

References: [1], [27], [28], [29], [30], [31], [32], [33], [34]

In the rigid type, glass is the most obvious choice. Next to its transparency, it has quite some interesting properties where processing is concerned: it is chemically inert, can withstand high temperatures and can be manufactured to be extremely flat. It also provides an effective barrier against environmental influences under operating conditions. On the downside, it is rather heavy and brittle, so relatively susceptible to breakage.

Silicon is used for a backplane as well, especially for microdisplays. This option offers an advantage over glass in the case of active-matrix displays, as the transistors can be fabricated directly in the silicon, whereas in the case of glass, a (thin film) semiconductor layer first has to be deposited (grown) onto the glass, resulting in thin film transistors (TFTs). These thin-film semiconductor layers are typically amorphous, microcrystalline or poly-silicon. Other materials exist, such as CdSe and ZnO, but are not too common. Increasingly organic materials are being used, resulting in organic TFTs.

Significant disadvantages of silicon as compared to glass is its cost and the smaller (wafer) size. As an illustration, Figure 1.27 shows that the evolution in glass sizes for LCD manufacturing, is proceeding to dimensions well over 2000 mm, with e.g. Corning recently announcing its plans to develop Gen 10 glass, measuring 2850 mm by 3050 mm, whereas for wafers 300 mm is standard nowadays, and 450 mm is still being heavily debated: major chip manufacturers want to proceed to 450 mm, equipment manufacturers seem somewhat reluctant; there is still a lot of discussion whether or not the switch is profitable at present. To show that price is a major factor, Table 1.1 gives some indicative values. Overall, in the third quarter of 2006, approximately 9.8 million square metres of LCD substrates were sold for around 833 million, as reported by DisplaySearch. According to Corning, a leading supplier of LCD glass, the glass accounts for less than 20% of the bill of materials for a regular 32” LCD TV.

[9] commonly the case for liquid crystal, electrophoretic, plasma, electrowetting and electrochromic displays

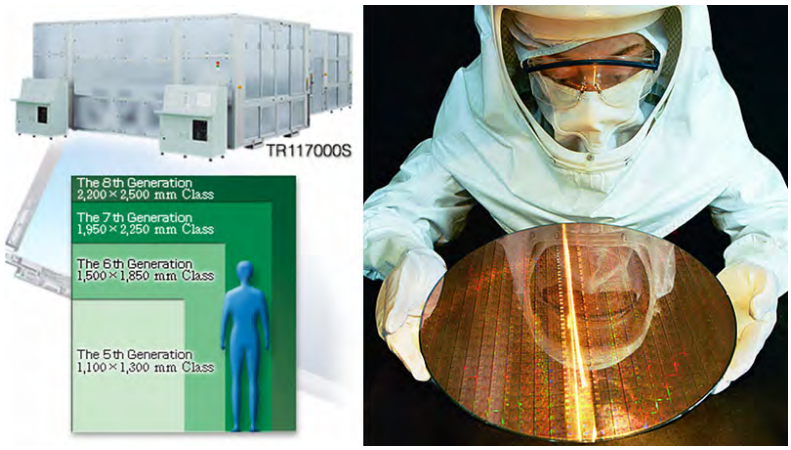

Figure 1.27: Illustration of the evolution in size: glass for LCD manufacturing (left, coating equipment TR117000S, Spinless) and maximal wafer sizes at present (right, Intel wafer)

Substrate	Cost [$]	Cost/Area [$/m^2]
200 mm Si wafer	45	1432
300 mm Si wafer	200	2829
9.8M m^2 LCD glass	833M	85

Table 1.1: Cost of some typical rigid display substrates (prices from the third quarter of 2006)

1.4.2 Flexible Substrates

References: [35]

Flexible type substrates offer some considerable advantages as compared to glass for display applications[10]. The thinness of the substrate usually results in a lower cost as well as reduced weight, and the nature of the materials commonly considered, lower the risk on breakage, as they are not as brittle as glass. Of course the flexibility also means that larger displays can be folded or rolled in smaller volumes. All these aspects lead flexible substrates to be favourable for wearable display applications.

Flexible substrates suitable for displays are mostly plastics, ranging from low-temperature PET, PES, PEN to high-quality PI (PolyImide) and PTFE (PolyTetraFluoroEthylene), but a noteworthy exception here is stainless steel. This last

[10]thin glass is also flexible but its fragility remains a major hurdle for processing and handling especially in the case of larger displays

material is considered a valuable alternative for plastics in applications where heat is generated excessively and has to be dissipated. Also, it is more robust (and therefore less flexible), which can be beneficial for certain applications.

The lower cost is accredited to several factors. First and foremost, a thinner substrate means less material is needed. Then, most plastics require low-temperature processes, lowering energy consumption. Finally, manufacturing methods might well prove more efficient in the long term for high volumes, if the batch processes for glass displays can be replaced by reel-to-reel-processing. Of course, initially massive capital investment is needed for adaptation of the processing equipment to flexible substrates.

Drawbacks of flexible substrates as compared to glass are linked with the benefits of glass: the chemical stability, the high-temperature capability and the barrier properties, and not to be forgotten the flatness, as flexible substrates often pose problems, in handling and in display applicationsdue to waviness and roughness, e.g. where spacers are necessary to ensure a uniformly thick layer of the display medium.

1.4.3 Next-Generation Substrates

References: [1], [36], [37]

Next-generation displays will probably advance features of current display technology, which is e.g. already the case with 3D-displays. As far as substrates are concerned, they might have to be adapted to cope with this. In 3D-displays, the substrate is sometimes modified with lenticular lenses (used in so-called autostereoscopy), or multiple display planes are physically stacked (creating volumetric displays). Figure 1.28 shows a 3D display prototype as example. Other 3D-displays are based on projecting images on a rotating mirror, as illustrated in Figure 1.29.

Figure 1.28: A 3D display prototype (Philips)

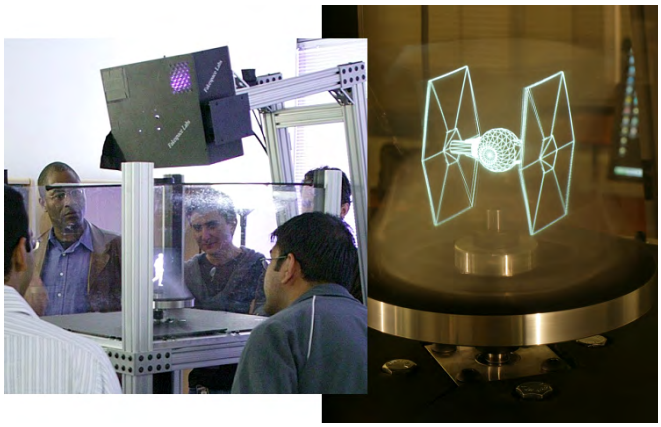

Figure 1.29: Displaying 3D-images through projection on a mirror

As for changing the substrate material itself, an interesting option would be to switch to stretchable substrates, where the space between the pixels, or the pixels themselves, might be stretched. Obviously, this would have quite some repercussions on the definition of the display specifications.

Another type of next-generation displays could be found in liquid displays, as compared to liquid *crystal* displays. If laser pulses are shot at water in a container, series of flashing dots could be generated. Figure 1.30 shows some tests illustrating the principle. The authors describe the display as having a spatial resolution and time resolution as high as respectively 10 pixels per mm and 500 frames per second.

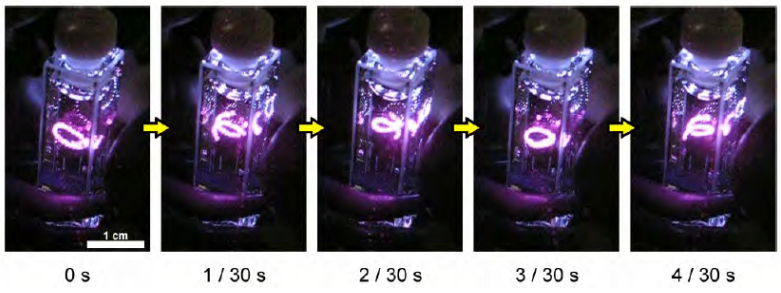

Figure 1.30: A display effect created by laser pulses shot at a water-filled container

1.4.4 Front Side Conduction

References: [1], [38], [39], [40], [41]

As the display effect requires electrical stimuli, electron conducting paths leading these signals to and from the pixels, have to be present. This is normally implemented by providing a patterned conductive layer at both sides of the display medium. This means there will always be a conductive interconnection layer in the line of sight of the viewer of the display, and care has to be taken that it does not affect the quality of the display too much. To cope with this, the conducting paths can either be made small as compared to the pixel size, or, and this is the more common solution, a transparent conductor is used. To be frank, this problem was encountered already some time ago, prior to the development of electronical displays, when, in wartime, a lot of effort was invested in research on transparent conductive coatings for de-icing the windshields of airplanes, as illustrated in Figure 1.31. In cars, up to now the first solution, whereby thin conductive lines are embedded in the (front and rear) windshields, is the more common option.

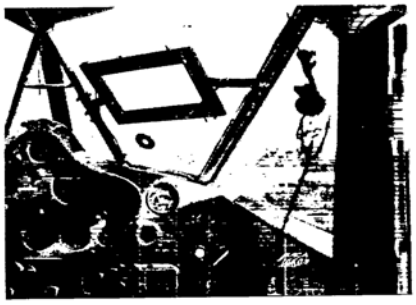

Figure 2.- Electrically heated windshield model mounted in an airplane windshield for flight tests. The main windshield is out out to permit the insertion of the heated panel.

Figure 1.31: Picture from a technical note of research on de-icing airplane windshields (1940)

In fact, any conductive layer will be transparent, when it is deposited sufficiently thin. However, this inversely affects the conductivity, so a compromise has to be made. Nowadays, by far the most widely used material for this is ITO, short for Indium Tin Oxide, and various formulations (mixtures) are used. Typical thicknesses for these layers lie in the range of 100 nm. Similar types are TiMo and several transparent conductive oxides (TCOs), e.g. Al-doped zinc oxide (AZO) and Zn-doped indium oxide (IZO).

Although the above mentioned materials show relatively high conductivities and high transparency in the visible region, alternatives are being researched and developed, due to high cost and limited supply of indium, the fragility and lack of flexibility of ITO layers, and the costly vacuum techniques used for layer deposition. Carbon nanotube conductive coatings are an interesting replacement to ITO, indicating more flexibility and robustness, lower cost and more environmentally

friendly processing, using wet-coating techniques. Conducting polymers such as PEDOT (Poly(3,4-ethylenedioxythiophene)) are also being used as alternative, but demonstrate less optical transmittance over the visible region. A comparison in optical performance of the discussed possibilities is shown in Figure 1.32.

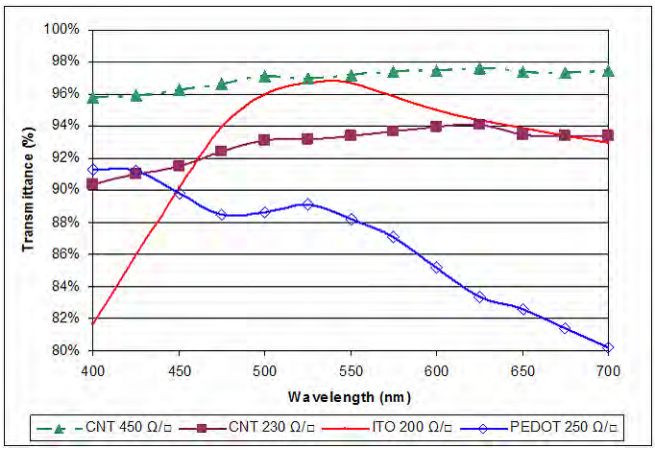

Figure 1.32: Optical performance: visible light transmittance of ITO, PEDOT and CNT films (EIKOS)

As this topic seems to be floating more and more into the general field of interconnection, the following chapter will provide some more background.

1.5 Advanced Display Research and Development

Several companies and research institutes are involved in advancing display research and development, many of which whose names have already popped up in the above explanations and examples. Of course a list can never be exhaustive here[11] but some of the better known are lined up in Table 1.2. The list is in alphabetical order to avoid speculations.

[11] a great many companies also have research areas very closely related to the display industry, although it is not their main focus

Barco NV	Bridgestone
Cambridge Display Technology	Center for Display Research (Hong Kong University of Science and Technology)
DuPont Displays E-Ink Corporation	Eastman Kodak eMagin Corporation
General Electric	Kent Displays
Lehrstuhl fur Bildschermtechnik (Stuttgart University)	Liquavista
Matsushita	Motorola
Philips	Pioneer
Plastic Logic	PolymerVision
Prime View International	Samsung
Seiko Epson	Sharp
SiPix Imaging Inc.	Sony
Thales Avionics LCD	Thomson
Toshiba	Universal Display Corporation

Table 1.2: Some companies in advanced display research

To deal with the specifics of each company would be leading us too far here, but a visit to their website should take you already a long way ...

1.6 Vision on Future Flexible Display Systems

References: [42]

The flexibility and the manufacturability of flexible displays themselves should evidently be considered an important issue, and, although this is not directly the main scope of this thesis, some introductory notes to these topics may be appropriate. First and foremost, it is clear, as with the comparison of display technologies in Section 1.2.10 and driving methods in Section 1.3.5, that the complexity and difficulties in the manufacturing process is highly dependent on several aspects: of course the display technology itself, but as well the used materials (substrates, conductive material for the row- and column-interconnection, display medium), the preferred driving method (matrix with or without TFTs), desired resolution (feature size) and optical behaviour of the resulting display (reflective, transmissive or emissive, color or monochrome, possible filters, refresh rate)...

On a slightly more general level, it might justifiably be advanced that the flexibility of a flat-panel display, apart from its driving electronics, is primarily dependent on 2 aspects: of each layer the material's elasticity, and this combined with its thickness. So this definitely means that also the total thickness is an important

factor. To give an example, in this way sometimes thin glass sheets are used as substrates for displays, which is a rather brittle material, but thanks to its thinness some flexibility is allowed.

Two examples to indicate the versatility of future flexible technologies: Shinoda Plasma and Samsung Electronics. Shinoda Plasma uses thin glass tubes and ITO conductive tracks for innovatively assembling flexible PDPs. The resulting display has total thickness of approximately 1 mm and has only horizontal flexibility. They expect to start commercial production by May 2009. Samsung Electronics has already fabricated color e-paper with CNT conductive tracks, using low-temperature processes on plastic substrates. The thickness of the result is a mere 0.3 mm.

Comparing different technologies' suitability for flexible display application, it seems that LCD technology has been studied more intensely, and therefore it can possibly be transferred more easily to flexible substrates, but it requires a backlight wherever it needs to compete with emissive technologies, e.g. plasma. Any backlight however will add significantly to the thickness: currently e.g. the thinnest backlights with lightpipe technology still have a thickness of around 1.5 mm. This might be reduced if backlights can be fabricated using large area LED technology on plastic. But in that case, it seems that the most promising technology for flexible displays would be OLED technology, as they can work with low voltages, are emissive themselves and can be produced compatible with low-temperature substrates. What should be taken into account here however, is that the used organic materials are still quite susceptible to moisture penetration and require sufficient barrier layers for protection against environmental conditions, and that they are current-driven, so that they require low-ohmic interconnection tracks. The drawback, as mentioned earlier already, is that thay are not bistable, so they need power constantly, but on the other hand they have a high refresh rate. For portable applications with low refresh rates, bistable e-paper technologies definitely have a high potential.

Concerning the interconnection tracks, rows and columns, on the display, flexibility is an additional requirement for the used conductors. As discussed in Section 1.4.4, ITO is the preferred choice for current glass displays, as it is highly transparent in the visible range and has a sufficiently low resistivity, although still many times higher than metals of comparable thickness. Unforunately, it is not considered suitable for displays that will be bent repeatedly, since it is rather brittle. Furthermore, for high-performance OLEDs several aspects of ITO are far from optimal: the migration and diffusion of indium and oxygen from ITO into organic semiconductors during OLED operation causes device degradation, the sheet resistance is still high, causing a significant voltage drop along the addressing line (and thus limiting the numbers of rows and columns), and the rising cost of indium. Alternatives are therefore being evaluated: e.g. carbon nanotubes (see a lit-

tle higher the example of Samsung Electronics), and polymers like PEDOT etc.[12], but also metals patterned with nano-imprint lithography (one of the "10 Emerging Technologies That Will Change the World", according to Technology Review), where thickness and width of the tracks in an array of tracks that constitutes a row or column track can be tuned to optimise transparency an conductivity, hopefully without severely compromising flexibility.

All of the above explanations indicate that a lot of possibilities are open for investigation and feasibility of quite a few technologies and combinations has already been proven and demonstrated. However, whether or not they can be scaled up for industrial production, and if so, in what timeframe this might be achieved, depends on a lot of things. For one thing, the current state of affairs, of LCD domination, will no doubt last some time, as there are still many low-end markets, e.g. in underdeveloped nations, where the high-volume capability of LCD can drive down the price of the display. Also, especially concerning new materials and technologies for high-end applications, this highly depends on how much the industry is willing and able to invest, the presence of suppliers to be found (and their eagerness to participate), and what the added value might be in the end application. All fancy words to say that I find it difficult to predict what will happen, and even more difficult where and when...[13]

1.7 Conclusion

In conclusion, it is apparent that a wide range of possibilities for displays exist through combining substrates with display effect technologies and driving methods, although not all combinations are viable, obviously. As there is no over-obvious winner in the ongoing display technology competition, it seems fair to state that the intended application is easily the most defining factor whenever a choice between display technologies has to be made.

As displays become more and more present in everyday life around the globe, display technologies are being heavily researched. This implicates that the display industry is a rapid-changing environment and it is difficult to give a comprehensive overview that will be valid for a long time. Therefore, the idea here was not to go too much in-depth, but rather illustrate the display industry and offer you a taste of some of its most famous flavours.

[12] also discussed in Section 1.4.4

[13] In my opninion, the prediction concerning flexible displays is comparable to e.g. the climate change debate: it is obvious for most people that it will happen (if it hasn't already), but what the implications will be and when they can be observed are not so clear, as it is more of a gradual process and not easily pinned down to just a few parameters in some simplified model

2
Introduction to Interconnection

"Time is the best teacher, but unfortunately, it kills all of its students."

— Robin Williams (1951 - ...)

This chapter ambitiously intends to give a technical overview of interconnection within the field of microelectronics. First some background as to "what, how and why?" is discussed, after which the topic of interconnection is broken down into several aspects. Starting from the carrying substrates, the subject is shifted to the fabrication of an actual interconnection layer on top of these substrates, and finally, assembly technologies are described for mounting components on top.

2.1 Electrical Interconnection of Components

References: [1]

Electrical interconnection means the physical linking of electrical devices so that transport of electrons between the devices is possible. This is necessary to supply the device with energy (electrical power supply) and/or a driving signal (communication with the device). To this end, it is preferable to have (electrically) conductive paths with as little electrical resistance as possible, so that the difference in electrical potential (voltage) is minimised, in value (heat losses) as well as in time (delay).

To compare different materials regarding resistance, Table 2.1 gives the resistivity values of some materials, some common in microelectronics, others rather

for reference.

Material	Resistivity @ 20°C [Ωm]
Silver (Ag)	0.0000000147
Copper (Cu)	0.0000000172
Gold (Au)	0.0000000244
Aluminum (Al)	0.0000000282
Iron (Fe)	0.0000001000
Lead (Pb)	0.0000002200
Indium Tin Oxide (ITO)	0.0000024500
Carbon (C)	0.0000350000
Polypyrrole (conductive polymer)	0.0100000000
Salt water	0.2000000000
Germanium (Ge), intrinsic	0.4600000000
Silicon (Si), intrinsic	3000.0000000000
Deionized (DI) water	181818.0000000000
Glass	10000000000.0000000000
PET	10000000000000000000.0000000000

Table 2.1: Resistivity of several materials

From Table 2.1, it is directly obvious that metals are by far the best option, at least where conductivity is concerned. In many applications, other properties are at least as important. For example in displays, the material for frontpanelinterconnection, is preferably optically transparent, directly eliminating all the electrically superior metals from Ag down to Pb. ITO is in this case the next best material and is therefore widely used in display manufacturing. Other applications require lower processing temperatures or low-cost deposition techniques, leading to conductive polymers as the preferable material. For reference, also the resistivity of two semiconductors, germanium and silicon, is included, as well as some better-known materials as glass and PET, often used (glass more than PET) for display substrates. Finally, the difference in conductivity between salt water and deionized water is illustrated.

Next to the conducting paths themselves, there has to be a carrier that supports these materials, as well as the devices. In its simplest form, this could be a cable or wire, but in the case of microelectronics, this usually does not offer sufficient support, implying an unreliable connection. Wirebonded chips e.g., in Section 2.4.2, have to be extensively protected by packaging or moulding technologies. Apart from these, the carriers are usually referred to as substrates[1].

Finally, interconnection in microelectronics is a complex subject and can be broken down into different categories: interconnection on a substrate, interconnection from a device to a substrate and interconnection from one substrate to

[1] except in the case of packaging where the carrier is the package itself

another. The first type of interconnection is achieved by depositing a conductive pattern on the substrate, here called routing technologies, the latter two types involve interconnecting the contacts of two independent pieces of, more or less advanced, electrical circuitry, and will be called assembly technologies.

As an example, the different aspects of electrical interconnection within microelectronics can be nicely illustrated by work that has been carried out within the frame of a thesis, the title of which can be translated as "Stretchable heater with built-in flexible display". On the one hand, a heating element was designed and simulated, and then fabricated on a stretchable substrate. The heating effect here is based on the heat losses generated when a current is driven through a non-ideal conductor with non-zero resistivity, as is the case for most electrical heating systems. On the other hand, circuitry had to be developed to drive and read out the temperature of this heater. Finally, everything had to be assembled together.

Figure 2.1 shows a picture of the first version of the heating element. It consists of a flexible, high-quality plastic (polyimide, PI) 25 μm thick, and a copper conductor layer. In the middle a temperature sensor is assembled so that the temperature (in the middle) can be measured. Contact pads on the heater are connected to the outer electronics by separate wires.

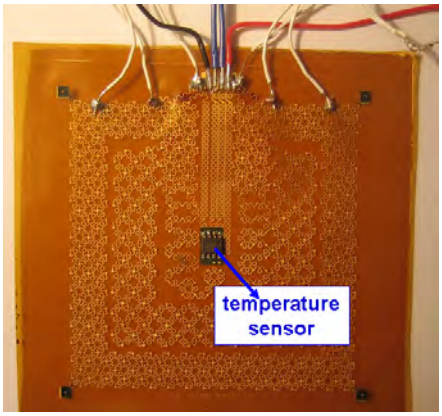

Figure 2.1: First version of the heating element: note the temperature sensor in the middle and the (rather primitive) wiring interconnection as interface

The final upgraded version is shown in Figure 2.2. The heater itself now consists of the same copper conductors, but they are embedded in a stretchable substrate. More accurately, they are sandwiched in between a thermally conductive silicone and an optically transparent, but not thermally conductive, silicone layer. Again, a temperature sensor is assembled, but this time nearer the contacts, and the heater is contacted by a flexible substrate, rerouting the contact pads to a connector.

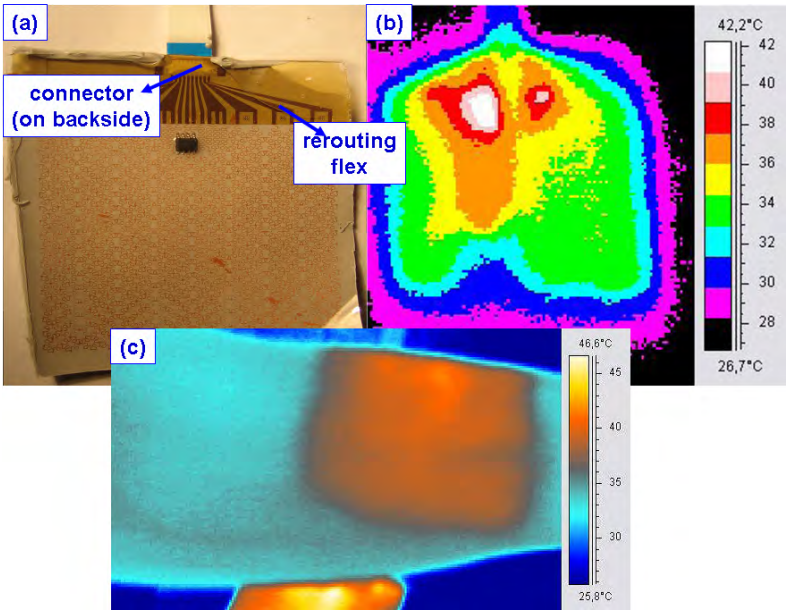

Figure 2.2: The upgraded version of the heating element: a picture of the fabricated result (a), as well as infrared images when operational, freestanding (b) and when placed on a volunteer's forearm (c)

Figure 2.3 illustrates the complete setup: the heater is connected with the drive and read-out electronics[2] through the cable connector, and 2 segmented LED-digits display the temperature. As shown, the display and electronics have also been upgraded to stretchable and flexible versions.

2.2 Substrates

References: [1], [35], [43], [44]

Substrates are, as mentioned already, the carrying structures of the interconnected circuitry, and so the choice of substrate is to be made very carefully beforehand. The mechanical properties of the complete system will be heavily determined by the substrate, so a sensible distinction in substrate types should be based on their mechanical properties.

Most substrates within the microelectronics manufacturing world, are currently of the rigid type. Examples are FR4 (FR stands for Flame Retardant)[3], well-known

[2] assembled on a rigid substrate

[3] FR4 commonly consists of a woven glass cloth construction laminated with an epoxy resin binder

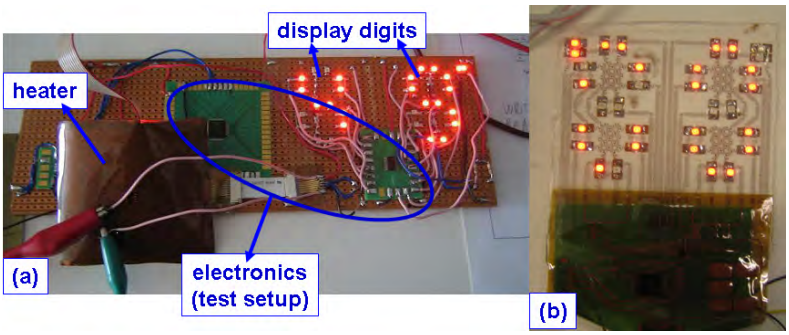

Figure 2.3: The complete setup: (a) the setup to test driving and reading out the heating element, and (b) the upgraded version of the setup, with stretchable display and flexible electronics

due to its widespread use for PCBs (Printed Circuit Boards), glass, used in almost all displays commercially available, and silicon, which, thanks to its semiconductor properties, can be at the same time used as substrate and as functional device, hence the name IC or Integrated Circuit. A typical PCB can be seen in Figure 2.4.

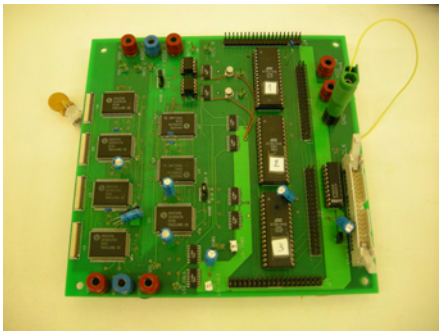

Figure 2.4: A PCB assembly for research on display driving schemes (TFCG Microsystems)

However, interest is growing for flexible substrates. These have the advantage of thinness, resulting in reduced weight and increased flexibility. Although the most obvious choices are all plastics, from the high-quality polyimides (PI) down to the low-temperature cheap polyethylene terephtalate (better known as PET), other interesting flexible materials include paper, (thin) stainless steel, thin glass and even thin silicon. It should be mentioned though, that the last two are considered too brittle at present to be used as stand-alone substrates. In Figure 2.5 a typical application for flexible circuitry is shown.

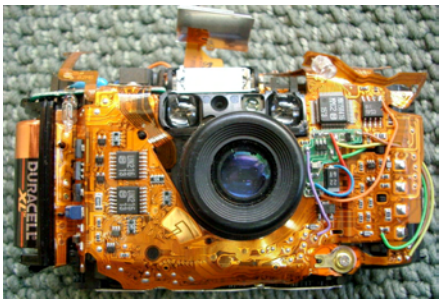

Figure 2.5: A camera without the case, revealing the flex circuit assembly (Olympus)

It is true that the introduction of flexible substrates into electronics has opened up a whole range of applications, and this can be mostly attributed to its mechanical properties of light-weight, bendability and conformability, especially interesting for portable applications. The next step down this road is probably introducing a certain degree of stretchability into the electronic substrates. This could lead to even more applications, and effectively and literally bring electronics closer to people, as obvious applications include intelligent textiles and implantable devices. Such devices could benefit greatly from the stretchability of the substrates as well as its breathability and biocompatibility. Most used materials here are silicones, such as polydimethylsiloxane[4], and polyurethanes.

Finally, intrest is also starting to grow for the use of recyclable substrates, e.g. through the use of mouldable thermoplastics, as well as biodegradable polymers. An evolution that can only be cheered, considering the current impact of electronics on the environment, which is increasing ever more with rising standards of living: both through the extensive usage of materials and energy throughout processing, and the resulting amount of generated waste after disposal of the electronic devices, the majority of which ends up in landfill sites around the world.

2.3 Routing Technologies

References: [1], [45], [46], [47], [48], [49], [50]

Interconnection on a substrate is achieved by routing technologies: in some way or other a pattern of conductive paths, able to route electrical signals, is deposited onto the substrate.

[4]PDMS, a polymer used in a wide range of applications, a.o. as food additive E900, in cosmetics and lubricants

2.3.1 Etching (Subtractive) Technologies

The standard way of getting a conductive pattern on a substrate in the microelectronics' industry, is by patterning a metal layer that has been deposited onto a substrate, as schematically explained in Figure 2.6.

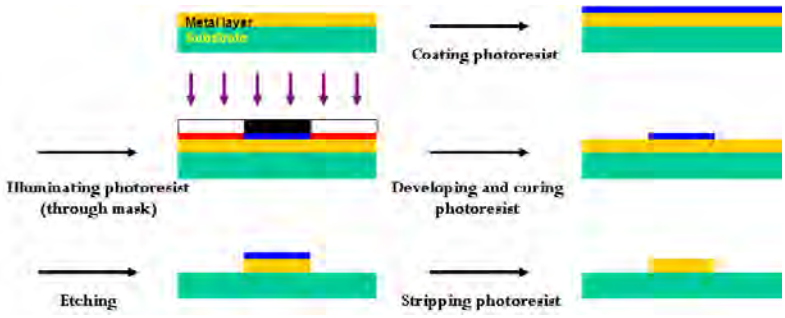

Figure 2.6: Schematical representation of typical lithographic patterning

In the case of Figure 2.6, the photoresist used is positive, meaning the illuminated parts are washed away during developing (so that the pattern in photoresist equals the pattern of the mask), but negative resists are used just as well. Etching technologies can be divided in two types: so-called wet and dry etching. Wet etching is a chemical process where the (unprotected part of the) metal is attacked and dissolved into the etching liquid. A phenomenon that has to be taken into account is called "underetching", because the etching liquid also etches material under the photoresist. Dry etching, also known as reactive ion etching (RIE) is the term usually reserved for plasma etching, where a plasma chemically and physically attacks the layer to be etched. This type of etching does not suffer from underetch and is therefore sometimes referred to as vertical etching. In few cases, etching is done by laser ablation, where laser bursts directly remove the metal from unwanted places. The advantage here is that (in some cases) no resist is necessary, but the drawback is that this is a serial process instead of a batch process (the laser has to "write" the pattern dot by dot), and therefore (again in most cases) not suitable for high volume production.

Deposition of a metal layer over the whole surface of the substrate in the above process can be done by different techniques. Lamination basically "glues" the substrate and a metal foil together, vacuum technologies as sputtering and evaporation physically deposit a thin film of metal onto the substrates, and plating techniques (electroless as much as electroplating) are used to either thicken an existing (thin film) metal layer or to deposit a new layer of metal. Plating is a (electro-)chemical process. Thin film processes typically deposit layers below 1 μm, whereas layers above this limit are commonly referred to as thick film. Nowadays, the difference is more fashionably called nano- versus micro-technologies.

2.3.2 Printing (Additive) Technologies

The printing process seems an interesting alternative to the subtractive technologies described above: vacuum deposition techniques are very time- and energy-consuming and, intuitively already, a lot of valuable metal is wasted by etching. Being fair and frank, however, it should be mentioned that lately, a lot of effort goes into recycling waste streams, both for cleaning/greening the process -less energy and (toxic) products wasted-, as required by current regulation, and for cost reduction purposes. In the sense of wasted effort, additive techniques would be less costly as well as more environment-friendly.

The material used for printing is referred to as conductive ink, and consists of small conductive metal particles[5] in a binder material. The metal content has to ensure the final conduction capabilities of the printed interconnections. The binder can be used to influence the viscosity and wetting properties of the ink and its adhesion to the substrate.

2.3.2.1 Stencilprinting

In stencilprinting and screenprinting, Figure 2.7, the ink, more accurately called a paste due to its high viscosity, is pushed through openings in a stencil or onto the substrate by the movement of a so-called squeegee blade. Stencilprinting is a quite commonly used technique in the electronics industry, especially for dispensing solder for assembly of components actually, so a lot of suppliers can be found for both adhesives and stencils.

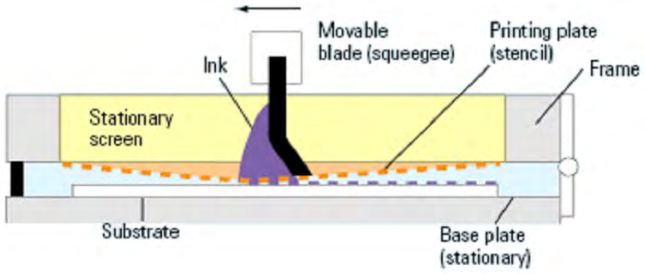

Figure 2.7: Stencilprinting principle

To illustrate, in the following is given a report of research on stencilprinting trials with conductive inks to look at the possibilities of printing very long and narrow lines. The idea behind it was to check if stencilprinting could be used in

[5] silver, carbon, copper,... , spheres as well as flakes

the fabrication of display backplanes, for patterning the conductor bus bars for the column and/or row tracks of active-matrix (flexible) displays.

From the stencil point-of-view, there is the difficulty of producing very narrow, but very long openings, causing stability problems. Concerning the ink, which consists of typically 50-80% metal particles (silver, copper, carbon) in a binder, the main difficulty lies in the current particle sizes: preferably the particles are 5 times smaller than the stencil openings, to ensure good printing results. 10 μm openings would therefore require particle sizes below 2 μm. No suppliers were found that could supply us with such materials. Future developments will undoubtedly resolve this problem, but for the moment inks with very small particles (below 1 μm) could be found only for inkjetprinting purposes, but these have a viscosity too low for stencilprinting. Suppliers contacted for inks are Cabot Corporation, Creative Materials Inc., Emerson & Cuming and Precisia LLC. For stencils MicroStencil Ltd, ScreenTec and Stork were considered.

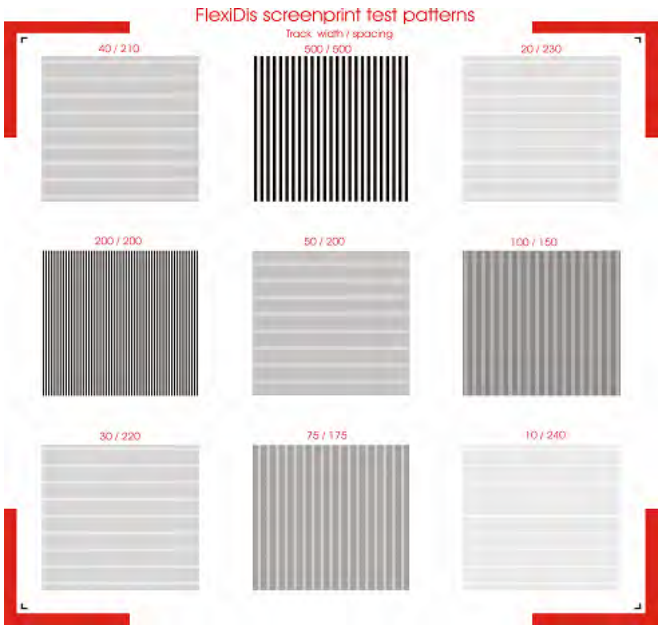

Figure 2.8: Test pattern design for fine line printing

With the first tests in mind, a design was made for a stencil for 100 mm by 100 mm substrates, incorporating nine similar patterns but with different dimensions. The layout is shown in Figure 2.8. The nine patterns are all approximately 25 mm by 25 mm and their track widths/spacings are designed to be (in μm) 500/500, 200/200, 100/150, 75/175, 50/200, 40/210, 30/220, 20/230 and 10/240. Adjacent patterns are rotated over 90 degrees, so as to distribute stresses on the stencil as

evenly as possible during framing and printing.

This design was discussed with MicroStencil Ltd (UK), and they agreed to make it. It is an electroformed stainless steel stencil, 7" diameter, 50 μm thick and mesh mounted on a 23" diameter aluminum frame.

MicroStencil had some difficulties to overcome in fabricating the stencil, due to the very long and narrow lines. One problem is the loss of adhesion of the photoresist during the development of the 10 and 20 μm lines. This is possibly caused by a high stress buildup in the exposed photoresist.

The coarser patterns however show some promising results in terms of sidewall quality, as can be seen in Figure 2.9. This indicates a potentially good release of the ink during printing.

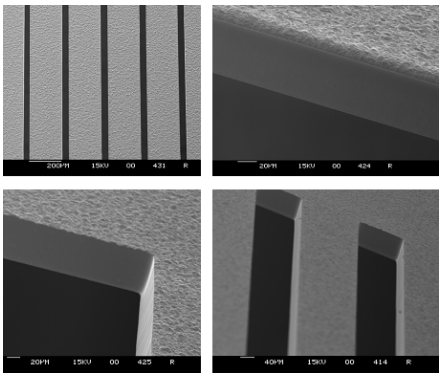

Figure 2.9: Result of stencil fabrication: illustrating an excellent sidewall quality

Another issue is the stability of the lines: the long lines easily move or damage after fabrication, Figure 2.10. This could lead to even more problems after framing (the X, Y, Z positions of the fabricated lines might shift or stretch) and during printing (the squeegee might damage the lines).

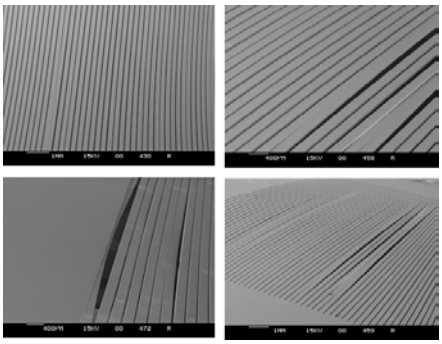

Figure 2.10: Result of stencil fabrication: the stability of the long narrow lines may lead to problems during framing and printing

To reduce the risks of this happening, it was decided to place stabilizer lines in all patterns. These are lines of 10 μm every 50 to 100 μm and have to provide more support for the long apertures. The consequence then is that either the ink has to spread enough so as to provide bridging, or it might be necessary to print twice, at a slightly moved (in the direction of the lines) position. In Figure 2.11 some pictures of the stencil are shown to illustrate the principle.

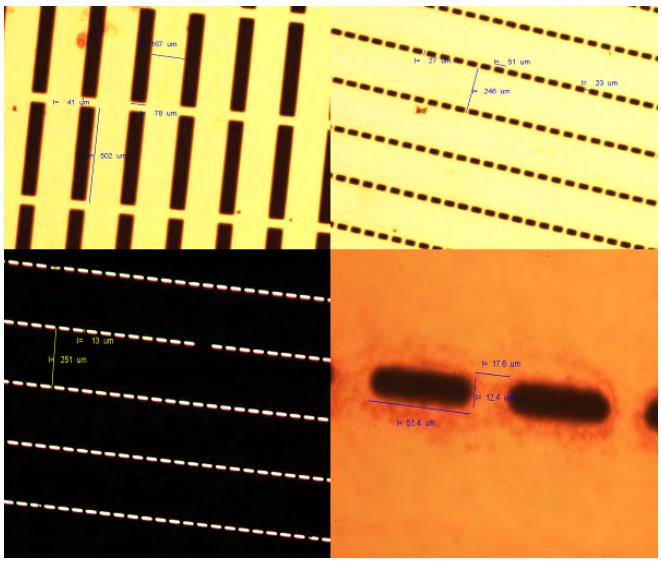

Figure 2.11: Result of stencil fabrication: clockwise from the upper left corner is shown the 75-μm pattern, the 30-μm pattern and two times the 10-μm pattern (the first one of these under a higher magnification)

For the inks, three samples were acquired for testing. These inks are XCE-80212-3iP from Emerson & Cuming (B, National Starch & Chemical), Electrodag PM-406 from Acheson Colloiden B.V. (NL) and CSS-010B from Precisia LLC (USA, Flint Ink Corporation), see the pictures in Figure 2.12.

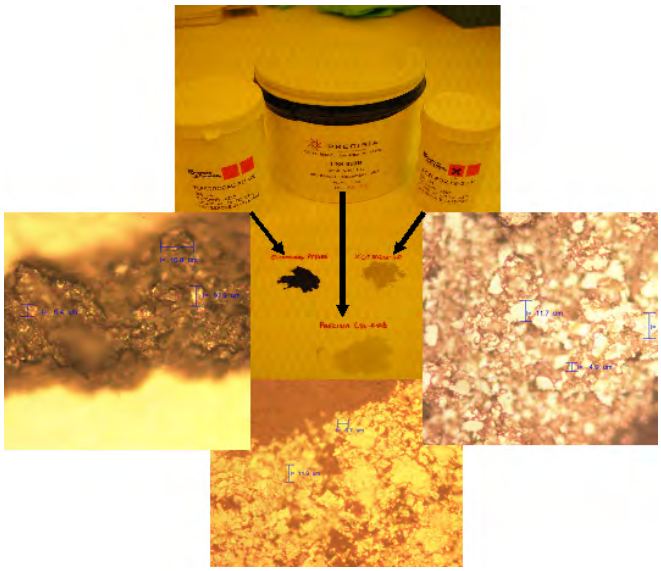

Figure 2.12: Acquired inks for stencilprinting trials: Electrodag PM-406 (left), CSS-010B (middle) and XCE-80212-3iP (right)

These inks all have comparable particle sizes (3-10 μm). XCE-80212-3iP showed the highest, and CSS-010B the lowest resistance. Also, XCE-80212-3iP showed the highest, and CSS-010B the lowest viscosity. Therefore the Precisia ink CSS-010B was used for the first tests, with the idea in mind that the lowest viscosity would have the highest chance on success in the smallest openings; that it should have the lowest resistance is also beneficial of course. Polyethersulfone (PES) substrates (transparents for an overhead projector) were mainly used, but polyimide (PI) was printed on as well. Figure 2.13 gives an impression.

Figure 2.13: Stencilprinting setup: from left to right the screenprinter, one of the test prints, and the used stencil

A few test prints were done, coarsely optimizing the printing speed for the smallest patterns from 80 mm/s to 50 mm/s. The print direction as well as the main printing parameters are shown in Figure 2.14. Results for the smallest features are given in Figure 2.15.

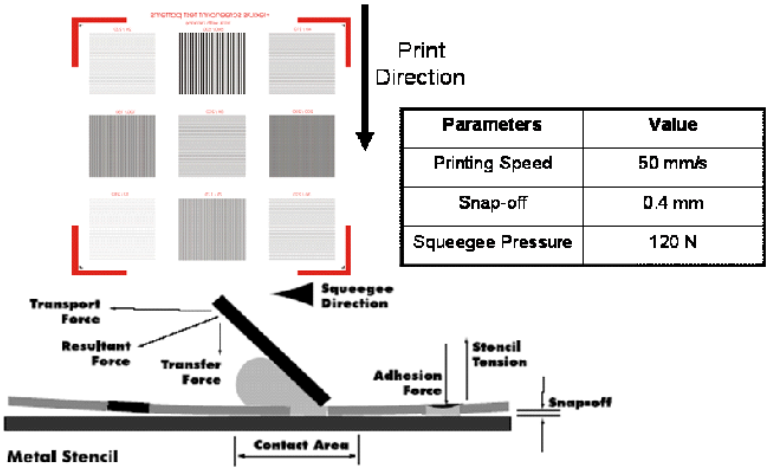

Figure 2.14: Stencilprinting setup: print direction and parameters

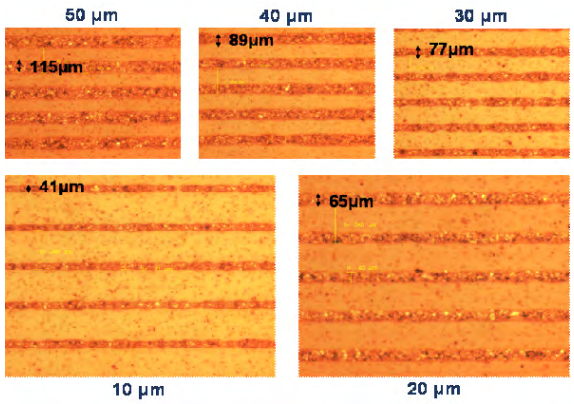

Figure 2.15: Stencilprinting results, clockwise from the top left corner: results from the 50, 40, 30, 20 and 10 micron stencil openings (all are 250 µm pitch)

The tracks shown have respective widths of approximately 115, 90, 75, 65 and 40 μm. The thickness of the deposited ink is 5 μm for the 50, 40 and 30 μm openings, while it is slightly lower for the 20 μm openings, 4 μm, and 2 μm for the 10 μm openings. A zoomed top view of the smallest lines and a few cross-sections are shown in Figures 2.16 and 2.17.

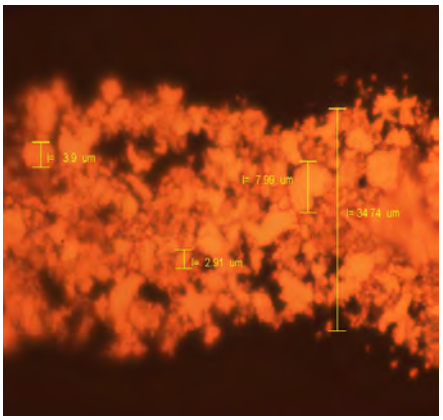

Figure 2.16: Stencilprinting results: zoomed top view of the smallest printed lines

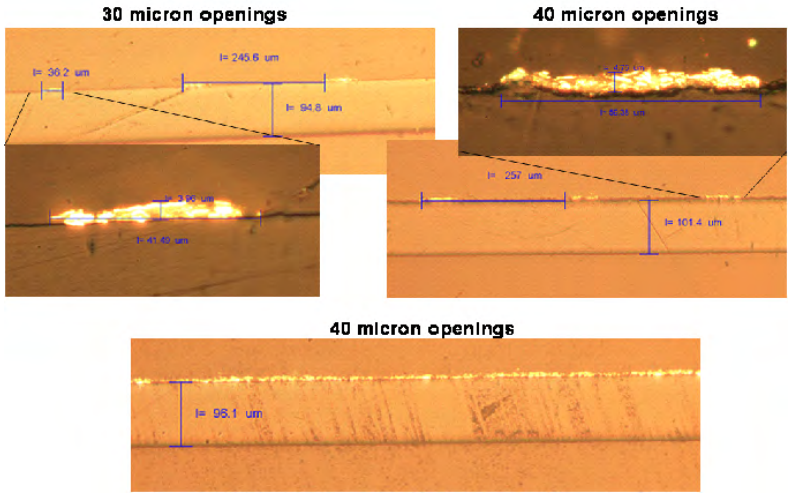

Figure 2.17: Stencilprinting results: cross-sections of the tracks corresponding with the 30 and 40 μm openings

The reason that the smaller openings resulted in thinner layers is probably due to the fact that it is harder to squeeze the ink through the smaller openings. This can also explain the drops at the extremities of the smaller printed lines, where there is not enough material pushed through the stencil to allow bridging between the adjacent openings, as shown in Figure 2.18.

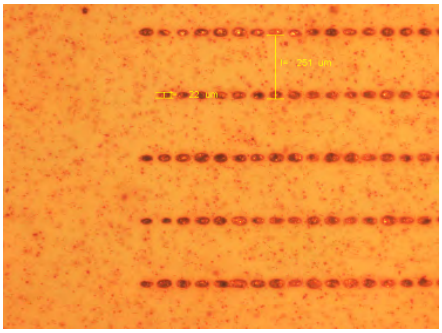

Figure 2.18: Stencilprinting results: drops at the extremities of the smaller printed lines

Resistivity values measured were all in the range of 0.1 - 0.3 Ω/□, Table 2.2, which can correspond to the Precisia datasheet reporting values lower than 0.015 Ω/□, for 25 μm layers.

Openings [μm]	Measured Resistance [Ω]	# Squares (approximately)	Sheet Resistance [$\Omega/\square$]	Thickness [μm]
50	2.15	20	0.11	5
	0.8	6	0.13	
	39.7	220	0.18	
40	1.24	6	0.21	5
	0.45	2.5	0.18	
30	0.65	4	0.16	5
20	0.5	2	0.25	4

Table 2.2: Stencilprinting results: electrical measurements

After some prints, the smallest stencil openings were clogged and could not be opened up again by cleaning. Some pictures of the clogged stencil, 30 μm openings, are given in Figure 2.19.

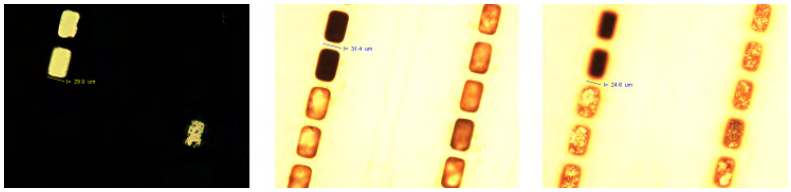

Figure 2.19: Stencilprinting results: clogged 30 μm openings, lighted from the backside (left), focused on the stencil surface (middle) and focused on the clogged silver (right)

The conclusion of this investigation was that, at this point, it seems that it will not be possible to efficiently stencilprint lines small enough so it can be used for depositing the conductor bars of a state-of-the art active-matrix display, where row and column tracks are typically 20 μm and lower (e.g. for a 100 dpi display). The limitations of stencilprinting lie in the combination of fine feature printing capabilities with cleaning possibilities. Intuitively, this can be explained as follows. The stainless steel stencil that is used in stencilprinting has to have a thickness of 50 or maybe 40 μm to guarantee sufficient mechanical strength during printing. This means that, to print features of 20 or 10 μm, the ink needs to be pushed through very narrow openings. Herein lies a drawback that is inherent to the stencilprinting technique: an ink with high viscosity is difficult to squeeze through the small openings and can easily clog those openings, while an ink with lower viscosity will flow more after printing, thus resulting in larger features than the intended 20 or 10 μm. A solution might be found in stencilprintable conductive inks that have smaller metal particles, down to nanoparticles as is the case for inkjetprinting inks. A uniform pretreatment might help to reduce flowing of the ink after printing.

2.3.2.2 Inkjetprinting

Inkjetprinting is a well-known technique from the graphical industry and is currently gaining in popularity in electronics manufacturing. The ink is shot at the substrate via nozzles, where the pressure is built up either thermally (bubble-jet) or piezoelectrically. The principle is shown in Figure 2.20.

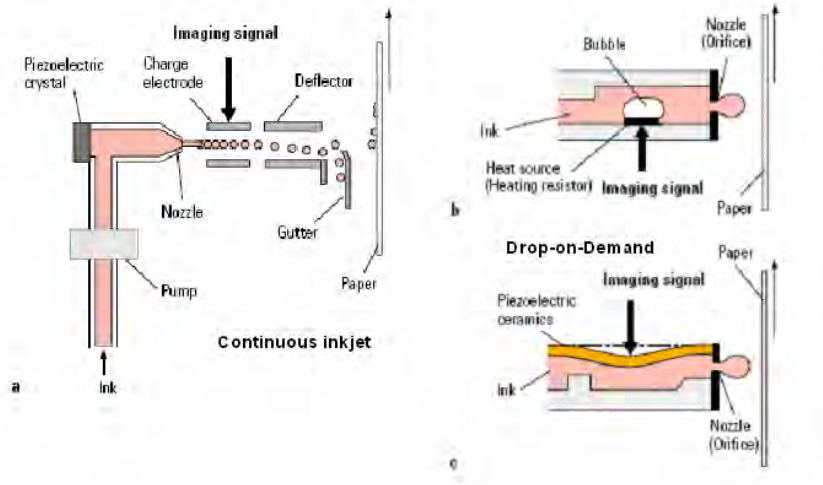

Figure 2.20: Inkjetprinting methods: continuous (a) and drop-on-demand thermal (b) and piezo (c) inkjet

Two interesting inkjet ink suppliers are Cabot-PEDs (Printable Electronics and Displays), and CimaNanoTech. The conductive inkjet inks typically consist of metal particles in a solvent, similar to other conductive inks, but with the main difference that the particles are much smaller (in the range of tens of nanometers), making the inks also much more expensive.

As an example, Figure 2.21 shows a labscale table-top Dimatix Materials Printer (DMP) together with some achieved results. The results shown were part of a master's thesis comparing screenprinting, inkjetprinting and lithographical patterning for wireless RFID tag applications using plastic substrates.

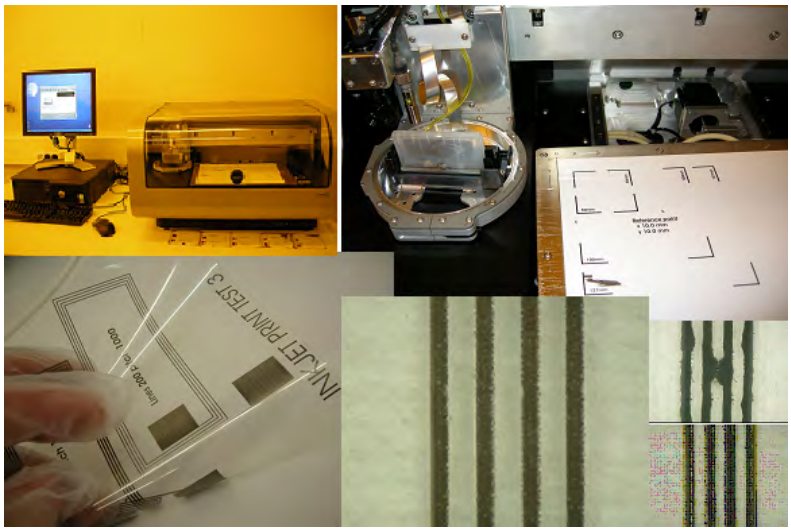

Figure 2.21: Inkjetprinting: the PC-controlled Dimatix Materials Printer (top left), the inside of the printer (top right) and some bad and good results on PET (below)

Figure 2.22: The Litrex M-series: large area electronics inkjet printers with performance proven up to Gen 8 substrates (up to 2400mm x 2400mm), a print speed of 1000 mm/s and a drop placement accuracy of 15 μm

The drawback of inkjet technology, is, similar to laser processing, that it is a serial process. Of course, if lots of nozzles are working in parallel (each completing a serial process), this drawback can be drastically reduced in importance. To illustrate the gaining popularity of inkjet printing, an inkjet printer for large area electronics is shown in Figure 2.22, developed for flat panel display (FPD)

manufacturing. Inkjets most important advantage, is the fact that it is a maskless process: subsequent substrates can easily be printed with slightly or completely different patterns through digital programming, without the necessity to physically alter anything in the production line.

2.3.2.3 High Speed Printing Technologies from the Graphical Industry

Other technologies for printing exist, and are, in principle, a lot older than stencilprinting and inkjetprinting, but have at the moment not yet been properly introduced in the electronics industry (although first steps are being made). The main technologies here are gravure, flexography and offsetprinting, where ink is transferred via a patterned cylinder to the substrate. They appear to have some major advantages over the mentioned technologies of stencil- and inkjetprinting.

- Since they are already being practiced for centuries, there is a lot of expertise available.
- These technologies are known throughout the world and equipment options are plentiful.
- They are all high to very high speed printing processes (e.g. for commercial web offsetprinting for newspapers and magazines, speeds of 15 m/s are common).
- Considering the widespread use, there is much pressure to constantly innovate and improve equipment and processes (especially for so-called security printing, printing bank notes,...).
- In newspaper printing, new printing plates are needed every day, so they must be made at quite short notice. This means plate manufacturing is rather quick as compared to stencil manufacturing.

A very good book describing and explaining seemingly all printing techniques used in the graphical printing industry is the "Handbook of Print Media" by Helmut Kipphan. An interesting company here is IGT Testing Systems NV (Amsterdam, NL), a company that makes proof printers, small printers that are used to test inks for gravure, flexography and offsetprinting. Currently, their main clients are businesses within the graphical printing industry, and therefore focused on colour proofing, but they are also interested in other applications, such as electronics printing. As for inks, e.g. Precisia has inks readily available for all three technologies. Figure 2.23 shows some of their (more commercial) achievements. For flexoplates, an important manufacturer of CtP-equipment (Computer-to-Plate) is EskoGraphics. They have in their product range an imager, the CDI SecuFlex, that can produce flexoplates with a resolution of 8000 ppi for security printing applications, which corresponds to a resolution of 3.175 μm. It is e.g. used in Japan

to negatively print characters of 1pt (approximately 350 μm). AGFA is a possible supplier for offset plates, and next to these, there is a company Triphol-NAKAN in Japan, which manufactures equipment for flexography and offsetprinting and is active in the display industry.

A good example of the possibilities of these high speed printing techniques, are of course bank notes. These have to be printed in large amounts with very fine print and often both sides are aligned. Furthermore, they have to be able to withstand a lot of rough handling. To illustrate, a 5 Euro bank note was examined in Figure 2.24.

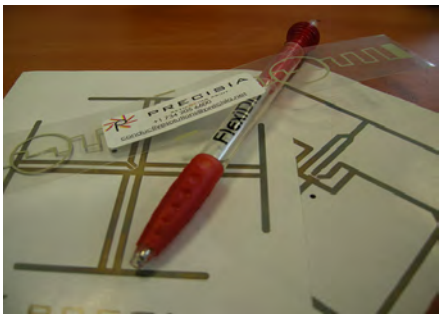

Figure 2.23: Achievements of Precisia with regards to printing Ag ink RFID patterns on flexible paper and PET substrates

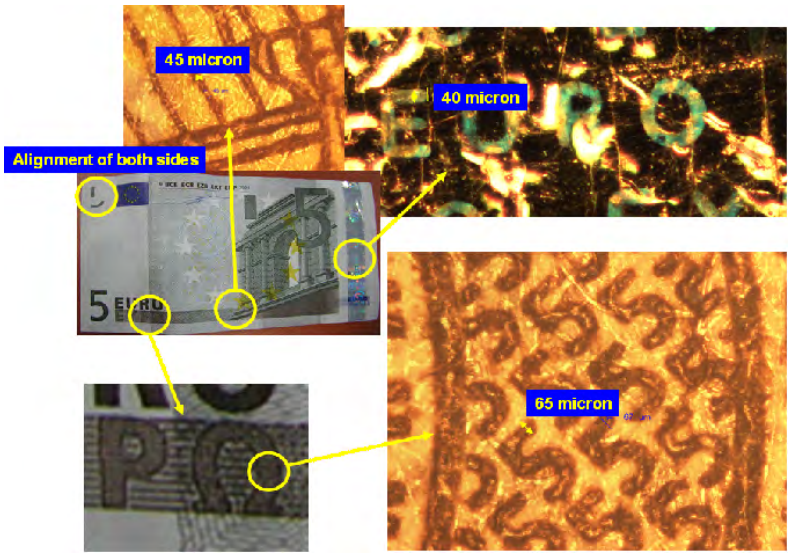

Figure 2.24: Banknotes are good examples of the possibilities of high speed printing technologies: high volume, small features and aligning both sides

The principle of gravure printing is given in Figure 2.25. A gravure cylinder contains the pattern to be printed, divided into discrete cells. These suck up the ink from the inking system and transfer it to the substrate, where it is sucked out again. Support is provided by the impression cylinder, countering the pressure from the gravure cylinder.

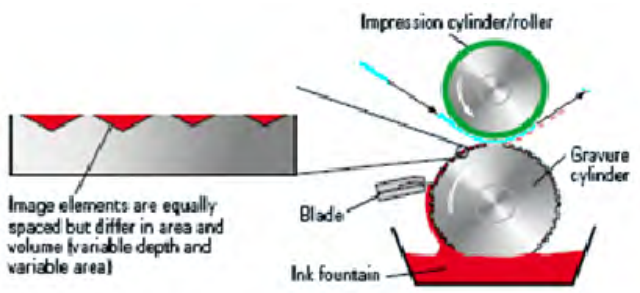

Figure 2.25: Principle of gravure printing

The principle of flexography is given in Figure 2.26. A soft, mostly photopolymer based, plate cylinder carries the elevated pattern. The ink is supplied by an anilox roller, whose discrete cells are filled up with ink. Then the ink, being on a raised platform, is transferred to the substrate, again supported by an impression cylinder.

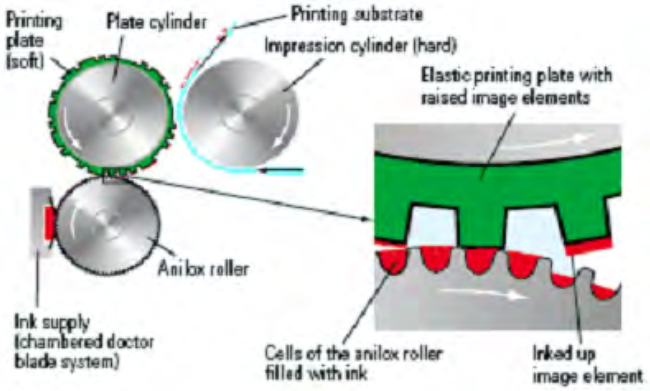

Figure 2.26: Principle of flexography

The principle of conventional offsetprinting is given in Figure 2.27. The major difference with this technique, as compared to the two previous ones, is that the printing and the non-printing parts (which form the pattern) on the plate cylinder

are practically on the same height level (around 1-2 μm difference), but for patterning, the printing parts are ink-accepting (oleophillic), whereas the non-printing parts are ink-repellent (hydrophillic). Two implementations are commonly used.

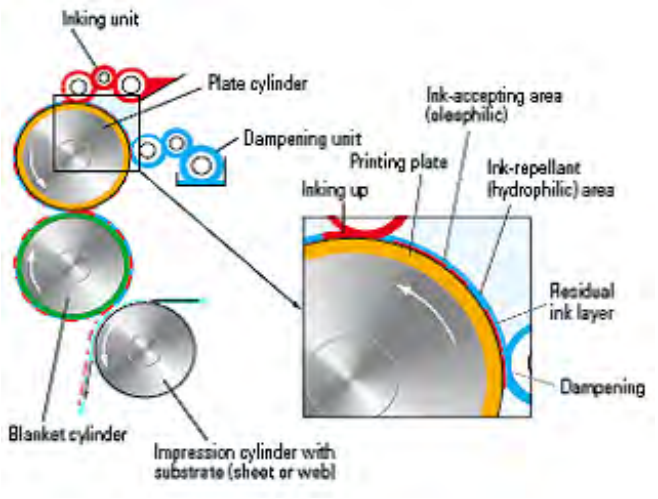

Figure 2.27: Principle of offsetprinting

In conventional offsetprinting, the non-printing parts are hydrophillic and accept water from the dampening unit. They are first wetted. The printing parts on the contrary are oleophillic and therefore almost totally unreceptive to the water. This means that the inking unit will only deliver ink to the printing parts, who are still open.

In waterless (dry) offsetprinting, the plate surface layer is ink-repellent, e.g. a silicone layer. Patterning is done by exposing the layer underneath, which is ink-receptive.

The main drawback of all these technologies is that they are not truly flexible in terms of switching print patterns: the master rolls have to be replaced, aligned and calibrated each switch. However, for high volume throughput, this is more than compensated by their sheer speed.

2.3.2.4 Comparison of Printing Technologies

To give an impression, microphotos of the plates needed for the technologies requiring a master plate are shown in Figure 2.28. A relative and a qualitative comparison between printing technologies is respectively given in Table 2.3 and Table 2.4.

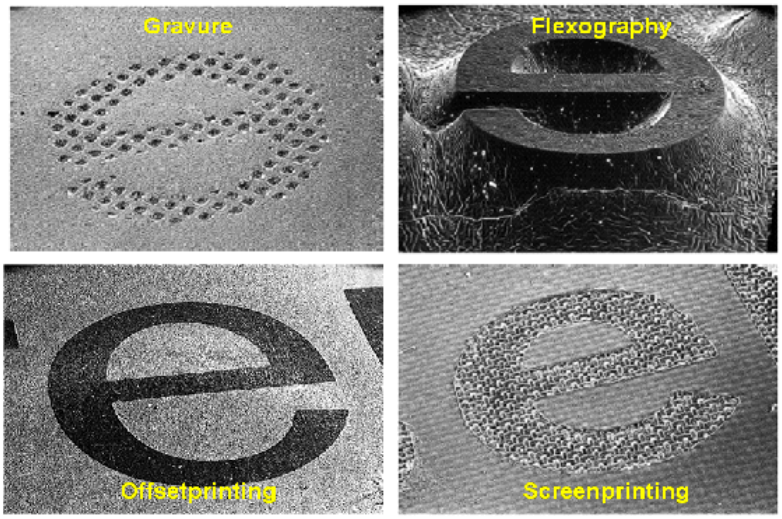

Figure 2.28: Masterplates for the various printing technologies (except for inkjet obviously): note that master plates for gravure and flexography require mirrored patterns

Table 2.3: Relative Printing Technology Comparison

Process	Resolution	Speed	Thickness	Particle Size	Ink Viscosity
Stencilprinting	0	0	+	–	+
Inkjetprinting	0	-	-	++	-
Gravure	?	+	0	?	-
Flexography	+?	+	0	0	-
Offsetprinting	+?	+	-	+	+

Table 2.4: Qualitative Printing Technology Comparison

Process	Advantages	Disadvantages
Stencilprinting	proven, thick possible	slow, discrete
Inkjetprinting	digital, proven	viscosity, very slow
Gravure	speed, resolution, solvents	viscosity, discrete, expensive
Flexography	speed, resolution, cheap, thick possible	viscosity
Offsetprinting	speed, resolution	limited thickness

Stencilprinting plates, or stencils in short, have sufficiently good resolutions: one was made at MicroStencil with 10 μm openings. Such high-resolution stencils

are costly and take typically times in the range of days to manufacture. Stabilizer lines are needed too, thus creating discrete cells, and reducing the potential resolution. However the stencilprinting inks have too large a particle size (a little below 10 μm) to achieve these high resolutions. Printing speed is adequate and thick layers up to several micron can be deposited. A wide variation of ink viscosities is printable and it is a proven technology in the electronics industry.

Inkjetprinting can supposedly realize 25 μm linewidths, it is a technology that has shown its applicability in electronics and can easily switch (digitally) between patterns. However it is rather slow, the deposited thicknesses are limited, as well as the viscosity range of the inks. Inkjet inks have the lowest particle sizes, in the range of 10-100 nm.

Gravure is said to be difficult to control due to the discrete engravings needed and the limitations this puts on the used inks (low viscosities). The engravings themselves are typically 4 μm by 4 μm. They are the cheapest for high volumes and can manage very high printing speeds. Since the plates need to be engraved, platemaking is rather expensive and time-consuming as compared to flexo plates.

Flexography can achieve potentially high resolutions[6], but is probably limited by the deformation of the soft printing patterns, since the printing and non-printing parts are not on the same height level. Its major advantage is its capability to print on a lot of different substrates, which is why it is widely used in the packaging industry (with non-absorbant and rough substrates). Plates are cheap and fast to make. Thickness can be high, but at the cost of resolution. Particle sizes lie in the range of microns. This could be a limitation to high resolution as well.

Offsetprinting has the highest potential for high resolutions, with Precisia claiming to have printed features of 15 μm, down to 10 μm. Printing speeds are high too, but achievable thicknesses are limited. The metal particles in the offset inks measure around 1 μm and are the smallest after inkjetted particles. Offset plates can quickly be made at resolutions above 4000 ppi, corresponding to 6.35 μm. Offsetprinting is also now the major printing technology in the graphical industry.

Cost was not looked into thoroughly, because this depends highly on the length and quality (yield, resolution,...) of the runs. An example of how the technologies can be compared is shown in Figure 2.29, from the "Handbook of Print Media".

[6] down to 50 μm fine lines are already printed industrially

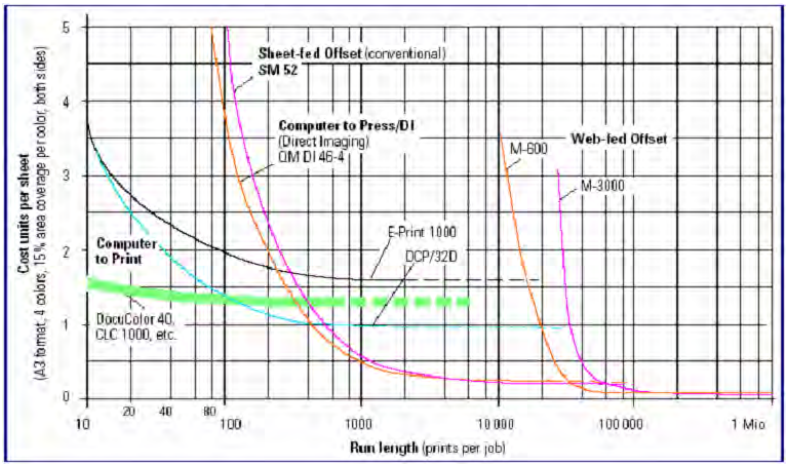

Figure 2.29: Examples of how to compare printing technologies: cost units per sheet in function of the run length

2.3.3 Hybrid Technologies

Again, as always, hybrid techniques are possible and quite often very interesting. As an illustration of a hybrid technique, a printing technology worth mentioning is electrophotography, more commonly called laserprinting. Here, the pattern to be printed onto the substrate is optically scribed in the patterning cylinder mere moments before it is printed, mostly with laser or LED arrays. This offers the advantage of high-speed reel-to-reel printing techniques combined with the pattern switching flexibility of digital (inkjet) printing, explaining why it is so widely used in office printers and photocopiers. The technology is illustrated in Figure 2.30.

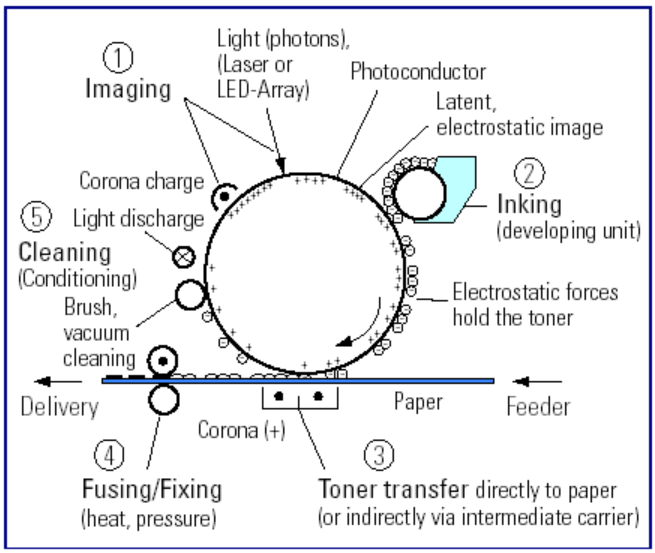

Figure 2.30: Laserprinting principle

Another interesting example of a hybrid technology, is when the etch mask is inkjetprinted, instead of a lithographically defined photoresist. This way quite a few steps in Figure 2.6 (soft-bake, illumination and developing) can be skipped in the process. The drawback here is that inkjetting can produce less fine patterns than lithography. A trial of inkjetprinting etch mask on glass is shown in Figure 2.31.

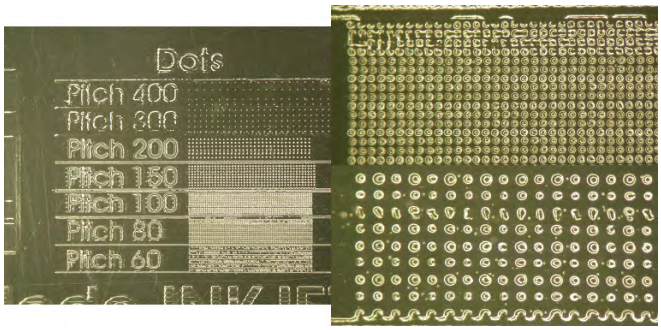

Figure 2.31: Inkjetprinting an etch mask: first trials on glass

One more technology under development consists of inkjetprinting the etchant onto the substrate. This is mainly interesting because it significantly reduces the amount of etchant needed, implicating a smaller cost and less waste.

2.4 Assembly Technologies

References: [1], [45], [51], [52], [53], [54], [55], [56], [57], [58], [59], [60], [61], [62], [63]

Assembly technologies are, as the name indicates, technologies for assembling devices and packages on top of a substrate, and by extension, also a substrate onto another substrate.

2.4.1 Soldering

Soldering, wave and reflow, is currently by far the most standard way of electrically assembling components onto substrates. Up until now, most component assembly was done by soldering with Pb-Sn-alloys. However, European regulation states that lead (Pb) must be banned from all processes, also in the electronics industry. Alternatives have been developed and are typically Sn-Ag-Cu-alloys (SAC). They have the (possibly temporary) disadvantage that they require higher reflow temperatures, over 250°C instead of approximately 180°C.

Contrary to manual soldering, with soldering irons and solder wire, industrial assembly plants use solder paste, a mixture of flux and the metal solder particles, for most soldering applications. As shown in Figure 2.32, the solder paste is dispensed on the contact pads on the substrate, then the components are aligned and placed, and finally the whole is cured in a reflow oven, where the particles melt together. The flux acts as a wetting agent and prevents oxidation of the metal surfaces involved. A microsopic view of the solder paste is shown in Figure 2.33.

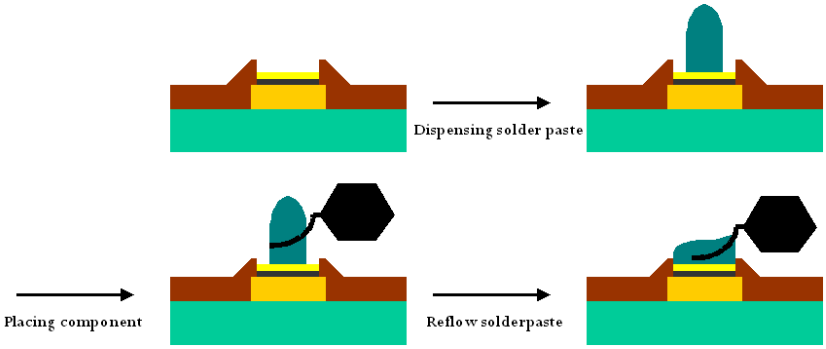

Figure 2.32: Bonding by Soldering

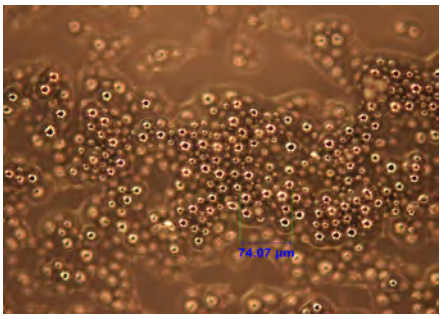

Figure 2.33: Solder paste as seen through a microscope: the SnAgCu solder particles in the flux material are approximately 20 µm in diameter

A common problem in soldering is tombstoning. The morbid term refers to surface mounted components, mostly small passives (resistors and capacitors), that rise up during reflow leaving one end soldered to the board and the other end free. It is caused by an unbalanced force due to non-uniform melting during reflow, mostly coming from different amounts of solder at opposite ends of the component.

A considerable advantage of soldering as compared to current adhesive assembly, is its self-alignment ability: during reflow, the solder makes sure the component's contacts (pins) are aligned optimally to the corresponding substrate pads. This is especially the case when a soldermask is applied next to the contact pads: the soldermask repels the solder, so that it is forced onto the pads. On the downside, soldering requires relatively high temperatures.

Solder can be dispensed, as above in Figure 2.32, but for finer features the solder is often applied beforehand on the package, or directly on the naked die, as bumps. An example of this are ball grid arrays (BGAs), a package where the contacts are arranged as an array of solder bumps. The use of solder bumps is illustrated in Figure 2.34.

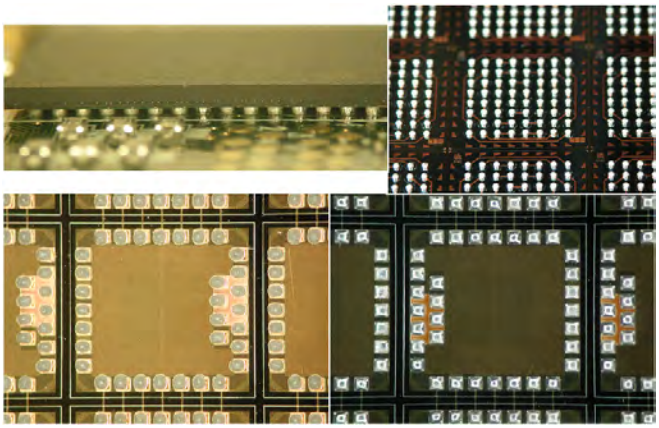

Figure 2.34: Illustrating the use of solder bumps: an assembled BGA package (top left), solder balls applied as bumps on naked dies (top right, 450 μm pitch), and the deposition of solder paste for wafer-level bumping before and after curing (bottom left and right, 300 μm pitch)

2.4.2 Wirebonding

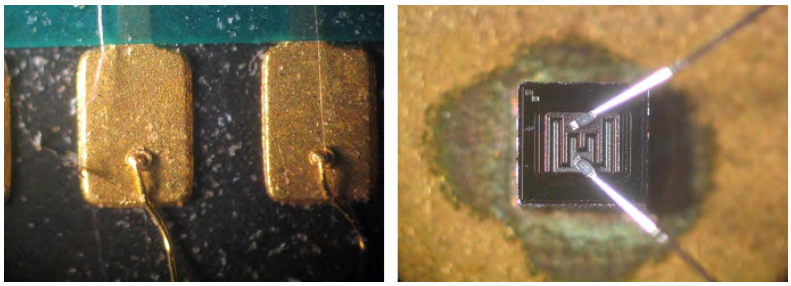

Figure 2.35: examples of wirebonding: gold wire ball-bonded to a gold contact pad (left) and aluminum wires wedge-bonded to a naked die (right)

Wirebonding is a technique, commonly used for interconnecting naked dies to a substrate and is the micro-equivalent of a simple cable connection. The wires used are generally gold, aluminum and copper with diameters from 15 μm up to several hundreds of μm. These wires are rather fragile and cannot be used for mechanical support. To this end, the naked chip is first glued face-up to the substrate, and afterwards the assembly is protected through packaging and/or moulding technologies. Two types of wirebonding are standardly used. Ball bonding is restricted to gold and copper wire and usually requires heat. Wedge bonding can use either gold or aluminum wire, with only the gold wire requiring heat. In either type of

wire bonding, the wire is attached at both ends using some combination of heat, pressure, and ultrasonic energy to make a weld. Figure 2.35 shows some examples.

Wirebonding is currently considered the most cost-effective and flexible interconnect technology for naked dies, and is used to assemble the vast majority of semiconductor packages. This is illustrated in Figure 2.36.

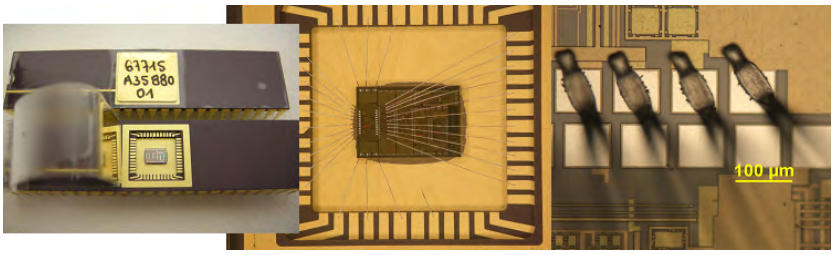

Figure 2.36: Illustration of wirebonding as a standard technique for assembling chips in semiconductor packages

Drawbacks of this technology are its fragility (the assembly has to be encapsulated), the parasitic effects associated with long interconnection lines (resulting in poorer high-frequency performance), the fact that the process is serial in nature (the bonds are formed one at a time) and the relatively large area on the substrate that is "lost" with this technique[7].

2.4.3 Adhesive Flip-Chip (FC) Technologies

An interesting alternative to soldering and wirebonding involves the use of conductive adhesives. Different approaches are possible using anisotropically, isotropically and non-conductive adhesives (ACA, ICA and NCA). They are mostly supplied as pastes, except for the anisotropical ones, that are more commonly used as film on a reel, somewhat similar to double-sided household tape.

Electrically conductive adhesives exist in various sizes and materials. They consist of conductive particles dispersed in a liquid polymer. Commonly, a distinction is made between hard particles and soft particles. Hard particles are then spheres of solid metal (Ni, Au, Ag, ...), while soft particles are plastic spheres coated with a metal.

Anisotropically and isotropically conductive adhesives are basically composed of the same materials, metal particles dispersed in a polymer, but the difference is that anisotropic ones have a much lower particle content (so-called solids content):

[7] as compared to flip-chip technology discussed in Section 2.4.3

the adhesive matrix contains a concentration of electrically-conductive metal particles that is below isotropicity. In other words, the concentration of conductive particles is limited to allow electricity to travel only in the Z-direction, and not on the XY-plane. Close-up pictures of the two types are shown in Figure 2.37.

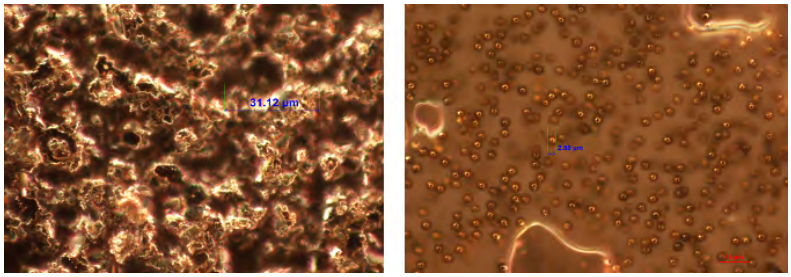

Figure 2.37: Isotropic and anisotropic conductive adhesive as seen through a microsope

2.4.3.1 Standard Isotropic Conductive Adhesive and Non-Conductive Adhesive (ICA/NCA) Assembly

Conventionally the isotropic conductive adhesive is applied on the contact pads, after which the chip is aligned and placed, and then the adhesive is cured. This is analogous to the soldering process, except for the fact that the temperature used for curing is much lower, namely around 120°C (and lower) instead of over 200°C. Next, a non-conductive adhesive, the so-called underfill material is brought in the remaining space between chip and substrate, typically a few tens of μm at the most, to increase the mechanical robustness of the assembly. This is done by applying the adhesive at one side of the chip, which subsequently flows under the chip, pulled by the capillary force of the empty space underneath the chip. The underfill time can be significant, easily 1 minute and more, depending on the size of the chip, the underfilling temperature, the underfill material (mainly its viscosity and wetting properties) and distance between chip and substrate (defined by the ICA bond and bump height), which is quite long as compared to most ICAs, snap curing in less than 10 seconds. The principle is shown schematically in Figure 2.38.

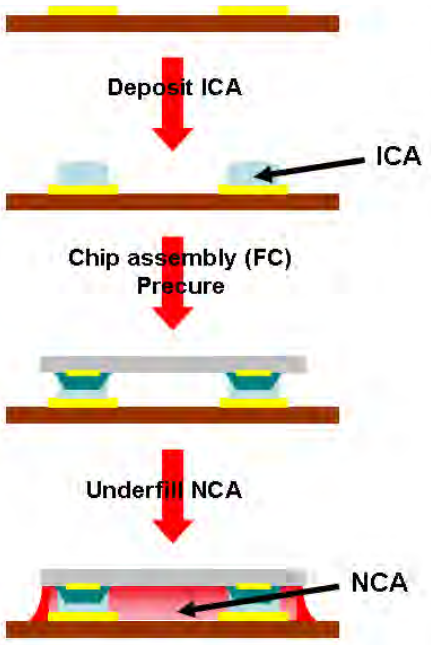

Figure 2.38: The principle of conventional adhesive assembly with isotropic conductive adhesives

This technology is used only rarely, mostly because the assembly is very fragile in the stage after curing the ICA, and before applying the underfill adhesive, often resulting in failed bonds at this point. On top of this, underfilling exerts a force laterally on the interconnection bonds and again risks damaging them.

2.4.3.2 Patented Isotropic Conductive Adhesive and Non-Conductive Adhesive (NICA) Assembly

A solution to the problems encountered by the standard ICA/NCA assembly sequence, as mentioned above in Section 2.4.3.1, is suggested by a similar technology, patented at the lab. The principle is shown schematically in Figure 2.39 and illustrated in Figure 2.40. The ICA is applied and pre-cured, and directly afterwards the NCA is deposited, before placing the chip. The NCA spreads out when the chip is being placed, and the whole is cured in a thermocompression step: a thermode head, heated to a certain temperature, presses on the assembly for a certain amount of time, similar to heat sealing.

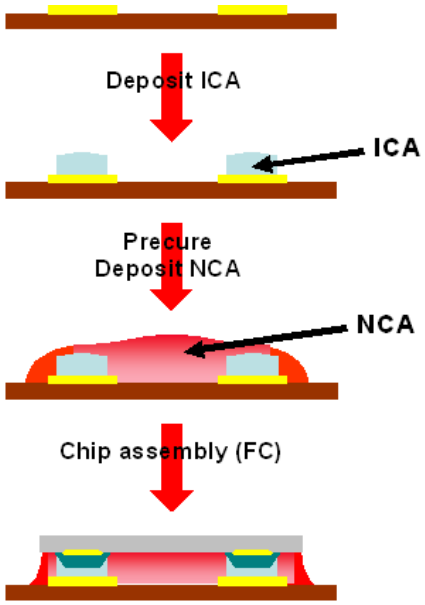

Figure 2.39: The principle of the lab's patented adhesive assembly with isotropic conductive adhesives

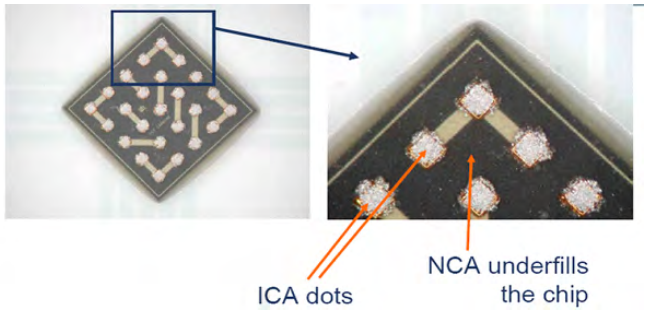

Figure 2.40: An example of adhesive assembly with isotropic conductive adhesives

This process is cheaper than the usage of anisotropic conductive adhesives as described below, and temperatures needed for curing are lower. It is faster than the conventional technology, since the slow underfill step can be left out, and is cheaper due to the lesser requirements for the NCA: the NCAs flowing properties are evidently much more important if it is to be used as underfill material. The main drawback as compared to anisotropic conductive adhesives is the significantly higher minimal interconnect pitch, because it is difficult to apply the ICA

dots on small pads, whereas with ACA, the adhesive can be applied uniformly over all the pads at the same time, so there is no need for fine-pitch dispensing.

2.4.3.3 Anisotropic Conductive Adhesive / Film (ACA / ACF) Assembly

Assembly with ACF is the technology mostly used for interconnecting drivers to a display and will therefore be returning several times throughout this thesis.

The principle of assembly technology using ACA/ACF is shown in Figure 2.41, and very straightforward: the ACA is uniformly[8] applied to the substrate, then the component is aligned and placed and finally the assembly is pressed and heated, in other words cured under thermocompression. In this thesis, as ACF, Hitachi AC-8408Y is always used, unless otherwise mentioned. The conductive particles are gold-coated plastic spheres, approximately 5 μm in diameter. These are coated with a very thin insulation layer, that has to be cracked during the thermocompression step. The purpose of this insulator is to prevent that the particles will conduct laterally when clustering occurs. The film thickness is 23 μm.

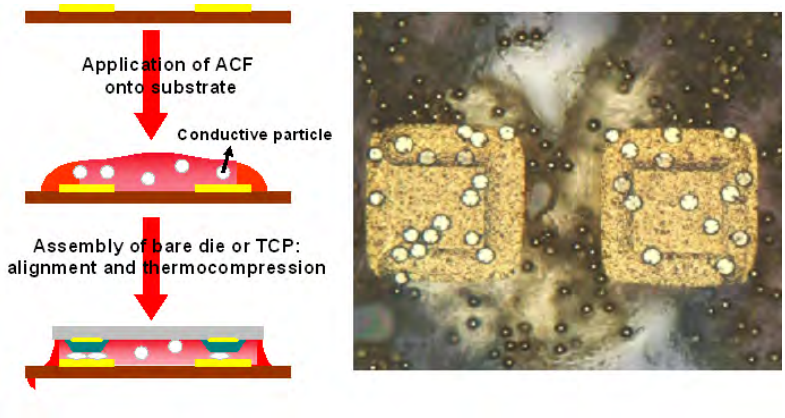

Figure 2.41: Principle of assembly technology using ACF

This technology can be used for very fine-pitch applications, 50 μm and even lower, but as there are currently only a limited number of suppliers, the adhesive is rather expensive. The main drawback of this technology is the slightly higher temperature needed for curing, approximately (minimally) 160°C as compared to 120°C and lower for ICAs and NCAs.

[8] in the case of ACF this is obviously fulfilled

2.4.3.4 Adhesive Bonding Equipment

This section provides a short overview of the equipment available at the lab (and needed) for adhesive bonding.

A stereomicroscope is indeed a convenient, if not essential, piece of equipment, when working with feature sizes down to 10 μm, the alignment accuracy needed when bonding at pitches down to 50 μm. It is used to apply the adhesive beforehand, and inspecting the bond afterwards. It is also useful for manual aligning, e.g. when the devices to be bonded are too large for the flip-chip aligner.

The working principle of the Karl Suss flip-chip aligner is shown in Figure 2.42. It basically involves getting overlapping images of substrate and chip in the microscope. The chip is picked up by a vacuum chuck, a beam splitter mirror is used so that the pattern on the chip and on the substrate can be viewed at the same time. The beam splitter effectively splits the incoming light, reflecting lower wavelengths (reddish), and allowing passage to higher wavelengths of the visible spectrum (bluish). Thus the chip can be aligned and placed. This is shown in Figure 2.42. It is clear that the calibration of the beam splitter mirror is crucial for the accuracy of the alignment.

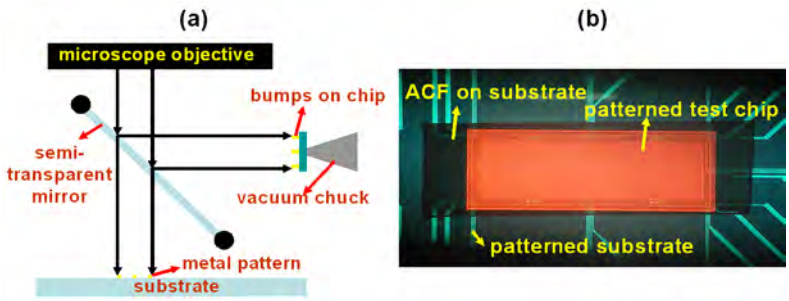

Figure 2.42: Aligning a chip to the substrate: (a) side view of principle, and (b) top view through microscope

After placement, the aligned assembly is transferred to the bonding equipment. For the actual bonding itself, two options are available. One is a very basic manual heat sealer[9], where the temperature of the thermode is set and controlled electrically, although with a rather large variation in time, oscillating nearly 10°C around the set temperature. Pressure is applied manually, and measured as applied kilograms. This is sufficient for more coarse work, with pitches over 500 μm, and up to bonding area dimensions of 5 mm by 125 mm. For finer assemblies, it is recommendable to switch to the semi-automatic (modified) Farco bonder. This is a

[9] a.k.a James (as in Bond 007)

machine that was originally intended for picking up, placing and bonding chips to substrates, but is in practice only used for bonding. The advantages here, as compared to the manual heat seal tool, are that the aligned assembly can be aligned to the thermode under a microscope, that a temperature profile can be configured for the thermode, and that the substrate table can be heated, which can be interesting for substrates that dissipate a lot of heat, e.g. stainless steel. Different sizes of thermode heads can be designed and manufactured, but the footprint area of the thermode is however limited by the (electrical) heating capacity of the drive electronics to approximately 150 mm^2. Both bonders are shown in Figure 2.43.

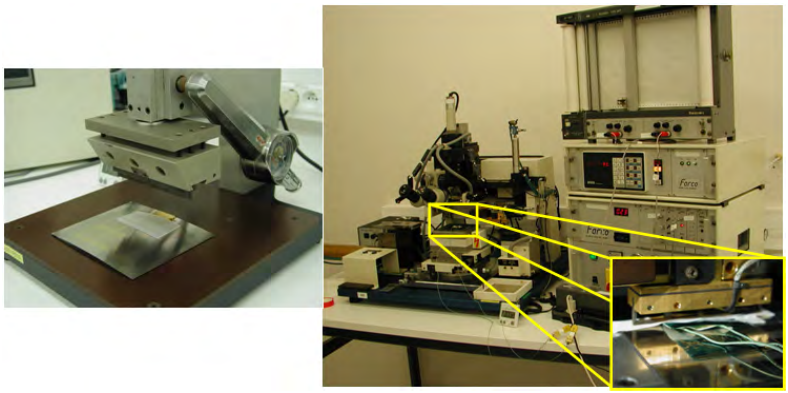

Figure 2.43: Bond equipment: the manual heat seal machine (left) and the semi-automatic bonder (right, setup with thermocouples for trials checking the temperature profile at the bond area

2.4.3.5 Adhesive Bonding Specifics

In this section, some topics are discussed that are important when bonding with adhesives, and therefore should be considered when the assembly is still in the design phase.

First and most important, there has to be an initial height difference between the conductive pads and the substrate of the devices to be bonded, in other words, the conductive pads to be interconnected of the devices should touch each other before their carrying substrates do. The reason for this depends on the type of bonding. In case of ICA/NCA assembly, the underfill should flow under the assembly, so a gap between the substrates is required. In case of NICA and ACA assembly, excess adhesive should be allowed to flow out from under the assembly during thermocompression; if not, the assembly will be actually floating on top of the adhesive and interconnection is not guaranteed. Also, alignment might well be lost after bonding.

To this end, pads to be interconnected are usually bumped. This means they

protrude more or less significantly out of the substrate. A distinction can be made based on the type of bumps. Hard bumps will crack when excessive pressure is applied, while soft bumps will rather deform plastically. Of course this also depends on the relative hardness of the substrate: sometimes the pads are simply pressed into the substrate. Hard bumps are typically solder, see Section 2.4.1, or NiAu, soft bumps include Sn and Au. Polymer bumps also exist, but are not common at all. Several technologies are available for deposition of bumps. One is chemical deposition by plating, both electroplating and electroless plating. Another important technique involves screenprinting of solderpaste. And studbumping, whereby basically a wirebond (ballbond) is torn off the pad, is also widely used. The former two are faster, as all pads are deposited at the same time, whereas studbumping is a sequential, one-at-a-time, process.

Stud bumps are generally more difficult to work with, at least as far as bonding is concerned: the tail of the studs varies in height (30 to 40 μm difference on an average height of 60 μm is common), is sharp and often not straight. Regarding flip-chip, this means that sufficiently high pressures are needed for establishing physical contact for all connections, and that the stud tips will concentrate stresses, exerted during first bonding contact, onto very small surface areas. Another possible problem that may occur is that the tail part of the Au stud can "fall down" instead of being pressed down when the tail angle[10] is too high. Figure 2.44 shows some typical Au studbumps.

Figure 2.44: Side view of Au studbumps on a Si chip, with top (left) and bottom illumination (right)

Another issue to bear in mind for adhesive bonding, but also in many other processing steps where structures are exposed to elevated temperatures, is thermal expansion. All materials expand (or contract) with temperature, and this is normally characterized for each solid material by the coefficient of linear thermal expansion (CTE). The CTE can thus be used to calculate (linearly) the expansion of a material, when it is heated up (or cooled down). During thermocompression bonding, the whole setup is heated up, and the substrates will expand according to their CTE. Usually, the two substrates will not expand equally, due to a CTE mismatch, and a difference in temperature felt by the substrates. The substrate closer to the thermode will probably absorb more heat than the one underneath. Also

[10]the angle formed between an imaginary vertical axis perpendicular to the silicon surface and the actual tail

it depends on the heat sinking capacity (heat conductivity) of the substrate, e.g. stainless steel diffuses heat much faster than glass. All this means that the pads on both substrates, while matching at room temperature, may not match anymore when curing sets in. The principle is illustrated in Figure 2.45. CTE values are usually expressed in ppm/K (parts per million per Kelvin), and are given for some typical substrates in Table 2.5.

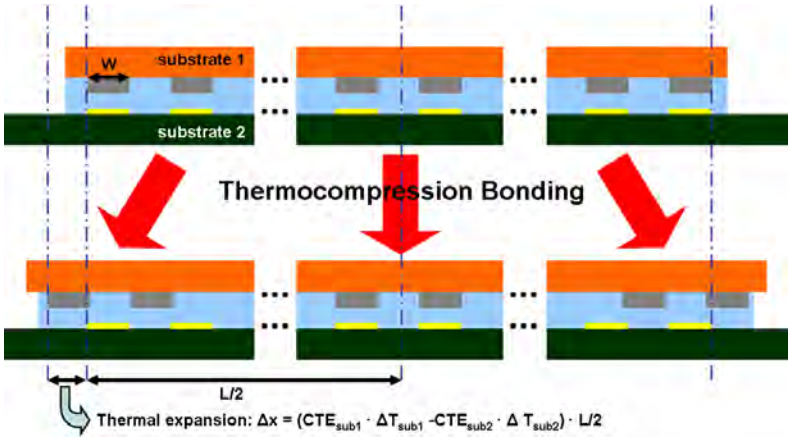

Figure 2.45: Principle of linear mismatch due to a difference in thermal expansion of the two substrates: L is the total bond length, W is the width of the bond pads, ΔT is the difference between thermocompression and room temperature

Substrate	Coefficient of linear Thermal Expansion [10^{-6}/K]
Glass	4.0-9.0
FR4	14 (in the plane of the woven glass cloth) 175 (perpendicular to the woven glass cloth)
PI	5-70
PET	20-25 (heat stabilised)
Ceramic	7
Silicon	3
Stainless Steel	15-20
Copper	16.5
Aluminum	22.2
Gold	14.2
Epoxy	18-20
Rubber	77

Table 2.5: Approximate CTE values for some common substrate types

Of course, thermal expansion is in most cases not critical. It depends on the

combination of total length of the bond area and the dimensions of the pads. More accurately, with the notations of Figure 2.45, there is no problem when $W \geq \Delta x$. Then, all the bonded pads will overlap at least half the bond pad area, if the middle area is accurately aligned, and although this results in a doubling of contact resistance at the sides as compared to the middle area, it usually does not pose a problem, as the contact resistance plays only a minor role in the total resistance. At least this is the case in display applications, where one of the metal layers usually has a relatively high resistivity.

Thermal expansion is usually precompensated in the design for the final assembly, based on either theoretically calculated expansion models, or practical bonding trials. Actual trials are generally recommendable, as a lot of factors in the complete setup influence the thermal behaviour during bonding: not only the substrates, but also the conductive patterns, the surrounding setup (such as carrier substrates) and the used substrates can play a significant role.

During bonding, parallellism is extremely important: the bumps of the bondpads should be pressed evenly to ensure contact over the total length. For instance, if the bumps are 10 μm, and the bond length is 50 mm, not uncommon for driver TCPs, a flatness is required equivalent to a maximal variation of 20 mm on a 100-metre-long stretch of road. Therefore, the thermode has to be accordingly flat, and it must be accurately calibrated before bonding. The calibration is usually carried out with pressure-sensitive tape. In that case, the tape is placed on the bond table and the thermode tapped down once. The table is then adjusted accordingly. Another possibility involves a full bond cycle, including thermocompression, that is forced on a burnable substrate, e.g. filter paper. After completion, the homogeneity of the scorched area then gives an indication of the uniformity of the bond. These techniques are illustrated in Figure 2.46.

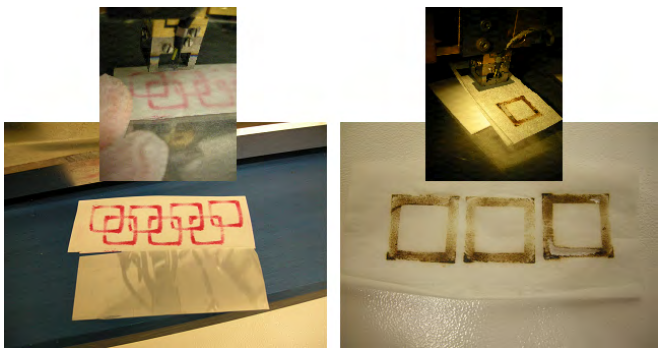

Figure 2.46: Two methods for calibrating the bonding thermode: using pressure-sensitive tape (left), and with filter paper (right)

To further enhance the homogeneity of the pressure felt by the assembly, a layer of thermally conductive silicone is normally laid in between the thermode

and the assembly. This somewhat redistributes any remaining pressure concentrations connected with the roughness of the thermode and of the pressed device itself.

One last practical note involves the storage of adhesives. In an industrial environment, this may not be a very important concern, but in a lab, where it is used only occasionally with intermittent periods, it is practical not to have to order new sample material every so often. In thermal curing adhesives, it is advisable to store the adhesive at the recommended temperatures, usually in a fridge around -20°C. Furthermore, it was found that for ACF, the lifetime, in our case a few months as stated by the manufacturer, could be extended by a few years, by keeping it stored in vacuum-sealed bags, as commonly used in food packaging.

Finally, a more general, and probably obvious, remark concerns the aspects to keep in mind when developing assembly technologies: optical, mechanical and electrical measurements should be carried out afterwards to verify the quality of the technology. Optical ones involve alignment accuracies and optical bond inspection, mechanical ones mean adhesion tests, namely peel strength and shear tests, and electrical ones range from daisy chains and 4-point contact resistance to capacitance and shorts testing.

2.5 Conclusion

References: [64]

Again a wide topic has been introduced in this chapter. Electrical interconnection has been split up into its different aspects of patterning or routing technologies, for on-substrate interconnection, and assembly technologies, for to-and-from-substrate interconnection. Increasingly, these technologies are being combined and integrated into complete systems, resulting in all kinds of advanced names varying from SiP (System-in-Package) and CoC (Chip-on-Chip) up to PoP (Package-on-Package) and RCP (Redistributed Chip Package).

For interconnecting drivers to displays[11], the technologies most common are adhesive bonding technologies, although wirebonding is also used for microdisplays, and zebra stripes interconnection, which will be explained further on in Section 3.1.2. For interconnection in the display itself, addressing the display pixels, all discussed patterning technologies, lithography and printing alike, are used for various processing steps in display manufacturing.

[11] as is the title of this thesis, if you remember

3
Rigid Displays

"Wonder is the beginning of wisdom."

— Greek Proverb

This chapter gives some practical examples of display assembly and physical integration with the driving electronics. All displays here are rigid displays, and more specific, they are glass displays.

The reason glass is usually the preferred choice as display substrate is threefold. First of all, it is transparent, required for at least one substrate of the display (as obviously you have to be able to see the display effect). Secondly, it is a very inert material, capable of withstanding high temperatures and most common chemicals and solvents. This means it is a very interesting substrate from a processing point-of-view. Finally, glass acts as a very efficient barrier layer against environmental conditions. It prevents heat and moisture from penetrating and thus effectively isolates the active display material from the most important detrimental outside influences.

3.1 Cell Phone Display

Cell phone displays are currently among the most widely used active- and passive-matrix displays around the world. Up to now, they are commonly built with glass substrates using LCD technologies. As there are so many around, there are also

some different methods in use for integrating the displays within the cellphone system. In this section, two actual methods are given and illustrated.

3.1.1 Flex Interposer Interconnection

A straightforward method of connecting a display to its driving electronics consists of using a flexible substrate, with a metal layer, patterned so that it matches the display's contacts on the one side and the electronic circuit's connector(s) on the other. This so-called flex interposer, is then bonded to the display substrate using ACF. An example is shown in Figure 3.1. In this example, the (dual) interposer flex consists of 25-μm-thick PI substrate with a 9-μm-thick Cu/Ni/Au routing layer.

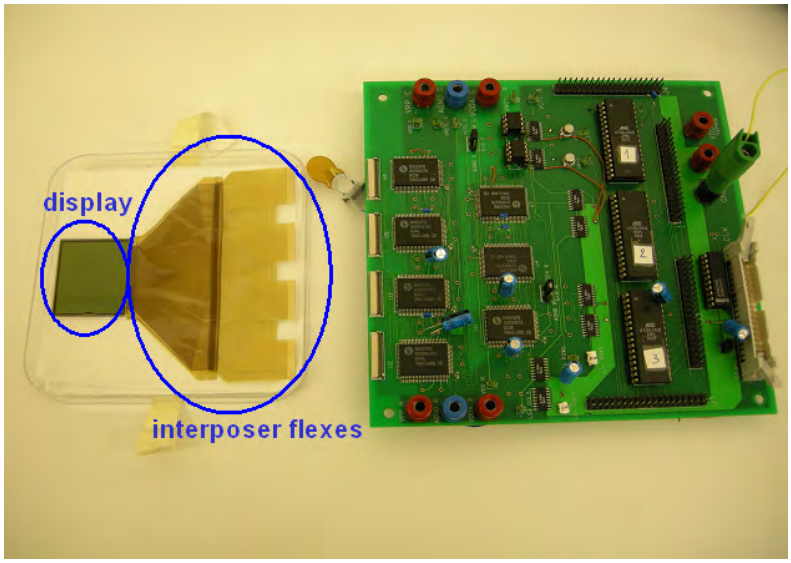

Figure 3.1: Interconnecting a display using an interposer flex: the display is intended for a cellphone, the PCB (on the right) is used for testing drive schemes (obviously far too big for an actual cellphone, see also Figure 2.4)

As the number of contacts equals the sum of rows and columns, a lot of interconnections have to be established for current cellphone matrix-displays. As discussed in Section 2.4.3.5, the finer the pitch and the larger the number of contacts, the more thermal expansion should be taken into account. An obvious solution to this is to compensate it beforehand in the design phase by shrinking the pattern on the flex interposer, as discussed earlier in Section 2.4.3.5. Another common solution, however, is to (gradually or suddenly) enlarge the features from the middle of the bond area towards the sides. This means the finer contacts are in the middle

area, the coarser at the edges, and thermal expansion is compensated for by the larger pitch of the outer contacts. This can be seen in Figure 3.2.

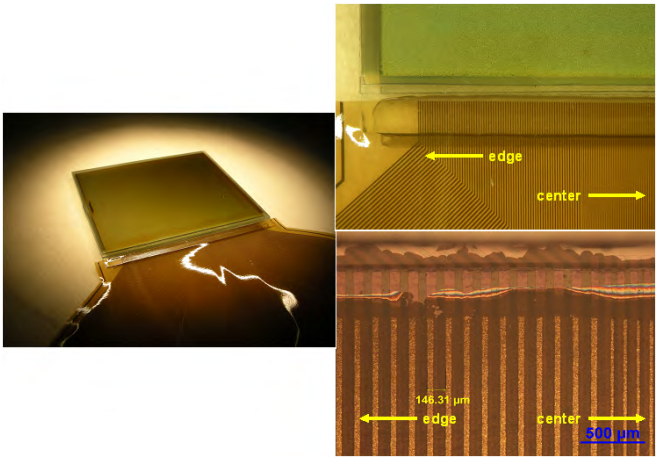

Figure 3.2: A display contacted by an interposer tape: the contacts are significantly denser towards the middle of the bond area (right)

3.1.2 Zebra Stripes Interconnection

Another very common method for electrically interconnecting a (cellphone) display to its driving electronic backplane is through zebra interconnection stripes. To illustrate, a cellphone was disassembled in Figure 3.3.[1] By mounting the driver chip directly to the front display substrate, the number of contacts to be connected to the driving electronics on the cellphone backplane is drastically lowered. The resulting coarser interconnect pitch allows for a zebra stripes interconnection.

Zebra stripes are a very basic form of (temporary) interconnection. The structure is fabricated so that it is electrically conductive in one direction only: it consists of layers of conductive material and non-conductive elastomeric material alternating at a pitch of, in this case 100 μm. The whole is sandwiched in between the substrates to be connected, in this case the front display substrate (glass) and the cellphone backplane (PCB). The principle is shown in Figure 3.4. Some pictures to illustrate are shown in Figure 3.5.

[1] Reverse engineering is a very instructive activity, especially for getting a good first impression of state-of-the-art technologies

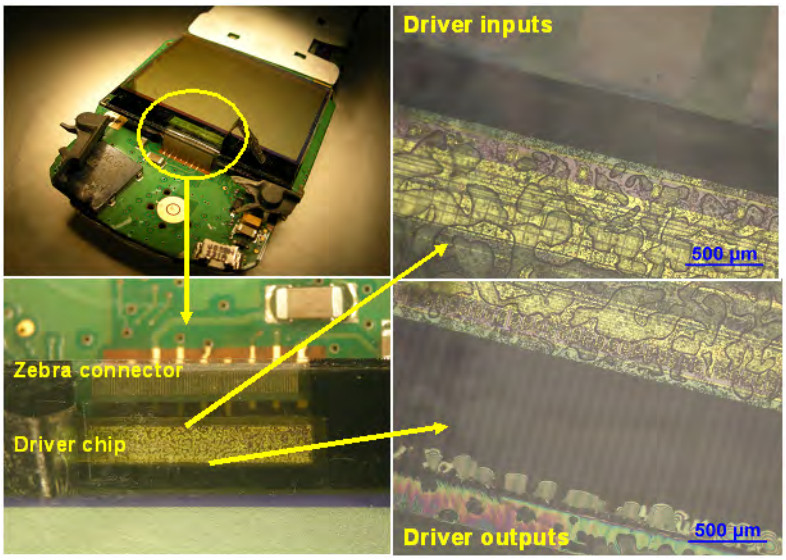

Figure 3.3: Disassembly of a cellphone: the driver chip is directly mounted on the glass of the LCD, and the (fewer) inputs are connected to the electronic circuitry by zebra stripes

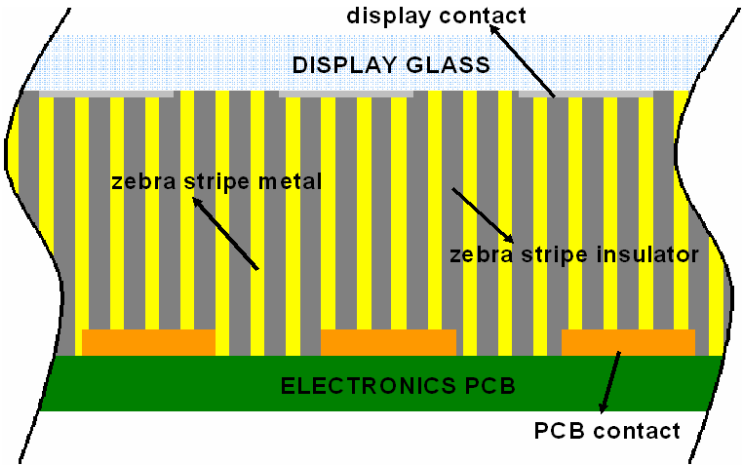

Figure 3.4: The principle of a zebra stripes interconnection

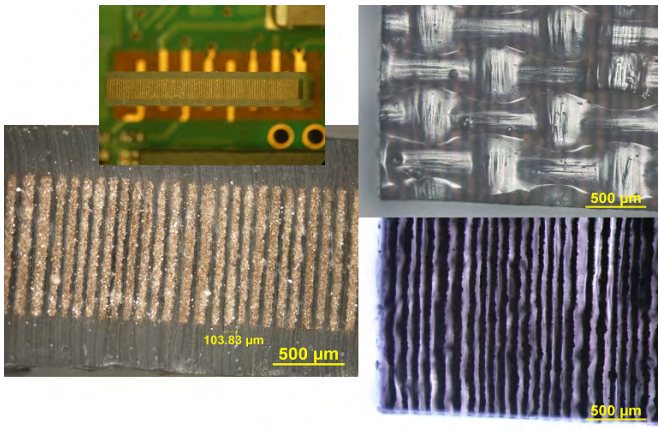

Figure 3.5: Zebra stripes: two top views (left), a side view showing the outer elastomeric material (top right), and a view explaining where the name "zebra stripes" originates from (bottom right, side view illuminated from the back)

3.1.3 Hybrid Interconnection

Although not actually a cellphone display, but a somewhat larger display to be used for agricultural machinery, is a nice example of the hybrid use of the above technologies. It involves long zebra stripes for the columns, and a flex interposer for the rows. The assembly is illustrated in Figure 3.6. The flex interposer is somewhat different from what's been described in Section 3.1.1. Instead of a polyimide foil with a Cu routing layer, a 23 μm PET foil, with a graphite routing layer is used. Additionally, the ACF is pre-applied[2] over the whole surface of the interposer, reducing the number of process steps for bonding, as the ACF no longer needs to be applied separately. On the other hand, more ACF is required and therefore wasted, which increases cost, but this might be compensated by the use of low-cost PET/graphite interposers.

[2] this is also called hot-melt

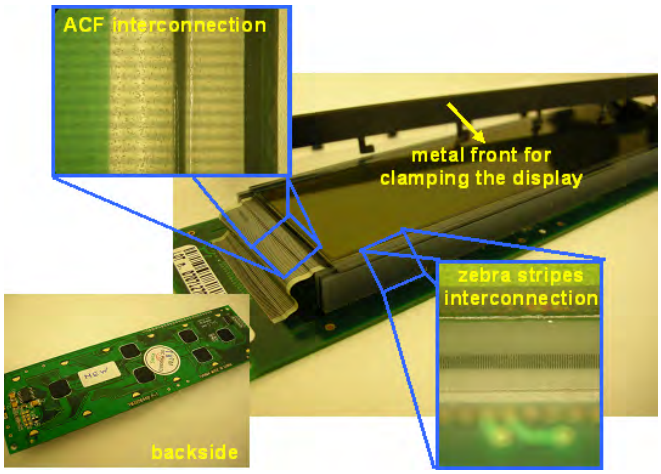

Figure 3.6: A display with ACF interconnection for the rows and zebra stripes for the columns: the electronic circuitry is assembled on the backside of the PCB, and the zebra stripes are clamped between display glass and PCB by a metal front

3.2 Watch Display

Within the frame of a master thesis, "Realisation of a flexible and stretchable wrist-worn display", a standard rigid glass LCD display, 4 digits and 7 segments, was to be driven and interconnected to make a wristwatch. In this thesis several technologies under development at TFCG Microsystems have been combined to produce a technology demonstrator. As application, the realisation of a fully functional flexible and stretchable watch was chosen. Electronics on polyimide film, a flexible substrate, are combined with moulding technology. Also a method to make the flex substrate more stretchable was shown. Display and necessary electronics were embedded in a stretchable silicone bracelet.

First a short summary of the thesis is given, from system design over the fabrication of the flexible prototype to the stretchable version. Finally a more detailed view on the interconnection technology used for the assembly of the displays is elaborated.

3.2.1 System Design

The watch system is built around the Texas Instruments MSP430f413 16-bit microcontroller, as shown in Figure 3.7. The design uses the MSP430´s on-chip timer to implement a Real-Time Clock (RTC). This way no external RTC-chip is

needed. The crystal oscillator, a 32.768 kHz watch-crystal, is used as the clock source for the timer/counter that serves as the time base.

The time is displayed on a rigid, 4-digit, 7-segment LCD-display. Driving the LCD-segments is achieved by using the microcontroller´s on-chip LCD-driver. User operation of the watch is done through the use of three buttons:

- Mode: Allows the user to select between setting minutes, setting hours, displaying time.
- Set: According to the mode, minutes or hours are increased.
- On/Off : Used to switch display on/off. Switching the display off, reduces power and extends the demonstrators battery life. The real-time clock is still updated when the display is disabled.

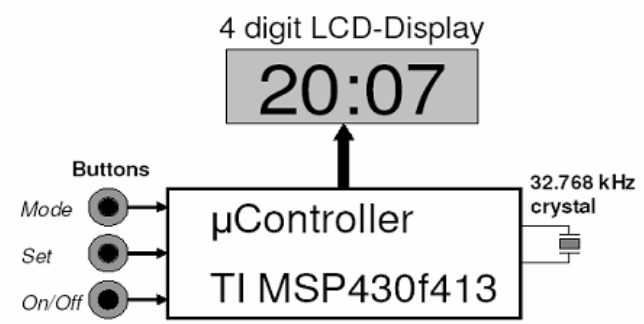

Figure 3.7: System design of the watch demonstrator

3.2.1.1 Components

To achieve a compact and thin demonstrator, small components are needed. The MSP430 microcontroller has a 64-pin Quad Flatpack No-lead package (9.1mm x 9.1mm x 0.9mm). The 32.768 kHz watch crystal has a thin SMD-package (3.3mm x 1.6mm x 0.9mm). Ultra-low Profile Dome Keys are used as switches (0.3mm thickness). The LCD-display has also acceptable dimensions (23.77mm x 13.7mm x 2mm). But finding a useful, thin and compact battery was the biggest problem. A 3V lithium-ion coin cell is used (diameter 12.5mm; height 2mm). The battery has a typical capacity of 16mAh and is provided with leads for SMD attach.

3.2.1.2 Power concernings

Due to the low battery capacity, a good low-power design is needed to ensure some battery lifetime. Therefore the low-power modes of the MSP430 controller

are used. The main loop of the implementation runs once every second, prompted by an interrupt. Between interrupts, the device is in low-power mode, resulting in very low power operation. Due to this way of programming the demonstrator uses about 2 μA, and $\sim$1 μA when the display is disabled. This gives about 1 year battery lifetime with the display switched on. So far, a prototype on display at the lab is still functioning, after 16 months of continuous operation (with the display switched on).

3.2.2 System on Flex

The watch circuit is fabricated on a flexible polyimide foil (thickness 25 μm). Lithography and wet etching of Cu (9 μm) are used. The flex is covered with soldermask by screenprinting (20 μm). Contacts are finished with Ni/Au plating. The flex-design was made single-sided. The circumference of the watch and a rectangular sparing for the display have been cut with a Nd-Yag laser beam. Anisotropic conductive adhesive (ACA) was used to bond the display on the flex. This way there is a direct attach of the display on the flex, which leads to a result as thin as possible. An assembled flexible watch is shown in Figure 3.8.

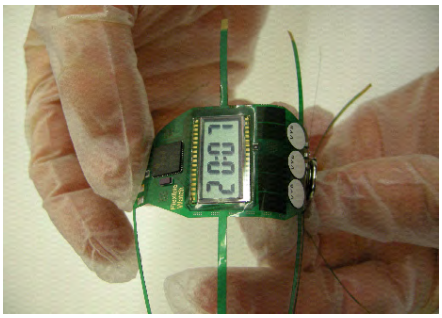

Figure 3.8: An assembled flex watch

3.2.3 From Flexible to Stretchable

Starting from the flexible circuit, a stretchable circuit was made. The stretchable electronic circuit is considered as a number of flexible component islands, connected by elastic interconnections. Stretchable interconnections are achieved by lasercutting meander shaped wires out of copperplanes on the flex. The wires are 100 μm wide. A result of a stretchable adaptation is shown in Figure 3.9.

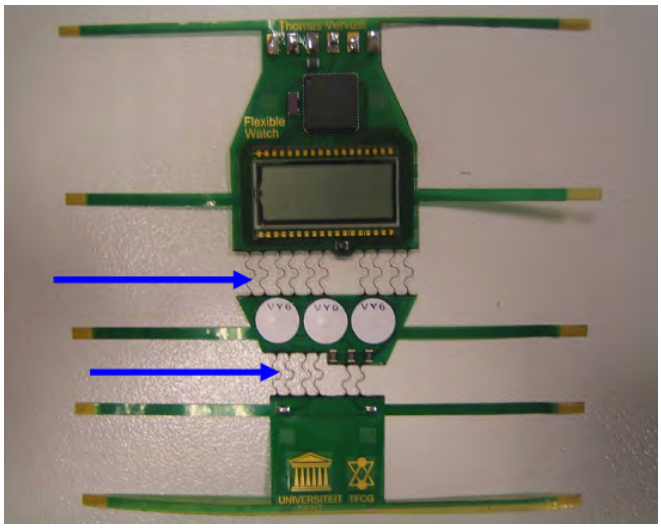

Figure 3.9: The stretchable adaptation of the flex version: note the meander shaped interconnections

To protect the components and the fragile meander structures, the entire watch circuit is embedded in a stretchable, transparent silicone. The silicone is moulded in the shape of a wristband. Three moulds are used to embed the watch circuit in two stages. First the upper part of the watch is moulded, using a mould for the upper shape and a mould as carrier. Next the lower part is moulded with the mould for the upper shape and a mould for the lower shape. In Figure 3.10, a picture shows the final result of the technologies demonstrator. The dimensions of the watch demonstrator are shown in Figure 3.11.

Figure 3.10: A resulting watch demonstrating a range of technologies

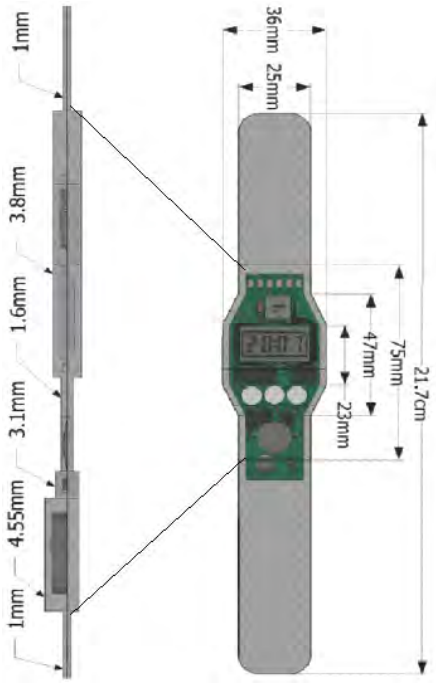

Figure 3.11: Dimensions of the watch as defined by the designed moulds

3.2.4 Resulting Demonstrator

The idea behind the thesis was to show how these advanced technologies can be used to reduce size and weight of electronics for portable applications, in this case a wristwatch. It is indicated that the choice of components, substrates and interconnection methods are very much the defining factors here, rather than the intended functionality and system design. This is nicely illustrated in Figure 3.12.

3.2.5 Display Interconnection

The display chosen for the demonstrator was a standard segmented glass liquid crystal display, commercially available from Varitronix. The layout schematics are shown in Figure 3.13. The display has two sides with contacts, all at a pitch of 1270 μm. The routing pattern on the flex, connecting microcontroller and display, is shown in Figure 3.14. The rectangle indicates the area that has to be cut out of the flex, so that it fits the rear glass substrate of the display. The close-up shows how soldermask had to be used for interconnection, since single-sided routing was preferred on the flex substrate.

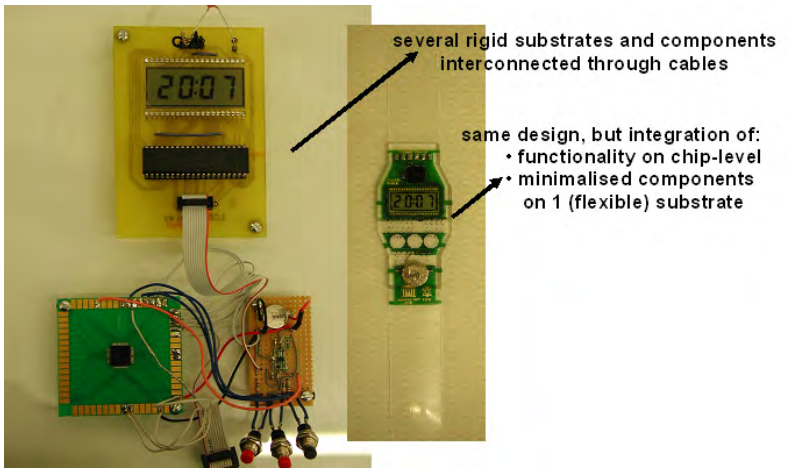

Figure 3.12: Illustration of how the choice of interconnection technologies defines size and weight of electronics: the two pictures are identically scaled

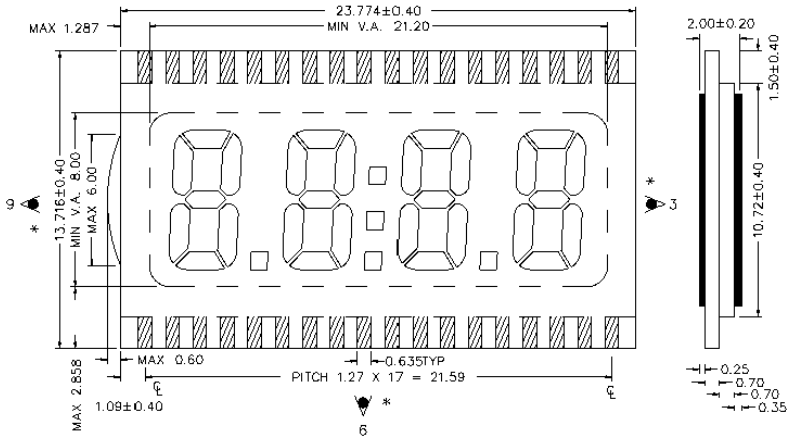

Figure 3.13: Layout schematics of the VI-451(R0) Varitronix LCD display (dimensions in mm)

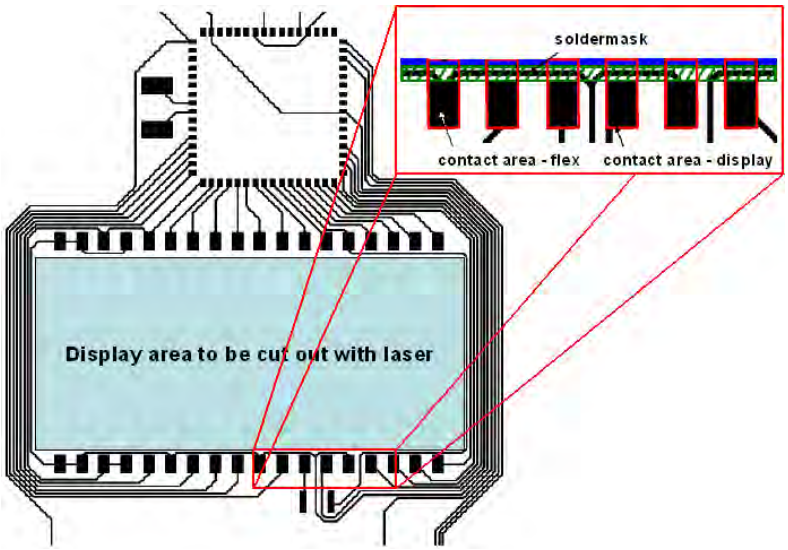

Figure 3.14: Routing pattern for interconnecting microcontroller and display on a single-sided flex substrate

The interconnection itself was realised through bonding with ACF. The principle is once more illustrated in Figure 3.15. Some issues came up. The bonding setup had to be adapted for the displays used. At first, bonding was carried out on a flat surface, but this led to breakage of the displays: during bonding, shear stress was introduced due to the polarizer film. Next to this, when uneven bonding pressure is applied by the thermode, there is a risk of the glass cutting off the flex substrate, especially in the corners of the cut-out area, as the stress will be most concentrated there. Also, overall excessive heat is to be avoided, because then the polarizer film gets damaged. On the other hand, if the heat is only applied locally, no such problem was noticed, probably thanks to the heat insulation properties of the glass substrates. These issues are clarified in Figure 3.16.

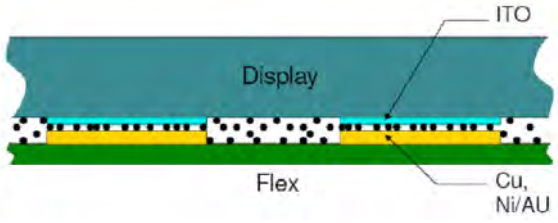

Figure 3.15: Principle of ACF for bonding the watch displays

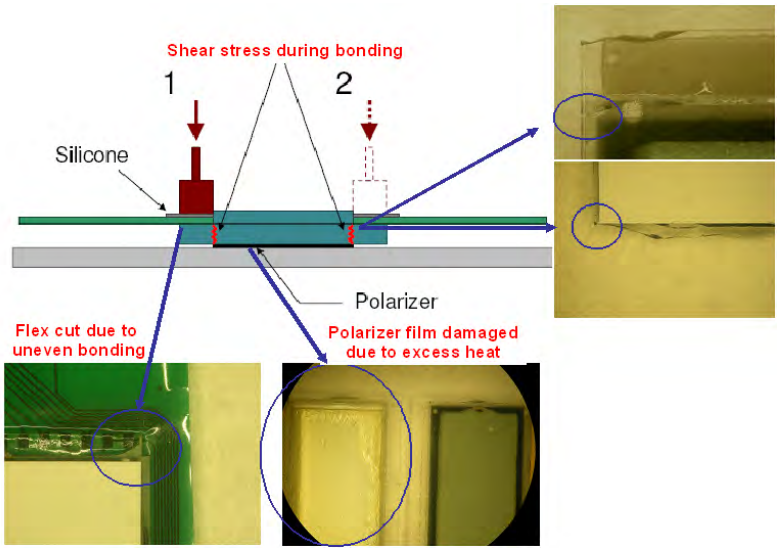

Figure 3.16: Issues with the initial bonding setup

To solve the issue of breakage, a setup was constructed on a ceramic substrate. Two supporting ceramic blocks were used to relieve any shear stress on the front display substrate. The setup is shown, schematically and actually, in Figures 3.17 and 3.18 and proved to be successful. A close-up of the resulting bond can be seen in the picture in Figure 3.19. The 0.2 mm silicone interlayer was added to more evenly distribute the thermode pressure, when it was clear that without interlayer, randomly some contact pads were not interconnected.

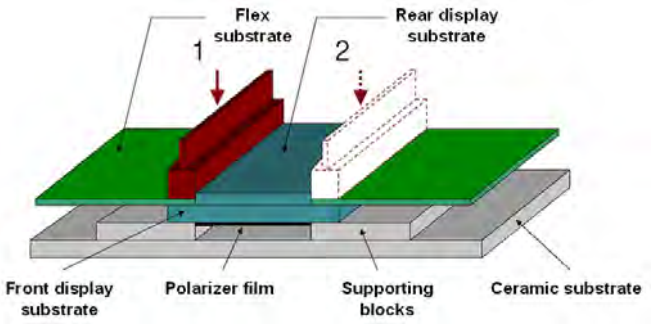

Figure 3.17: Adapted setup for bonding the watch displays: schematic

Bonding was done with a pressure buildup from 1 to 2.8 bar, and a temperature buildup from 50 to 170°C.

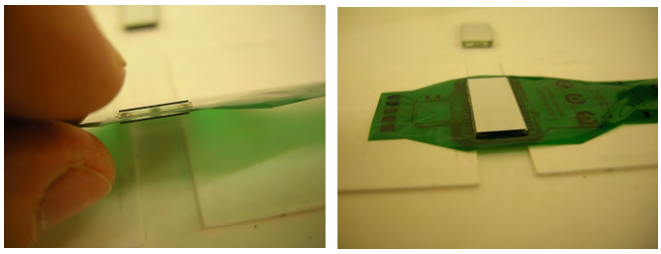

Figure 3.18: Adapted setup for bonding the watch displays: actual

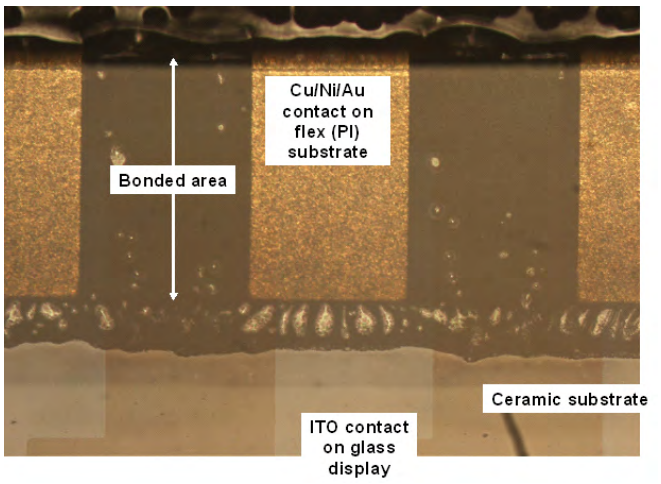

Figure 3.19: A close-up of the resulting display bonded to the flex substrate with ACF

3.3 Sensor Matrix

Previous examples involved interconnecting rigid glass displays to a flexible substrate, routing the display contacts to the electronic components of the driving circuitry. Here, a device built up on a glass substrate is directly interconnected to the naked chip that has to process the electronic signals of the device. The interconnection of chip to substrate is done through flip-chip assembly. The idea is to check if bonding the chip on top of the device will have any effect on the functionality of the device. Bonding is again carried out with ACF: it minimises the risk on damaging the devices thanks to the low-temperature curing, as well as offering the necessary fine pitch interconnection capabilities.

The device itself is a type of sensor matrix: an amorphous silicon (a-Si) hybrid detector, where an array of 256 photodiodes provides the input for image detec-

tion. Although admittedly, this is not a display[3], a detector matrix can, with some goodwill, be considered the inverse of a display: whereas in a display, data supplied by the user is shown (displayed) to the environment, a sensor receives its data-input from the environment and shows it to the user.

The tests were carried out as subcontracted work for Rome's Sapienza University[4] for the research project "Hybrid Detector Technology" financed by the Italian Ministry of University in the framework of the project "Rientro dei Cervelli".

3.3.1 Setup

The schematical structure of the device is given in Figure 3.20. The common conductive layer for the 256 photodiodes is provided by a transparent conductive oxide (TCO), the photodiodes are built on a large area and their output signals are read by an integrated circuit realized in VLSI connected to the photodiodes through two conductive routing layers, 200 nm thin layers of CrAlCr and TiW. An 8-μm-thick layer of BCB acts as insulator between the conductive layers. The last step consists in the realization of interconnection between the output pads and the pads of the chip.

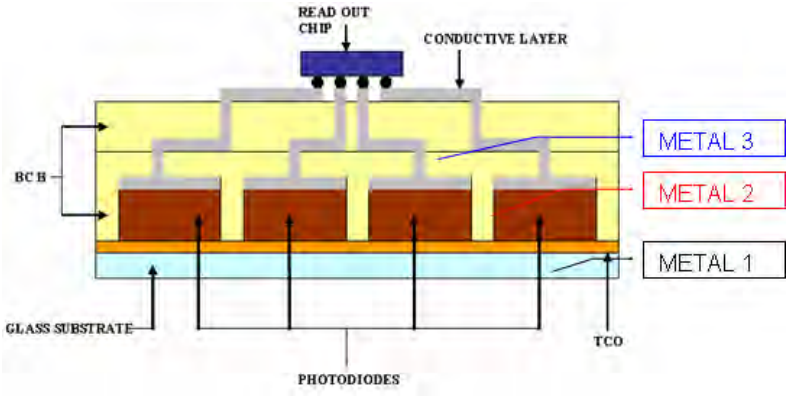

Figure 3.20: A schematic crosssection view of the detector structure (Patent application: A. Nascetti, M. Overdick, WO2003019659, "Sensor arrangement consisting of light-sensitive and/or x-ray sensitive sensors", Koninklijke Philips Electronics N.V.)

The read-out chip to be connected is the ISC9717, built by the Indigo System Corporation, and usually used for X-ray detectors readout. The ISC9717 is shown in Figure 3.21. It was supplied as bare die without bumped pads. For ACF bonding

[3] while this Chapter clearly describes itself as "Rigid Displays"
[4] Dipartimento di Ingegneria Aerospaziale e Astronautica

however, bumps are required, so it was decided to have them bumped with gold (Au) studbumps. Some pictures of these are given in Figure 3.22.

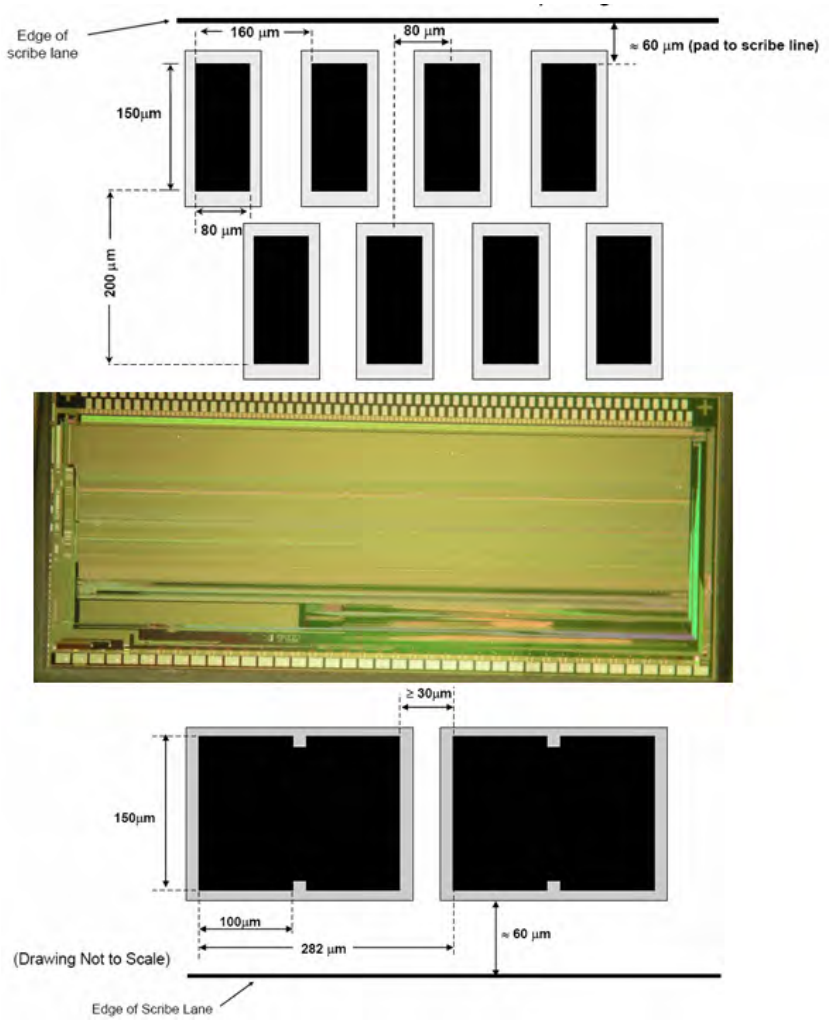

Figure 3.21: The read-out chip ISC9717: input pads (top) are staggered 160 µm by 80 µm pads at a pitch of 160 µm, while the output pads (bottom) have the approximately the same size (150 µm by 100 µm) but have been paired up at a pitch of 282 µm

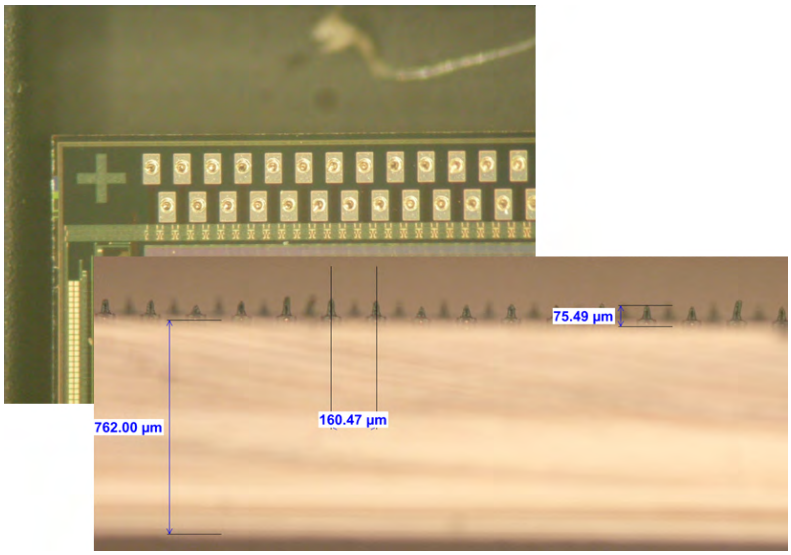

Figure 3.22: The input pads of the ISC9717 after bumping: the Au studbumps have a height of approximately 75 µm

The chip has 128 input channels, so two chips are needed on the substrate to read the signal of all 256 photodiodes, as is shown in Figure 3.23. With the red circle are marked the output pads of the sensor, to which the 128 input pads of the chip have to be contacted. The output signals of the chip have to be connected to the pads marked in green.

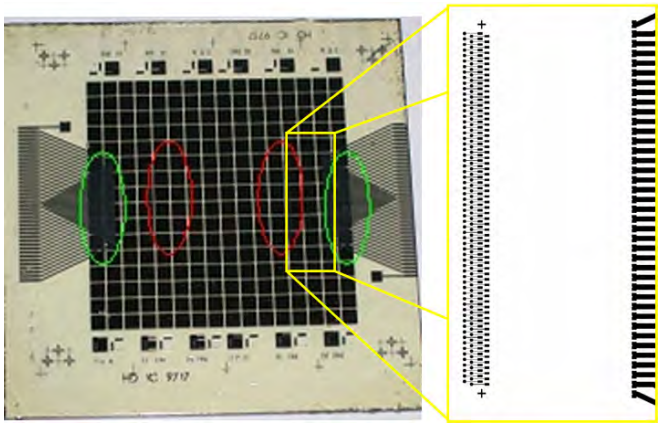

Figure 3.23: The detector substrate: a matrix of square photodiodes is visible, and the patterns where the read-out chips have to be bonded are marked and shown up-close (as designed)

3.3.2 Bonding trials

Instead of directly trying to bond fully functional substrates and chips, some trials were done first to test the device functionality after bonding. For this, available test chips were used and matching substrates were fabricated.[5] The chips measured 2.5 mm by 15 mm and had peripheral contacts pitched at 200 μm. They were bumped with NiAu, approximately 5 μm thick. As for the substrates, small (0.5 mm by 0.5 mm) and large (1 mm by 1 mm) photodiodes were incorporated at different places under the bonding area to test the influence of bonding.

The bonding process is described in Table 3.1, with the used temperature profile during bonding as shown in Figure 3.24. The process itself is illustrated in Figure 3.25.

step #	step	remarks
1	clean substrate and chip	with isopropanol
2	cut and apply ACF on substrate	slightly larger than bond area for homogeneous bonding
3	pre-bond ACF	4s @ 90°C, 1mm silicone interposer
4	remove ACF release film	
5	align chip to substrate and place chip	calibration beforehand concerning mirror tilt
6	align chip to thermode and bond chip	30s @ 170°C, 2.5 bar, 0.2mm silicone interposer

Table 3.1: The sensor matrix bonding process in words

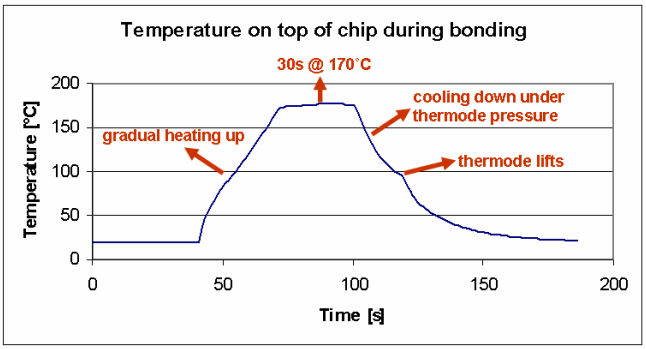

Figure 3.24: The temperature profile on top of the chip during thermocompression

[5]The test chips are the ones developed and used in Section 4.2.1

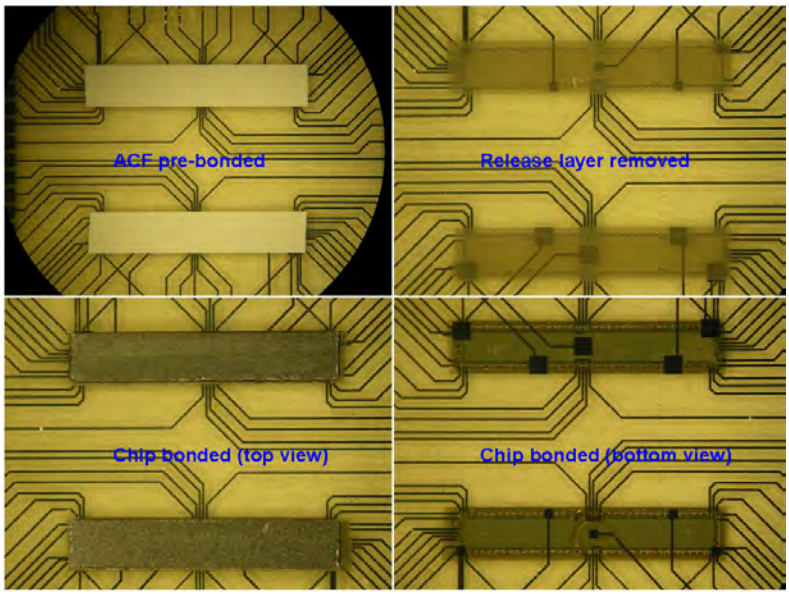

Figure 3.25: The sensor matrix bonding process in pictures: the small and large square photodiodes are visible underneath the chip (under the middle of the chip as well as underneath the peripheral bond pads themselves)

3.3.3 Results

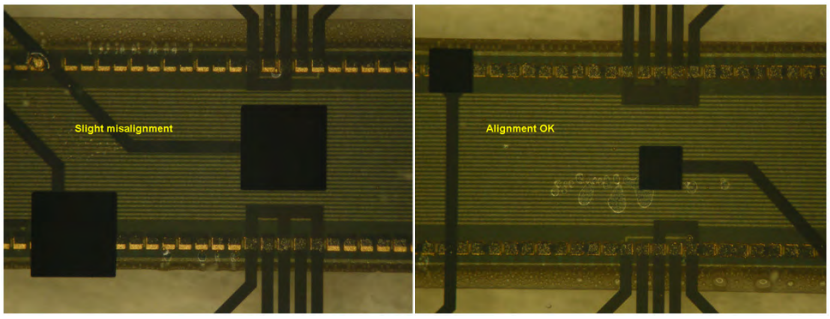

Figure 3.26: Some close-up results of the bonding trials: note the slight misalignment on the left, and the indentations on the contact pads (these are marks caused by the ACF's metal particles being pressed into the thin contact pads on the substrate during thermocompression)

Some pictures of the results of the bonding trials are shown in Figure 3.26. Optically and electrically the interconnection was successful: the daisy chain formed

by peripheral bond pads and matching substrate patterns could be measured, and the slight misalignment was acceptable. As for the photodiodes, they were measured before and after bonding, and no difference was noticed. An example of these measurements is given in Figure 3.27.

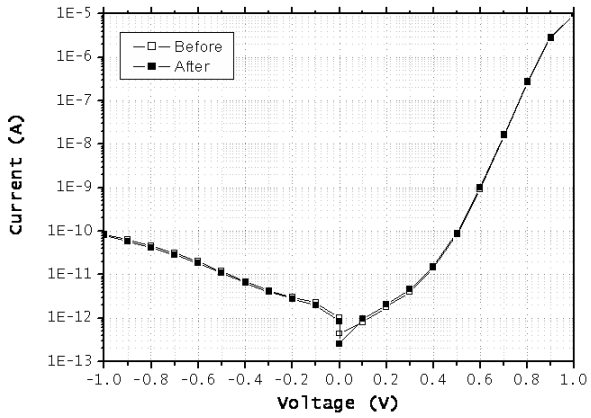

Figure 3.27: Current-Voltage characteristic in dark conditions of a photodiode before and after the flip-chip process

3.3.4 Demonstrator bonding

With the success of the trials in mind, some demonstrator substrates, with large and small photodiodes, Figure 3.28 were assembled. Figure 3.29 illustrates the assembly process, while Figure 3.30 shows some pictures of the resulting demonstrators.

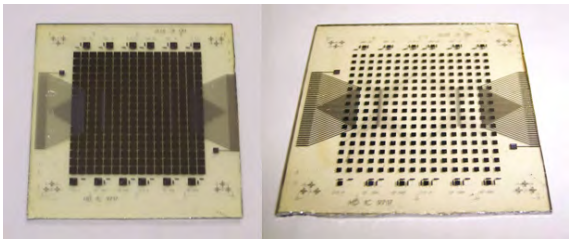

Figure 3.28: Two types of demonstrator substrates were used: large photodiodes (left) and small photodiodes (right)

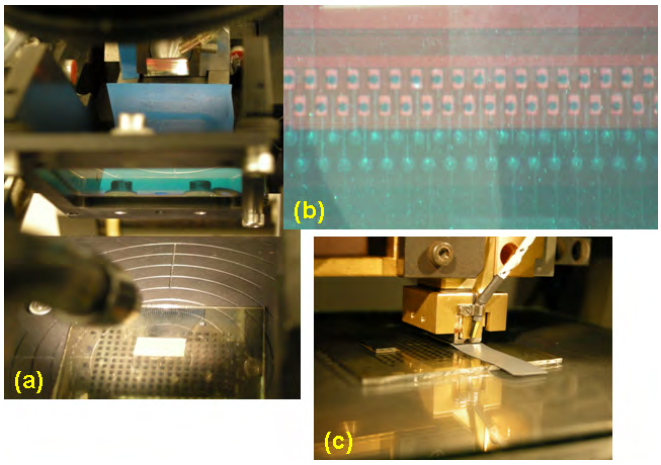

Figure 3.29: Illustrations of the assembly process: (a) the aligning and placing setup (beam-splitter in the middle, chip at the top, picked up by the chuck and substrate at the bottom of the picture) (b) a view through the aligner microscope (the round contours are the studbumps) (c) the thermocompression step (on the left one chip is already assembled, on the right the silicone interlayer covers the chip during thermocompression)

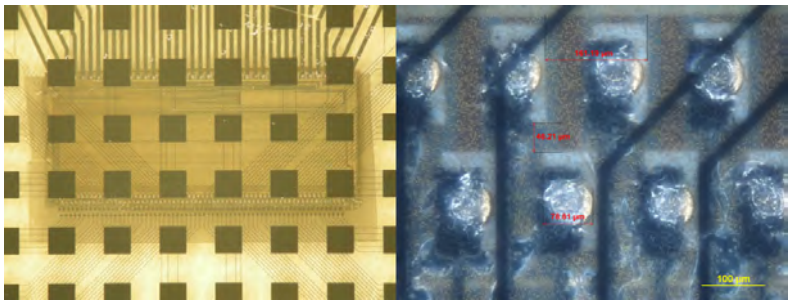

Figure 3.30: Results of the assembled demonstrators: an ACF bonded chip (left) and a close-up of the input area of the read-out chip (right, the studbumps are aligned to the contact pads on the substrate)

3.4 Helmet Display

HeMind, the acronym for Helmet-mounted Miniature INformation Display system, is a European project intended to develop a helmet system for fire-fighters, equipped with a high-resolution miniature viewer and an autonomous, portable computer system capable of presenting, overlapped to the normal viewing field of the user, images from a video camera (thermal images, standard images) as well as data from sensors integrated in the clothes of the user or received through

a radio-communication system. Within the frame of this project, passive-matrix liquid crystal displays were assembled with glass substrates, and these had to be interconnected to the driving electronics.

The interconnection for these systems combines the technologies used in the above sections: both interconnection of flex substrates to glass displays and direct flip-chip assembly of naked driver chips onto glass substrates are involved. First, the needed components and substrates are discussed, then the full fabrication process for the display system is explained, and finally the encountered bonding issues are somewhat more elaborated.

3.4.1 Materials, Components and Substrates for the Complete Assembly

The glass substrates for the display fabrication are 0.7 mm thick and carry a 20-nm-thick ITO layer, patterned with rows and columns at a pitch of 31.25 μm in the display active area. The ITO bonding pads for the chips and flex foils have been covered with 50 nm TiW and 100 nm Au, for improved visibility during aligning, as ITO is inconveniently transparent at this point. Examples of column and row substrates are shown in Figure 3.31.

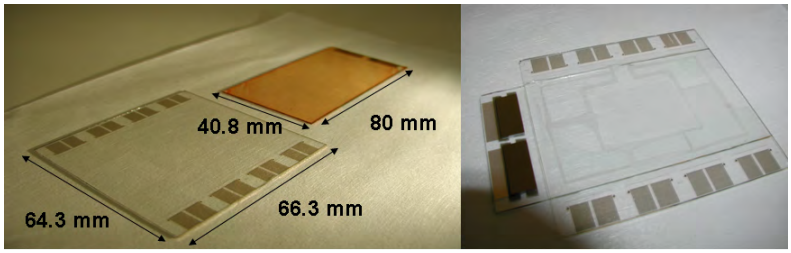

Figure 3.31: Glass substrates for display fabrication: a column substrate on the left and a row substrate on the right (left picture) are used to fabricate a HeMind display (right picture); the row substrate in the left picture is still coated with photoresist for protection during polishing, explained in Section 3.4.3; the display active area is visible at the center of the assembly in the right picture

The driver chips used are column drivers from Clare Micronix, commercially available, and row drivers designed at the lab. The column drivers "MXED401" measure 1.76 mm by 12.83 mm, and have 83 inputs at a pitch of 110 μm and 200 outputs at a pitch of 60 μm. The row drivers "Mjöllnir" measure 6.6 mm by 15.75 mm, and have 60 inputs at a pitch of 260 μm and 300 staggered outputs at a pitch of 120 μm. The column drivers have 15 μm high Au bumps, and the row drivers have been studbumped using Au wire. Some pictures are given in Figures 3.32 and 3.33.

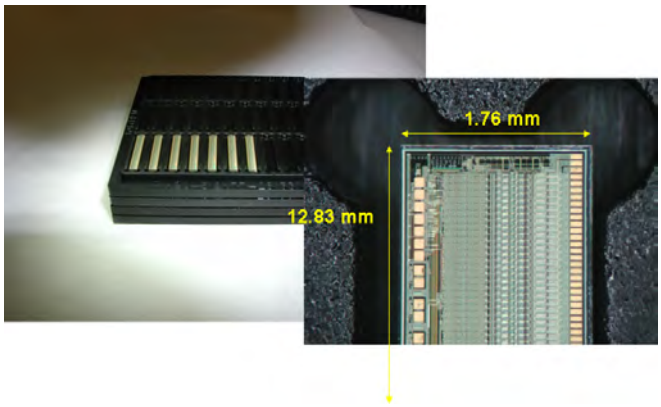

Figure 3.32: The column drivers used for the HeMind display

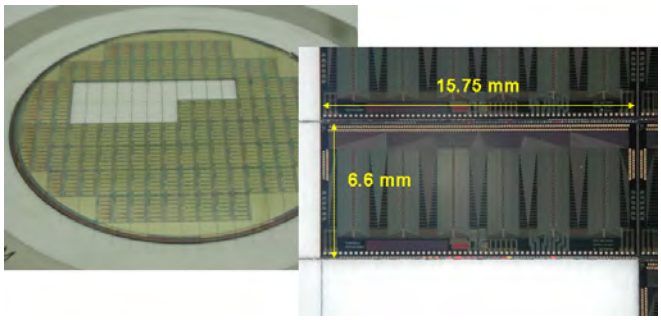

Figure 3.33: The row drivers used for the HeMind display

For contacting the inputs of row and column driver chips, standard flex foils were patterned at 300 μm and 260 μm for the column and row inputs respectively, as indicated in Figure 3.34. The flex foils, unpatterned, are Upilex-25S from UBE, and consist of 25 μm PI covered with 9 μm Cu. As no soldermask is applied, the Cu is plated with a few μm of Ni and a Au flash to protect it from oxidation and corrosion.

PCBs for rerouting to a cable connector were designed and outsourced for manufacturing. As can be seen in Figure 3.35, a hole was made in the center of the PCB for the active area of the display, as the HeMind display is intended for through-display viewing, overlapping with normal vision.

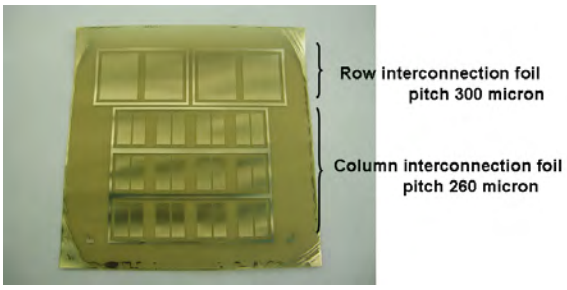

Figure 3.34: Patterned flex foils for interconnecting driver inputs (row and column) to the underlying PCB

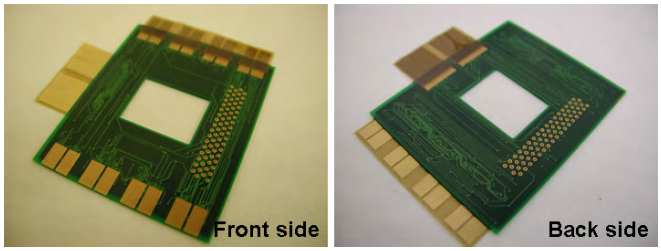

Figure 3.35: The underlying PCB for rerouting all driver input signals from a cable connector to the appropriate drivers

3.4.2 Display Fabrication Process

The sequence for assembling the HeMind module, interconnecting the rows and columns of the display to the cable connector, via the drivers, is a bit complex, at least as compared to most other display module assemblies, as in this case double-sided flip-chip, and double-sided interposer flex attachment is involved, and is described in Table 3.2. The design for the resulting module is shown in Figure 3.36, and the assembly sequence is illustrated schematically in Figure 3.37.

step #	step
1	bonding trials
2	bonding column drivers (8)
3	bonding row drivers (2)
4	bonding column flex to glass (2)
5	bonding row flex to PCB (1)
6	glueing glass (display) to PCB
7	bonding column flex to PCB (2)
8	bonding row flex to glass
9	testing assembly…

Table 3.2: The assembly sequence for the HeMind module, described in words

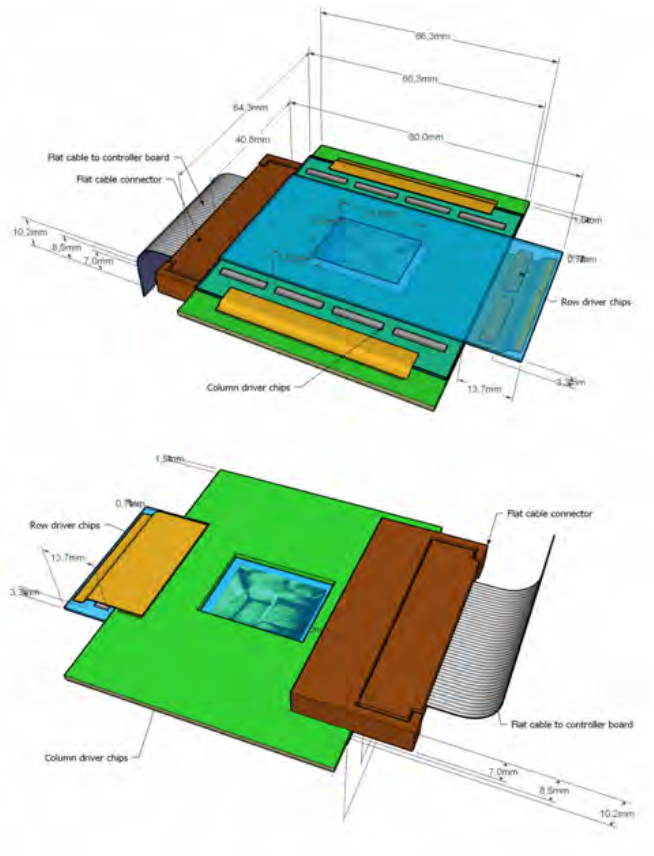

Figure 3.36: The designed end result for the HeMind module

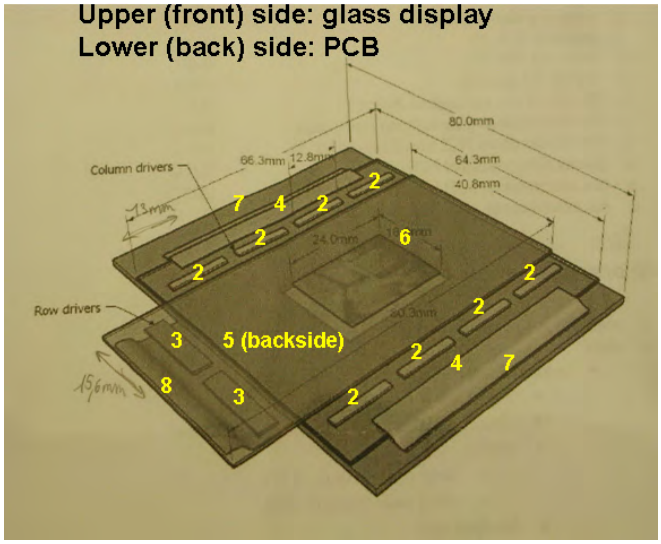

Figure 3.37: The assembly sequence for the HeMind module, illustrated on the design

Before starting an actual assembly, all bonding steps were tested separately to acquire a satisfying set of bonding parameters. The bonding for these tests were carried out on separate glass substrates, as shown in Figure 3.38 so that the resulting assemblies could easily be checked optically from the backside. Based on these tests, the bonding specifications, as described further on in Tables 3.3 and 3.4, were determined.

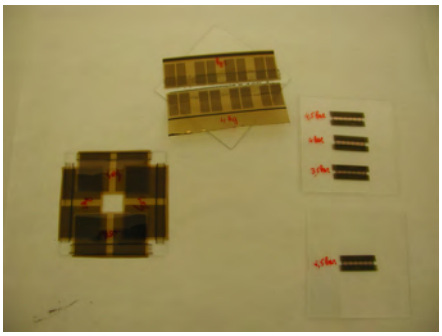

Figure 3.38: Bonding tests on glass

The specifications for bonding the column and row driverchips are given in Table 3.3. Pictures illustrating the result and the process are shown in Figures 3.39 and 3.40.

driver type	bonding	contact pad height [μm]	ACF thickness used [μm]
column drivers	30s @ 300°C, 3.5 bar	15	23 (1 layer)
row drivers	30s @ 300°C, 4.5 bar	70	69 (3 layers)

Table 3.3: Bonding specifications for the driverchips

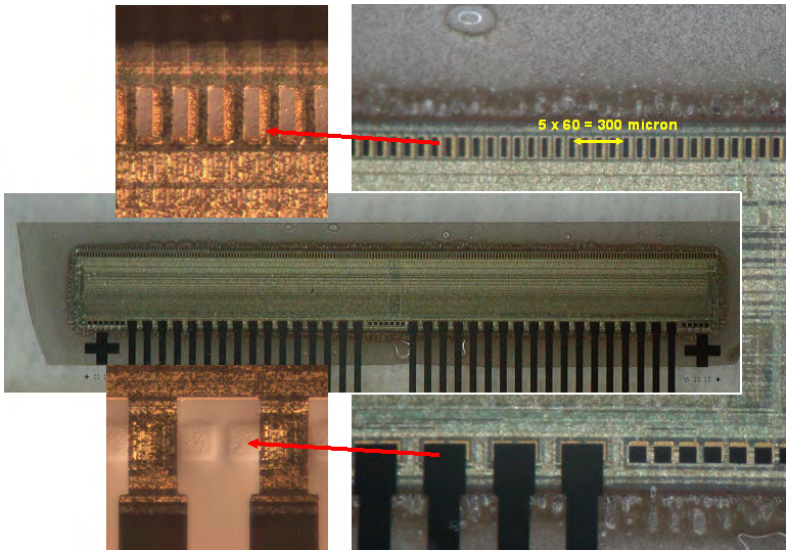

Figure 3.39: Column driver chips bonded to the display

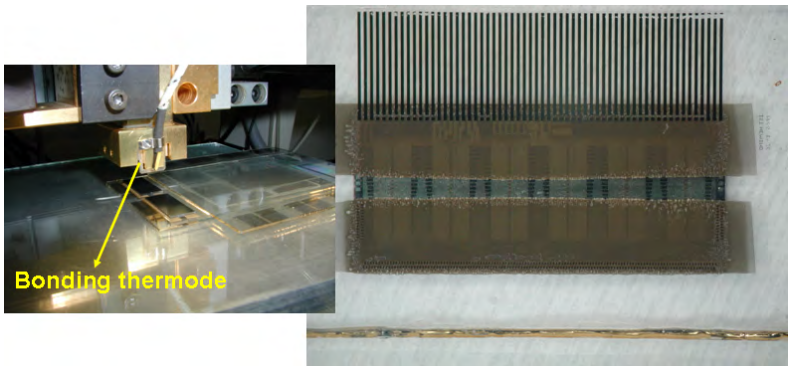

Figure 3.40: Row driver chips (being) bonded to the display

As for the flex foils, they each have to be bonded twice: one side to the glass display substrate patterned with a thin ITO/TiW/Au-layer ($\sim$0.2 μm), the other

side to the PCB patterned with a thick Cu/Ni/Au-layer (∼50 μm). The specifications here are given in Table 3.4, some pictures in Figures 3.41 and 3.42. In between these steps, for improved robustness of the assembly, the display is glued to the PCB. This is done with a 2-component epoxy adhesive, the standard combination of a resin and a hardener, that was cured at room temperature for 24 hours. The adhesive is of course not applied at the active area of the display (as it matches the hole in the center of the PCB). Pictures of this are given in Figure 3.43.

bond type	bonding	contact pad height [μm]	ACF thickness used [μm]
column flex to glass	30s @ 300°C, 4 kg	10	23 (1 layer)
row flex to PCB	30s @ 300°C, 3 kg	60	69 (3 layers)
column flex to PCB	30s @ 300°C, 4 kg	60	69 (3 layers)
row flex to glass	30s @ 300°C, 3 kg	10	23 (1 layer)

Table 3.4: Bonding specifications for the flex foils

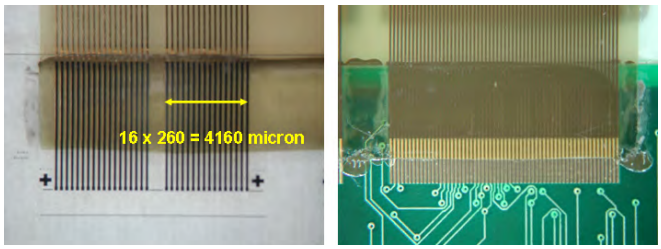

Figure 3.41: Flex foils bonded: column flex to glass (left) and row flex to PCB (right)

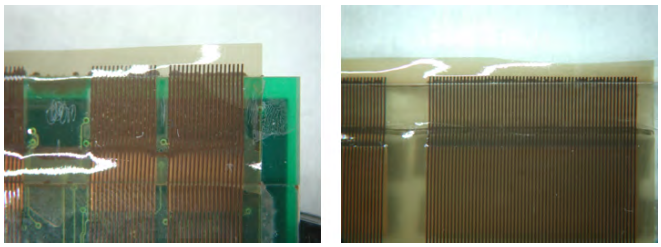

Figure 3.42: Flex foils bonded: column flex to PCB (left) and row flex to glass (right)

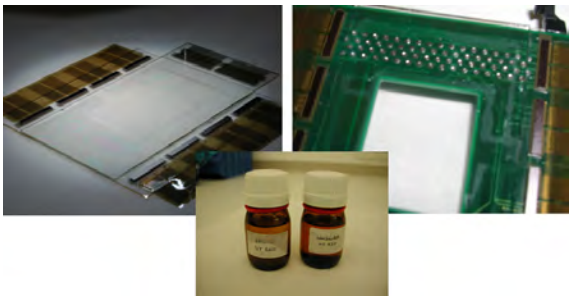

Figure 3.43: The status of the display assembly before (left) and after (right) gluing the display to the PCB; the 2-component epoxy adhesive is shown in the middle

The final result of the assembly is shown in Figure 3.44. The white ceramic is attached to the front display substrate, to protect the active side of the row drivers from UV-light. The column drivers are UV-sensitive as well, but they are already protected by the PCB in the complete assembly. The connector is pre-assembled to the PCB. The reason for this is that it is through-hole soldered, and the temperatures used in this process would most probably inflict considerable damage to the liquid crystal inside the display.

After completing the assembly, the modules are tested in the lab, as shown in Figure 3.45.

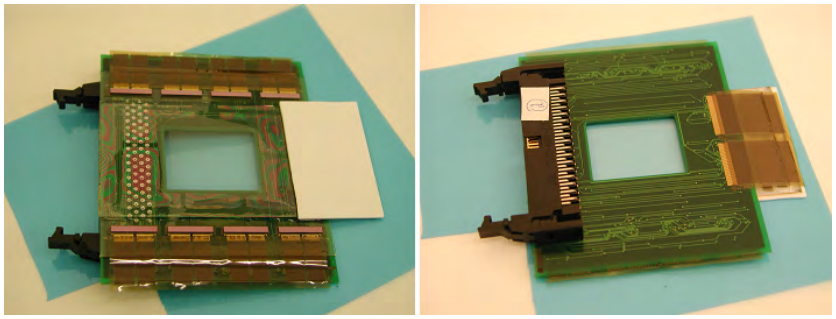

Figure 3.44: The final HeMind module seen from the front (left) and the back (right)

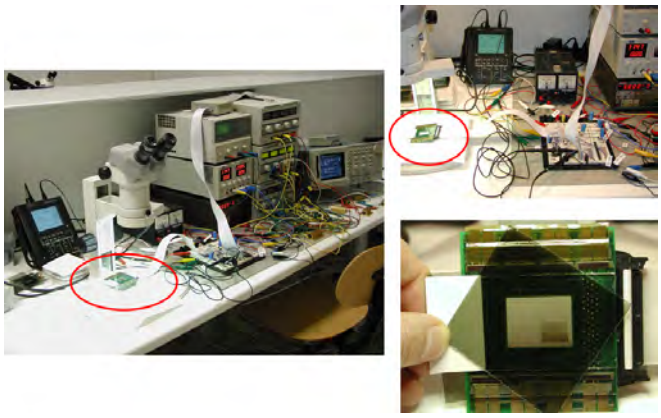

Figure 3.45: The complete setup dedicated for driving the HeMind module

3.4.3 Bonding Issues

Unfortunately, the result of the above assembly sequence was not completely successful. A few bonding issues were encountered and are illuminated in this section.

The alignment of the column driver chips was feasible but difficult, as the pitch of the outputs (60 μm) nears the lower limit of the align and place equipment available at the lab.

Slight delamination occurred at the sides of the flex foils bonded to the PCB contacts. This is probably due to the ACF, since it is not a type optimized for PCB bonding. As long as the assemblies were handled carefully, there was however no problem with electrical interconnection.

Although the row drivers are less critical in feature size, alignment was still difficult, because three layers of ACF had to be used. This thick ACF layer means the thin ITO/Au pattern on the glass substrate is only barely visible through the microscope.

In the described process, all too often, the front glass display substrate cracked when bonding the row drivers. This can probably be attributed to three factors:

- the sharpness of the tips of the stud bumps will concentrate contact stresses and might induce very locally very high pressures on the glass;
- the row drivers are located very close to the glass edge;
- the quality of the glass used for the display fabrication.

From the look of such a crack, as shown in Figure 3.46, it seems that the crack is initiated at the glass edge. To try and solve this, subsequent assembly was done

with the same glass substrates, but polished at the edges beforehand. No significant improvement was noticed however. Under the assumption that the bumps were to blame then (they are definitely different from the bumps of the column drivers, as illustrated in Figure 3.47), tests were done to flatten the row driver studbumps, and at the same time bonding pressure was lowered to 3.5 bar. The flattening was carried out with the chip on a test glass substrate, for 30 seconds under a pressure of 4.6 bar. Pictures before and after flattening are shown in Figure 3.48.

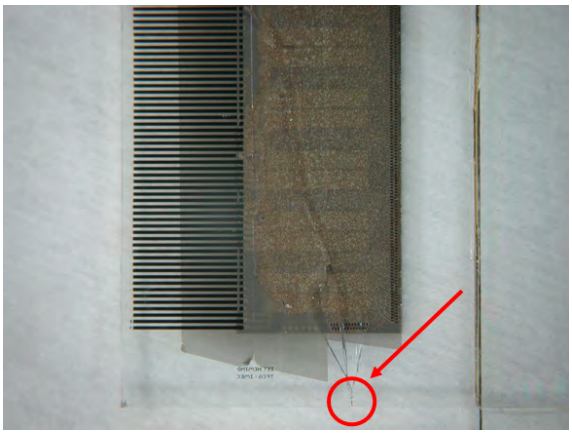

Figure 3.46: The crack in the glass originates from the glass edge

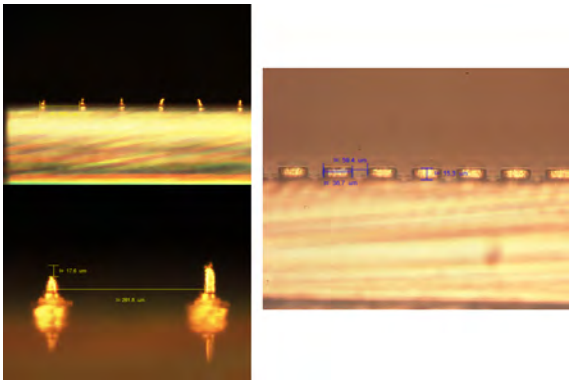

Figure 3.47: The highly irregular studbumps of the row driver (left), as compared to the flat, plated bumps of the column driver (right)

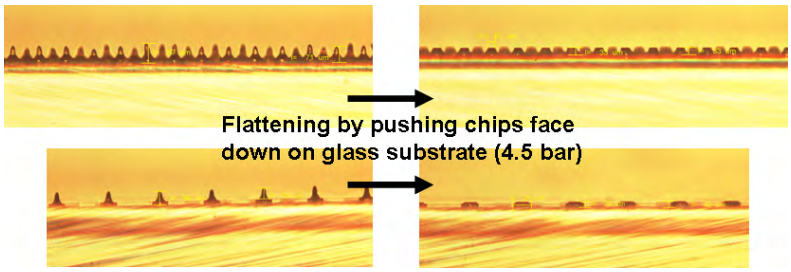

Figure 3.48: Flattening the studbumps to lower locally induced pressure during bonding

As the bumps are flattened, only two instead of three layers of ACF were used, increasing visibility and therefore beneficial for aligning. However, having the bonding pressure lowered, electrical interconnection was lost. This is clear when looking at the pictures in Figure 3.49.

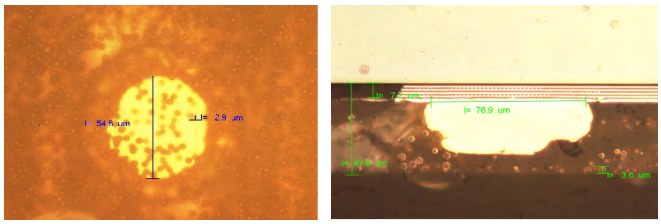

Figure 3.49: Through-the-glass-substrate view (left) and cross-sectional view (right) of an unconnected flattened bump

Due to ending of the HeMind project, resulting in a shortage of substrates, no more trials could be carried out unfortunately. As a conclusion, because no cracks or even remotely related problems were observed in the bonding tests done on the separate glass substrates[6], the main blame was finally laid in the combination of the overall quality of the used glass and the bonding locations being too close to the edge.

[6]which was another type of glass, but tests were done similarly close to the edge

4
Flexible Displays

"Any sufficiently advanced technology is indistinguishable from magic."

— Arthur C. Clarke (1917 - 2008)

Usually, one of the main driving forces for commercial development[1] is to get as much benefit with as little effort as possible. Unsurprisingly, for displays, this is translated in a clear trend to grow larger in size, while at the same time lighter, so that a maximal viewing area is achieved with minimal excess material. This way, CRT displays are being replaced by flat panel displays, and the current glass-based ones will be replaced by even lighter ones.

This line-of-thought also indicates that the prime motivation for commercially developing flexible displays is not so much the flexibility, but rather the lighter weight and the thinner form-factor. This is not to say that flexibility is not considered as an upgrade, but at this point people still have to get used to the possibilities, so that, as with most new developments, it is difficult to predict what the impact will be on the existing market. Another important motivation concerns the fragile nature of glass: almost everybody is taught the dangers of broken glass as a young child and how to be extremely careful handling it. Breakage is also a major concern when transporting glass, especially with the panels for displays growing larger and larger. Lastly, the use of glass also limits the size and speed of processing: the last generation of glass substrates is currently limited by the container size in which they are shipped around the world, and flexible substrates might offer the

[1] apart from any cost considerations, that is

possibility of roll-to-roll processing and the corresponding advantage of speed and high volume throughput.

Up to now, meaning in Chapter 3, examples of more or less standard[2] display assembly were elaborated to illustrate the terms and technologies explained in Chapters 1 and 2. Here, in this chapter, similar assembly technologies are used, but adapted for flexible display substrates.

4.1 Sensor Read-out IC Assembly

This example is a very basic one, and has nothing to do with displays, either flexible or rigid, but is included as a first introduction to assembly on flexible substrates. A (bumped) bare die is flip-chip assembled onto a standard patterned PI substrate with Cu routing layer. A double-sided soldermask is applied, two-sided to prevent curling with openings for the contacts, that have been plated with electroless NiAu. The chips measure approximately 1.6 mm by 1.6 mm, have a minimum contact pitch of 170 μm, and are basically sensor read-out ICs.

PI is a high-quality plastic that can withstand temperatures above 350°C, so no problems should arise from a thermode temperature of 300°C during ACF bonding. Pictures of the results are shown in Figure 4.1.

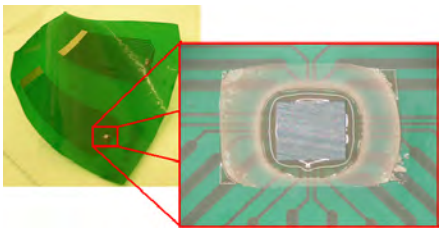

Figure 4.1: Chips assembled on a PI substrate

Two notable phenomena that were encountered, relate to the carrier substrate used. At first, ceramic substrates were used, but the high temperature and pressure, used during thermocompression, plastically deformed the backside soldermask, pressing it into the rough surface of the ceramic carrier. Although this should not pose any problem electrically, it makes checking the bond optically (alignment and quality of the bond) difficult. With a glass plate carrying the PI substrate, this problem is reduced. On the other hand, when glass was used, it was found that, sometimes, the backside soldermask was pinned to the carrier. This can most probably be attributed to the fact that glass is a better heat insulator than ceramic,

[2] or rather: rigid

so that the temperature of the backside soldermask is somewhat higher on glass than on ceramic, and some soldermask is pinned to the glass by the chip's bumps. The adhesion of the soldermask to the glass carrier is at this point apparently better than to the PI substrate. These phenomena are illustrated in Figure 4.2.

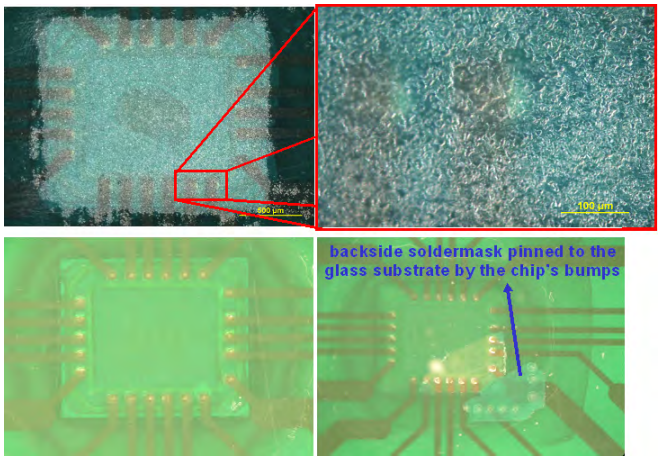

Figure 4.2: Illustrating the influence of different carrying substrates used during thermocompression: bonding carried out on a ceramic (top) and on a glass (bottom) carrier

The electrical functionality of these assemblies was not tested at our lab, and unfortunately, no feedback was received from the people requesting the assembly trials.

4.2 ePaper Display Assembly

References: [65], [66], [67], [68], [69]

Within the european FlexiDis project, an obvious acronym for Flexible Displays, different active-matrix flexible display technologies were investigated and developed, with the main focus lying on the industrial manufacturing of the displays themselves. Nevertheless, these displays have to be interconnected to the driving electronics.

One of the interesting technologies was proposed and is developed by Plastic Logic. Their display technology involves deposition of the active matrix through inkjetprinting of organic materials, so-called oTFTs (organic Thin Film Transistors), onto low-cost Au-patterned PET substrates, supplied by DuPont. On top of this backplane, a layer of electrophoretic ink, supplied by E-Ink, is laminated to

serve as the display effect, also referred to as the frontplane. Their technology is targeted for ePaper applications and is shown in Figure 4.3.

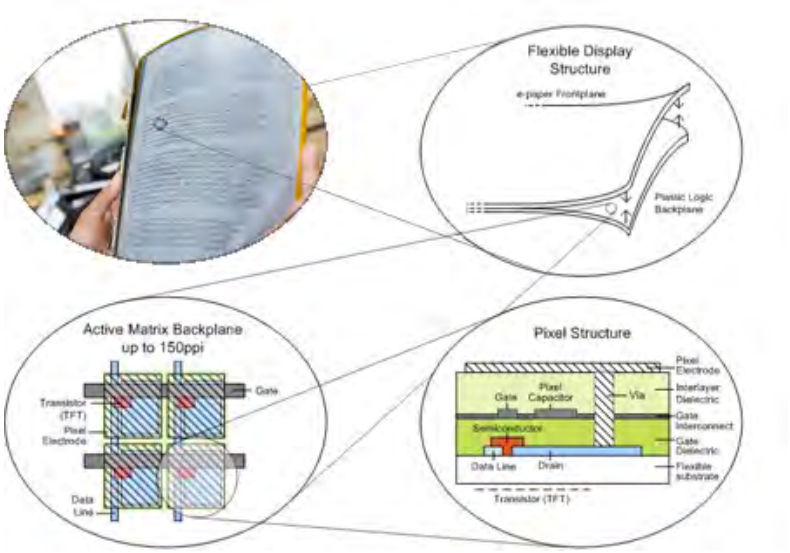

Figure 4.3: Plastic Logic's flexible backplane is combined with a frontplane material (e.g. electronic paper) to make a flexible display (from their website)

For interconnecting drivers to their kind of Au-patterned PET[3] substrates, a collaboration was setup for exchanging designs and substrates for bonding trials. Two interconnection methods were investigated: the first involves direct flip-chip assembly of the drivers onto the PET substrate, the second tries assembling drivers packaged as TCP (Tape Carrier Package, see Section 1.3.6). Both methods make use of the technology for bonding with ACF.

4.2.1 Flip-Chip Assembly

4.2.1.1 Test Setup and Design

In this option, the technology of directly assembling the driver chips on the display substrate, is investigated. To this end, tests were designed, where test chips are placed and bonded on the substrate, by means of the flip chip technique. Test chips and corresponding substrates were designed for different sizes and pitches. This is illustrated in Figure 4.4 and Table 4.1. The test chips are slim, as actual driver chips commonly are.

[3] low-cost, but also low-temperature

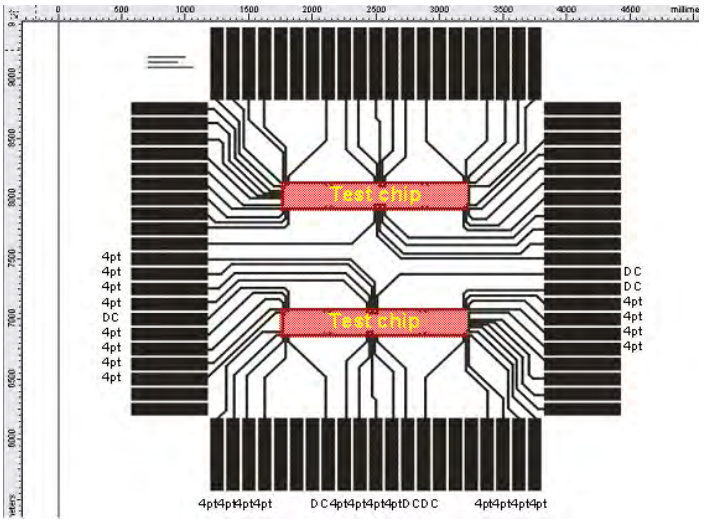

Figure 4.4: Test setup and design layout (example)

size [mm x mm]	pitch [μm]	# contacts	# 4-point structures
2.5 x 7.5	200	90	6
2.5 x 7.5	100	194	6
2.5 x 7.5	50	380	6
2.5 x 15	200	166	6
2.5 x 15	100	338	6
2.5 x 15	500	680	6

Table 4.1: Different sizes and pitches designed for FC tests

The patterns include daisy chains so that contact yield can be measured and 4-point structures for contact resistance measurements. The principle of 4-point measurements is illustrated in Figure 4.5: a "large" current I_{in}, in the order of 1 mA, is driven through two contacts, and the voltage V_{out} is measured in between the two neighbouring contacts. V_{out} is measured through a measuring current I_{out}, much smaller than I_{in}, typically below 1 μA. If I_{out} is small enough as compared to I_{in}, the first terms in the formula for V_{out} can be neglected and we find: $R_{contact} = \frac{V_{out}}{I_{in}}$.

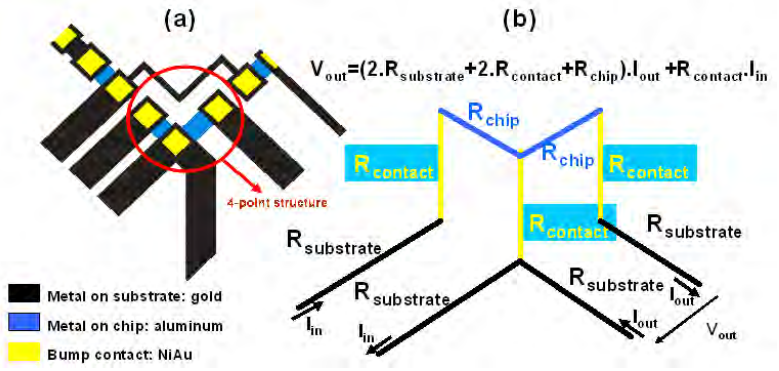

Figure 4.5: Principle of 4-point measurement: (a) top view and (b) "3D"-view explaining the principle

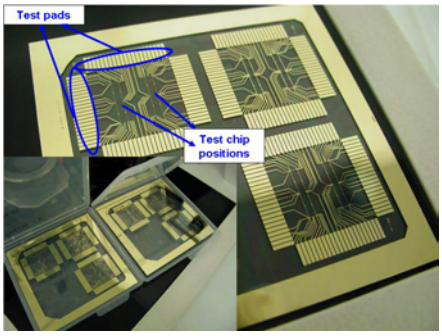

Figure 4.6: Pictures of Au-patterned PET substrates for flip chip tests

layer	deposition step #	thickness [μm]
Electroless Au plating	5	0.1
Electroless Ni bumping	4	10-15
PECVD Si_3N_4	3	0.4
Sputtered TiW + Al	2	0.02 + 0.5
PECVD SiO_2	1	0.4
Si wafer	0	700

Table 4.2: Layer buildup of test chips

The substrates were provided and patterned by Plastic Logic Ltd (PLL). They were 100 mm by 100 mm, approximately 150 μm thick, and mounted on a glass carrier. The metal pattern on the substrate consists of 60-100 nm thick gold. Fig-

ure 4.6 shows some pictures of those substrates. The test chips themselves were fabricated in-house, with the layer buildup shown in Table 4.2.

Two batches of wafers were processed. They yielded some good test chips for the coarser pitches of 200 and 100 μm. However, overplating and underplating, respectively in the first and second batch, in the bumping stage rendered the 50-μm-pitch test chips useless from an electrical point-of-view, as is illustrated in Figures 4.7 and 4.8.

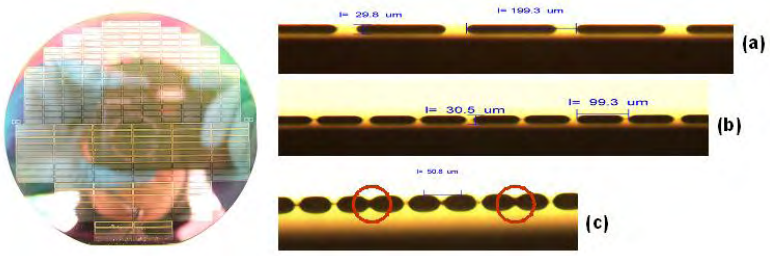

Figure 4.7: Resulting chips of the 1^{st} batch: pitches (a) 200 μm, (b) 100 μm and (c) 50 μm (overplated and shorted)

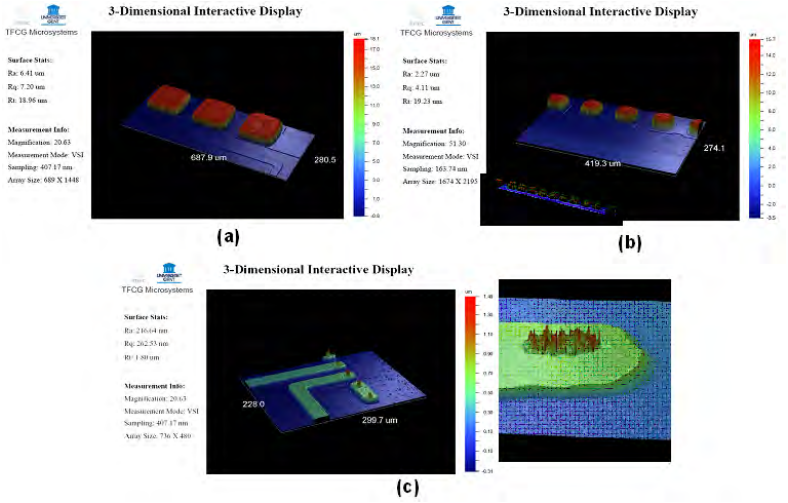

Figure 4.8: Optical inspection of the wafer surface, 2^{nd} batch, shows the results of the test chip bumping process: pitches (a) 200 μm, (b) 100 μm and (c) 50 μm (underplated)

4.2.1.2 Bonding Process

step #	process step	remarks
1	Clean substrate and chip	With isopropanol
2	Cut and apply ACF on substrate	Slightly larger than bond area for homogeneous bonding
3	Pre-bond ACF	4s @ 90°C, 1mm silicone interposer
4	Remove ACF release film	Should be easily removed
5	Align chip to substrate	Calibration beforehand concerning mirror tilt
6	Place chip	
7	Align chip to thermode	
8	Bond chip	30s @ 170°C, 0.2mm silicone interposer

Table 4.3: The bonding process

The actual bonding process consists of several steps. The sequence is given in Table 4.3. Pre-cleaning of the substrate is important as otherwise pre-bonding fails. Aligning the chip to the substrate and placing it is done with the semi-automatic flip chip aligner.

For the actual heat-bonding step, the placed chip (on the substrate) is aligned to the thermode. A 0.2 mm (thermally conductive) silicone interposer tape from ShinEtsu Chemicals is placed on top of the chip to redistribute slight pressure differences. Then the thermode is lowered onto the chip with a set pressure of 1-2.5 bar (depending on chip and bump size) and heated up gradually to the final bonding temperature of 200°C. At this temperature the ACF has a much lower viscosity, the applied pressure ensures electrical contact, and the excess adhesive flows out from under the chip. The gradual heating is needed to get optimal adhesion: if the thermode is heated up too fast, the ACF is cured too suddenly and inhomogeneously, resulting in bubble formation, and implying lower adhesion. After 30 seconds, the thermode heating is switched off so that the thermode cools down, while it still presses on the chip. This is to minimise residual stresses in the adhesive material of the ACF, so again to get optimal adhesion. When the thermode temperature has reached a temperature of 100°C, low enough so that the ACF has solidified sufficiently, the thermode is lifted up again. Thermocouple measurements result in the thermode temperature plot in Figure 4.9.[4]

[4] Attentive readers may have found that Figure 4.9 is the same as Figure 3.24. This is definitely true, because indeed the same profile was used.

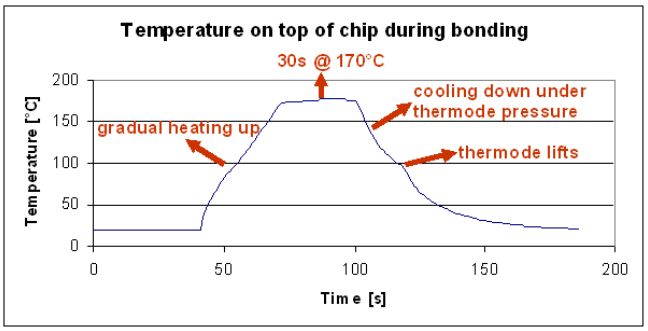

Figure 4.9: Temperature on top of chip throughout the actual bonding process

The bonding conditions had to be optimized for bonding on PET, as temperatures and pressures cannot be as high as when glass is used as substrate. To illustrate this, Figure 4.10 shows what happens when conditions used for bonding on glass are used on the PET supplied by PLL. The PET cannot withstand the high temperature and "melts" and the chip is pressed into the partially liquefied PET substrate. As no interposer is placed in between chip and thermode, the molten PET sticks to the thermode. Subsequently, when cooling down, the PET solidifies again and when the thermode retracts, it pulls plastic strings (clearly seen in the pictures) right out of the substrate.

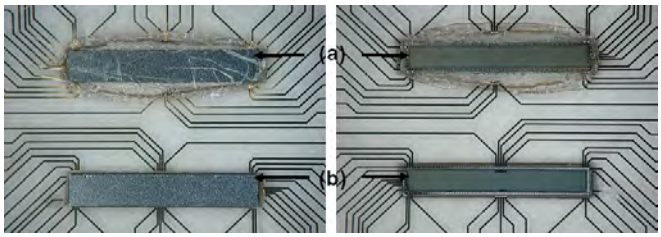

Figure 4.10: Comparison between bonding on glass and on PET, top and bottom view: (a) bonding carried out under "glass conditions", 30s @ 300°C, no interposer; (b) bonding with modified conditions, 30s @ 170°C, 0.2mm silicone interposer

4.2.1.3 Test Results

Firstly, feasibility to align bumped 50 μm pitch chips to a gold patterned PET substrate has been proven. This is illustrated in Figure 4.11. Secondly, no significant thermal expansion difference between substrate and chip was observed in any of the tests. This means no compensation has to be calculated in the substrate design beforehand (at least when the chips used remain smaller than 2.5 mm by 15 mm).

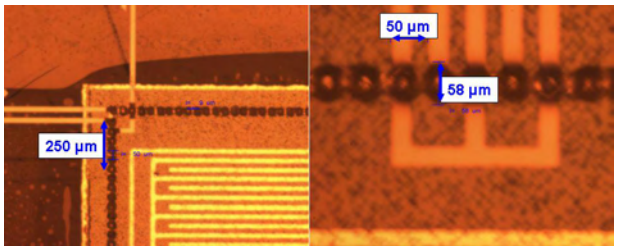

Figure 4.11: Pictures of a flip chip assembled test chip, proving the feasibility of aligning 50-µm-pitch chips to a patterned substrate; note the overplated contacts

Thirdly, it is important to level the thermode head accurately with the substrate. Uneven bonding easily results in a high variation of contact resistance, and worst case even loss of contact, along the length of the chip. To get an idea of what an uneven bonded chip looks like in bottom view (through the substrate), see Figure 4.12. Pressure was higher on the right side (in the figure) than on the left side. It can easily be recognised, as on the left no particles can be seen squeezed into the substrate whereas on the right there are. There is no electrical interconnection on the left side of the chip in the picture.

Figure 4.12: Pictures (left and right extremes) of an unevenly bonded test chip, 2.5 mm by 15 mm, 200 µm pitch

Fourthly, there is an important difference between bonding on glass and on PET concerning bonding pressure. Glass (and the metal pattern on it) cracks when using too much pressure, resulting in a sudden loss of interconnection, which can be translated into a maximum allowable bonding pressure. PET however, being a plastic, absorbs an excess of pressure energy by plastic deformation, instead of dissipating it along cracks in the case of glass and ceramics. There was some fear that this would result in a more gradual increase in (contact) resistance when more and more pressure is used for bonding, and the interconnection track on the substrate is bent more and more, until the line could be completely cut through by the side of the chip. On the other hand, a fear existed that if even more pressure was exerted, conductive particles clustered to the side of the chip would be squashed, possibly causing shorts between two or more neighbouring paths. Both fears are

explained schematically in Figure 4.13. However, no such things were observed in the conducted experiments, as far as this could be measured in the used setup, and with pressures up to 3.5 bar.

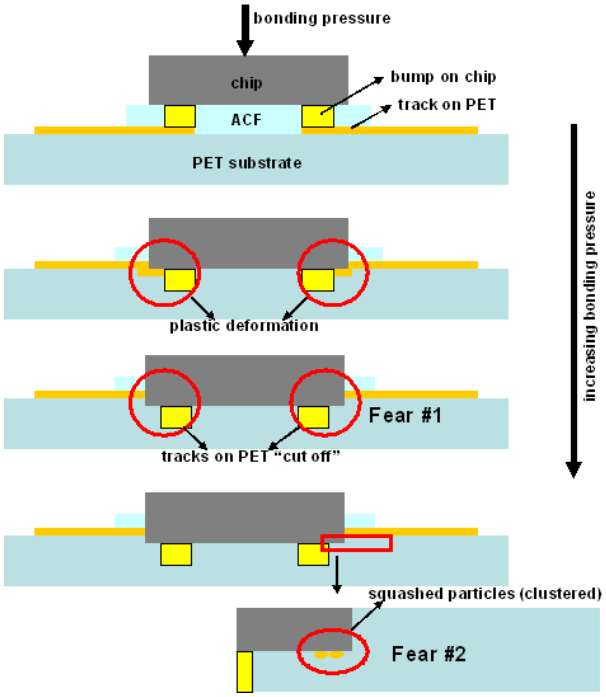

Figure 4.13: Schematic presenting fears that turned out to be wrong

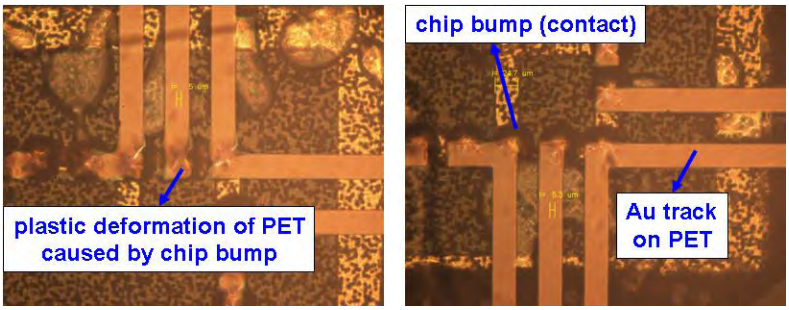

Figure 4.14: Pictures of a flip chip assembled 50-µm-pitch test chip: the contacts are pressed slightly into the substrate

Furthermore, the bumps are always pressed slightly into the substrate (causing

some plastic deformation) to ensure electrical contact between bump and substrate path. Figure 4.14 shows this effect under high magnification.

Electrical 4-point-measurements on the assembled 200 and 100 μm-pitch chips, given in Table 4.4, show contact resistances well below 1Ω. This resistance value can -currently- be neglected, when knowing that the used thin film gold interconnection lines on the substrate show resistances in the range of 0.5-1 $\Omega/\square$.

pitch [μm]	contact resistance [Ω]	# measurements
200	0.27 ± 0.23	82
100	0.27 ± 0.13	39

Table 4.4: Electrical 4-point measurements: results

The relatively high values in standard deviation, Table 4.4, can be attributed to (minor) misalignment: the contact resistance can vary significantly with the overlapping area of bump and contact on the substrate. The daisy chain measurements show that a contact yield of 100% could be achieved for 184 contacts at a pitch of 200 μm and 356 contacts at a pitch of 100 μm.

As for the mechanical adhesion, a significant indication that adhesion will be good enough is given in Figure 4.15. This shows that some adhesive still sticks to the substrate, while some held on to the chip. On the one hand some bumps were torn off the chip, on the other hand, some of the gold pattern was torn off the substrate.

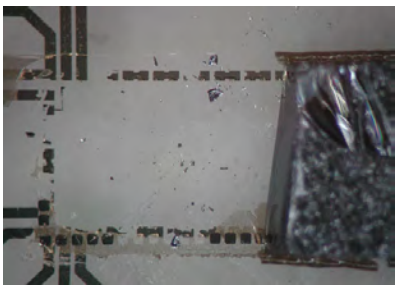

Figure 4.15: Chip broken off the substrate

The die shear strength for a standard bonded test chip, 2.5mm by 7.5mm, 200 μm pitch, was measured as 512.76N, using a Dage bondtester fitted with a DS100Kg cartridge. This corresponds to over 50 kgf, while a widely used standard for die shear strength, the US military MIL-STD-883 2019, only stipulates a die shear strength of over 5 kgf, if the die is larger than 64x10-4 IN2, equalling approximately 2mm by 2mm (most demanding requirement).

4.2.2 Tape Carrier Package Assembly

4.2.2.1 Setup

Another option to interconnect drivers to the display is to bond TCPs to the display. This is currently standard in flat panel displays (LCD, plasma and e-paper) manufacturing on glass substrates. Again this type of technology has to be modified for flexible substrates. One important thing to take into account is tape expansion during bonding: when the temperature rises, due to a different coefficient of thermal expansion (CTE) of flexible substrate and TCP material, the tape expands more, or less, than the display backpanel, as explained earlier in Section 2.4.3.5. This expansion was determined beforehand, at 57 μm for a length of 40mm, and compensated in the designs for the tests.

From a materials point-of-view, the tests were designed for PET display substrates, delivered by DuPont and patterned by Plastic Logic, and the tape material was provided by Shindo, a Japanese TCP manufacturer for ST Microelectronics. The tape material consists of a 75-μm base PI layer, with a 25-μm copper top layer, both held together by a 12-μm adhesive layer.

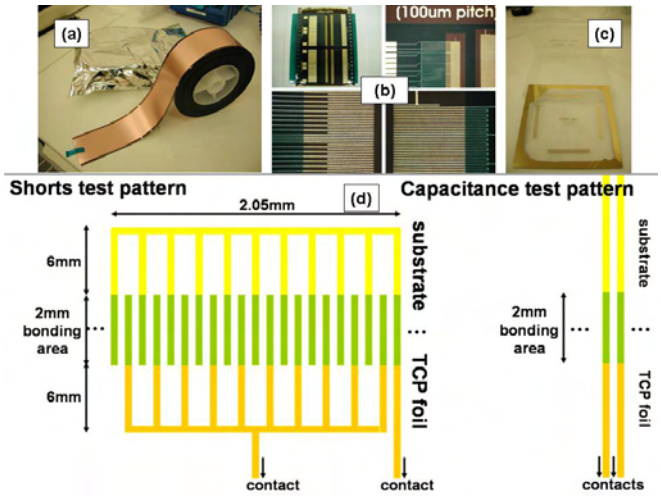

Figure 4.16: Tape material as delivered (a), after processing (b), patterned PET substrate (c) and design setup for shorts and capacitance testing (d)

Electrically, the tests are designed for daisy chain and capacitance measurements, and testing for shorts. The contacts are spaced at 100 μm pitch, patterning lower pitches was tried at 80 and 60 μm pitch, but proved too difficult to achieve with standard spray-etching techniques with an acceptable yield. To finish it off, 20-μm soldermask is applied and the contacts are electroless NiAu-plated. The

daisy chain pattern comprises 400 contacts. Figure 4.16 illustrates the setup designs and the patterned substrates, both tape and display PET.

4.2.2.2 Bonding Process

The bonding process itself is quite similar to the one described previously in Section 4.2.1: bonding was carried out with the same temperature profile and with a pressure of 2 bar, using the same semi-automatic bonder, but with a slim thermode head of 2mm by 70mm. However, aligning and placing was done manually, under a microscope, for the TCPs, and both ends are attached temporarily to the substrate with a soldering tool, before final bonding. As the PET substrates are attached to transparent glass carriers, backside illumination offers better viewing, as is illustrated in Figure 4.17.

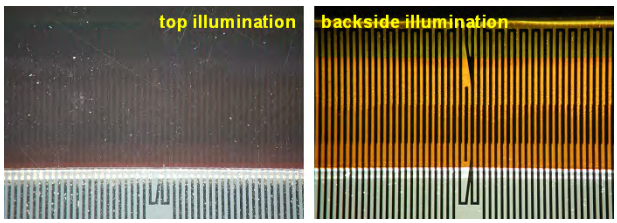

Figure 4.17: Aligning is much easier with backside illumination, mainly due to the thick PI

4.2.2.3 Test Results

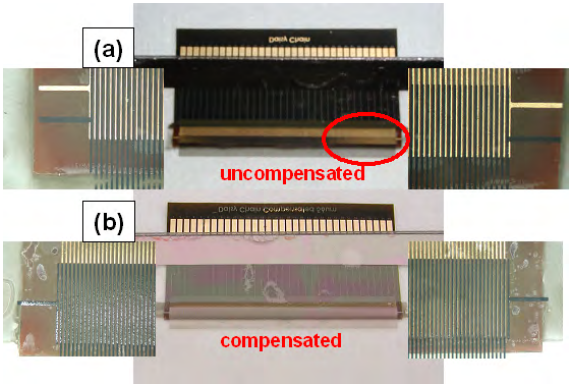

Figure 4.18: (a) Expansion leads to mismatch at the edges after bonding. (b) Compensation of expansion minimizes mismatch.

Optically, tape expansion, relative to the display substrate, was correctly compensated in the design. Also, it is possible -and rather convenient- to check optically whether or not electrical interconnection is established: this is the case when the particles are slightly squeezed into the display substrate's contacts. Both of these are illustrated in Figures 4.18 and 4.19.

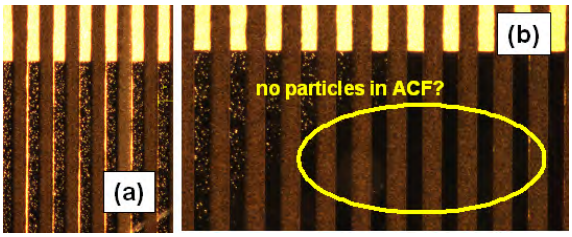

Figure 4.19: (a) ACF particles are pressed into the contacts, as seen through the substrate. (b) No electrical interconnection due to a lack of particles in the ACF (visible because no indentations are noticed)

Electrically, three types of measurements were carried out: daisy chains, shorts between neighbouring contacts, and capacitances, all listed in Table 4.5. The daisy chains show that the total resistance is primarily due to the resistance of the thin film gold on the substrates, so that contact resistance can be neglected. No shorts were found that were not present already before assembly, namely defects from prior processing steps. Capacitance between two neighbouring lines that are 8 mm long was 12 ± 1 pF. It should be mentioned that this is near the lower limit of the multimeter tool used, and 6 pF is the value measured when the probes are simply placed next to each other, 10 mm apart on the table.

Daisy chain measurements			
# contacts	# squares	line length [mm]	resistance [Ω]
12	880	48	571 ± 33
14	960	56	665 ± 38
16	1040	64	753 ± 39
Check for shorts			
0			
Capacitance measurements			
line length [mm]	C_{meas} [pF]	C_{offset} [pF]	C_{net} [pF]
8	12 ± 1	6	6 ± 1

Table 4.5: Electrical results for TCP on PET trials

Industrial requirements for data line resistance and capacitance for electrophoretic active-matrix displays are typically below 12 kΩ and 180 pF for 200 mm

long, 100 μm wide lines spaced at a pitch of 200 μm. With some recalculation, it is possible to extrapolate the measurements so that a comparison can be made. The results are shown in Table 4.6, where it is clear that the requirements are adequately met. Pictures can be found in Figure 4.20.

Extrapolation of measurements			**Requirements**
line length [mm]	line width [μm]	resistance [Ω]	
48 $\rightarrow$ 200 56 $\rightarrow$ 200 64 $\rightarrow$ 200	50 $\rightarrow$ 100 50 $\rightarrow$ 100 50 $\rightarrow$ 100	571 $\rightarrow$ 1190 665 $\rightarrow$ 1188 753 $\rightarrow$ 1177	$\leq$ 12 kΩ
line length [mm]	line width [μm]	capacitance [pF]	
8 $\rightarrow$ 200	50 $\rightarrow$ 100	6 $\rightarrow$ 150	$\leq$ 180 pF

Table 4.6: Extrapolation needed to compare measurements with requirements

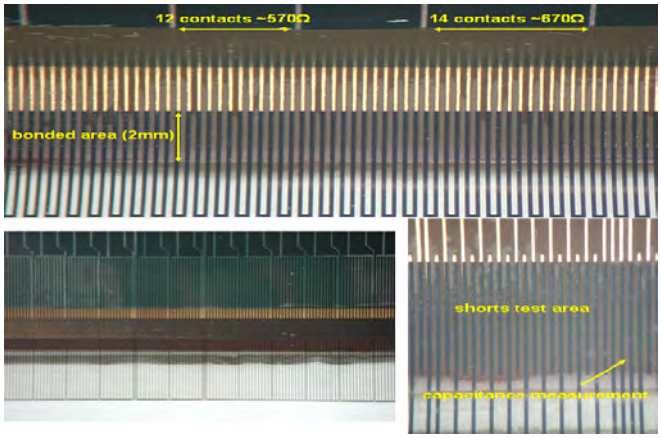

Figure 4.20: Assembled test TCPs (not on scale, widened): daisy chain (top) and shorts and capacitance (bottom) designs

One more remark concerns accuracy requirements: even major misalignment does not affect electrical interconnection significantly. A misalignment of 40 μm for example, shown in Figure 4.21, gives comparable measurements as a perfectly aligned assembly. Of course contact resistances can be expected to vary significantly, but this is not reflected in the measurements due to the much higher thin film resistance on the substrate.

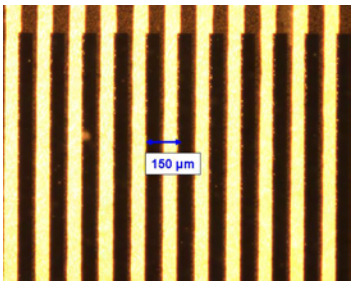

Figure 4.21: Despite misalignment electrical interconnection is still ensured through the ACF particles (indents still visible in the tiny overlap areas)

Mechanically speaking, adhesion can be measured by tweezer pull testing, also known as peel strength testing. The results indicate good adhesion, at least as far as the ACF is concerned. Measurements can be done perpendicular to the bond length or along the bond length, setups are as shown in Figure 4.22. The PET substrate is still attached to its rigid carrier when it is clamped in a holder that can be moved at a given speed while pulling.

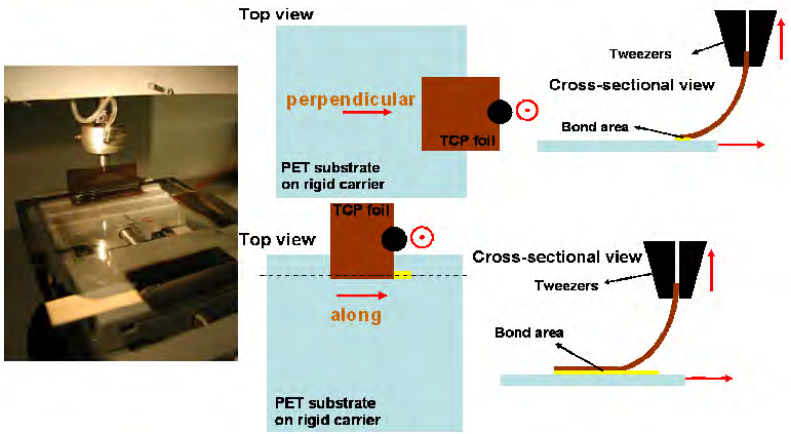

Figure 4.22: Setup for peel strength tests perpendicular (above) and along (below) the bond length; the movement of substrate and tweezer (pulling) is indicated by the red arrows

Perpendicular test results linger around 2000g / 40mm, and both substrate and TCP metallization are damaged in this type of peel test. Along the length of the bond however, this is rather 10-30g / 2.5mm. The results are slightly lower as compared to values reported in glass display interconnection of around 0.3 kN/m, but the top layer of the PET substrate tends to peel off (the failure is not due to

the ACF) and this interface thus becomes the limiting factor. This is shown in Figures 4.23 and 4.24 and the assembly, with this type of substrate and TCP, can be considered successful.

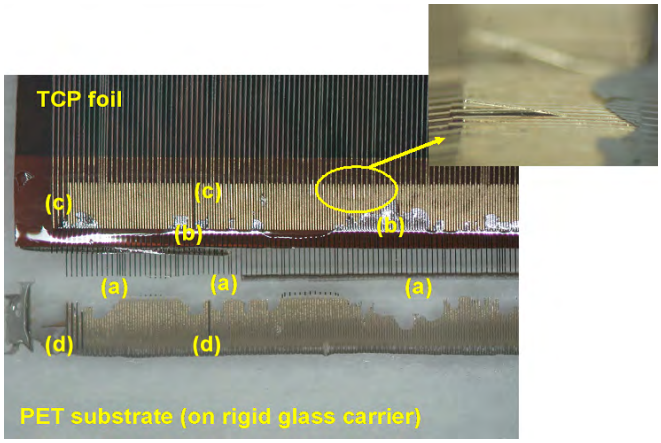

Figure 4.23: Resulting surfaces after peel strength testing perpendicular to the bond length: in some areas a layer (with gold metallization) is torn from the PET substrate (a), and still clings to the TCP foil (b), in other areas, copper traces are torn from the TCP foil (c) and still cling to the substrate (d); the zoomed view shows a copper trace that is partially torn off the TCP foil, while at the same time a layer of the PET substrate is still sticking to the TCP foil

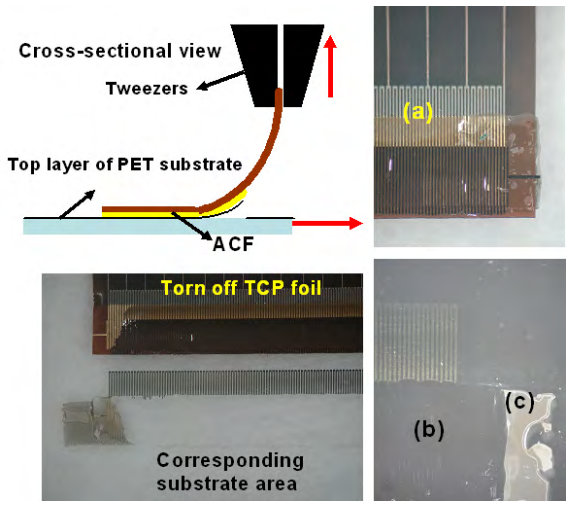

Figure 4.24: Results for peel strength tests along the bond length: the top layer of the PET substrate is torn loose and remains attached to the TCP foil (a), a void area is left behind on the PET substrate (b), with the exception of some adhesive leftovers at the sides (c)

4.2.3 Outlook

This section has shown how the existing industrial technologies in glass-based displays manufacturing can be adapted to fit the requirements introduced by switching to flexible PET substrates. The thus developed technology for bonding drivers, either packaged on tape or as bare die, to flexible display substrates, has been evaluated optically, electrically and mechanically.

These technologies are relevant and are currently being developed by ,Plastic Logic (UK), currently nearing the stage of a product application. A factory for manufacturing flexible displays on PET, on a commercial scale, has been built in Dresden, Germany, and has been officially opened September 2008.

4.3 oLED Display Assembly

References: [70], [71], [72], [73], [74], [75]

Another technology for flexible display manufacturing, also pursued within the FlexiDis project, is flexible OLED technology. Whereas Section 4.2 uses PET as flexible display substrates, with e-paper applications in mind, this section involves stainless steel substrates, which are more suitable for OLED displays, as OLED deposition processes require higher temperatures than what PET can withstand. As explained in Chapter 1, OLED is better suited than ePaper for videospeed and brightness[5] and can withstand higher temperatures.

For this technology as well, a collaboration was setup with CEA-LETI and Thomson, to develop the needed interconnection technology. In this case, it was decided, for reasons of available drivers and knowledge, to develop the technology for standard row and column drivers packaged as TCP.

4.3.1 Setup

In this section, functional TCP-packaged drivers from NEC (uPD160702ANL) and Hitachi (HD66358T03E), supplied by Thomson, are bonded to stainless steel substrates that were supplied and patterned by LETI. These are 152 μm thick and need to be polished before they are covered with a 1.5 μm thick SiO_2 insulator layer and a 350 nm thick TiMo metal pattern, matched to the TCP contacts. The polishing reduces the average roughness of the stainless steel from 95 nm to 0.6 nm, and is needed to minimize shorts from the metallization to the backpanel. It also improves the visibility of the metallization, as is illustrated by Figure 4.25. This difference in visibility caused a lot of struggling and frustration during the

[5] with OLED being an emissive technology whereas reflective ePaper displays are more dependent on lighting conditions as far as brightness is concerned

trials: illumination was needed from the sides for the rougher steel samples, and even then visibility under the microscope was sometimes problematic. This actually depended a lot on the direction of the bond patterns as compared to the direction of the steel substrate[6].

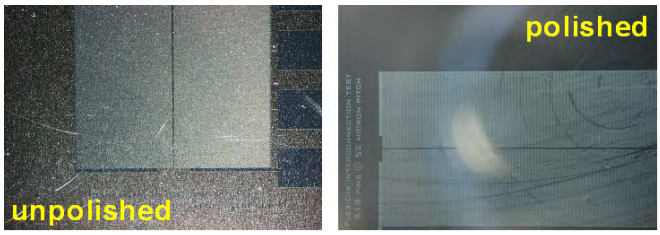

Figure 4.25: Comparison of polished and unpolished steel substrates

The specifications of the driverTCPs are given in Table 4.7, and it is also worth mentioning that the Hitachi TCP's contacts are shrunk by 40 μm to compensate for thermal expansion during bonding. This is not the case for the NEC TCP.

	pitch [μm]	# contacts	PI [μm]	adhesive [μm]	Cu [μm]
NEC	90	267	38	none	8 (Sn-plated)
Hitachi	52	519	75	12	15 (Sn-plated)

Table 4.7: Specifications of driverTCPs used

As the tests are carried out with actual TCPs, design options for electrical testing are limited: the substrates are patterned with incomplete daisy chains that can only be completed by a correctly bonded TCP. The setup is given schematically in Figure 4.26.

[6]there is an anisotropical roughness introduced in the fabrication process of the steel substrates, most likely due to roll-to-roll processing

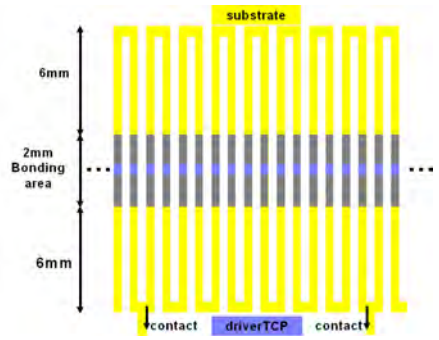

Figure 4.26: Setup for electrical interconnection testing of bonds with existing TCPs

4.3.2 Bonding Process

The bonding process is again quite similar to the previous examples in Section 4.2, although there are a few important differences. First of all, steel is not transparent and this means backside illumination is not an option. Next, the contacts that need to be interconnected have a finer pitch, down to 52 μm for the Hitachi driver. These differences mean that placing and aligning are far more difficult, although not impossible. Then there is also the fact that the contacts have lower bumps, so the bonding pressure is raised from 2 to 2.7 bar to squeeze out more adhesive. Finally, it should be mentioned that heat dissipation is rather different, as steel conducts heat far better than PET. However, the temperature of the bonding head (thermode) does not need to be raised if an insulating glass plate is placed between the substrate and the (metallic) substrate table.

4.3.3 Test Results

Optical and electrical results are summarized in Table 4.8. The thermal expansion is sufficiently within range using the current bonding parameters, so that all TCP outputs can be electrically interconnected to the substrate. The measured resistances are, as earlier on with the other options on PET, mostly due to the thin film resistance of the metallization on the substrates, and are supposedly sufficiently low for current active-matrix OLED displays.

	NEC TCP	Hitachi TCP
# samples bonded	7	11
misalignment before bonding [μm]	-0.5 $\pm$ 2.0	-0.7 $\pm$ 2.6
misalignment after bonding [μm]	16.6 $\pm$ 4.6	3.1 $\pm$ 4.5
expansion measured [μm]	34 $\pm$ 12	46 $\pm$ 9
# daisy chains measured	45 (out of 49)	53 (out of 77)
# contacts / daisy chain	76 (38 x 2)	148 (74 x 2)
# squares on substrate	7600	25615
line length [mm]	532	1036
resistance [Ω]	3020 $\pm$ 135	12049 $\pm$ 1942

Table 4.8: Results and measurements on assembled daisy chains

Please note that not all daisy chain patterns of the bonded samples have been included in the measurements. This is because of mistakes that were made in the bonding process and the steps preceding this, such as (slight) misalignment, the thermode that is not sufficiently aligned to the substrate (resulting in uneven pressure during bonding), insufficient cleaning, as well as problems due to the steel backpanel (bypassing several daisy chain patterns and thus disrupting electrical measurements), and shorts between neighbouring contacts due to defects introduced during patterning (mask faults, dust contamination, ...).

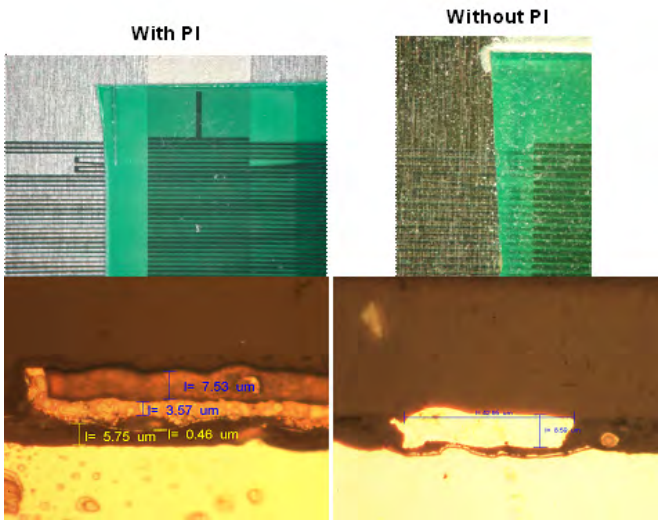

Figure 4.27: A PI insulating layer vs an SiO_2 insulating layer for steel substrates

One issue requiring special attention involves the mentioned problems with the steel backpanel. The 1.5 μm SiO_2 insulating layer suffers from pinholes due to the

surface roughness of the steel substrates, even after polishing. One solution would be to use a thicker (e.g. 5 μm) organic PI layer, that would double-act as a spun-on planarizing layer. This would also significantly enhance viewing the metallization. This is illustrated in Figure 4.27.

Mechanically, adhesion was tested with the same setups as described in Figure 4.22, whereby the tests resulted in the damage shown in Figure 4.28 for the Hitachi TCP and Figure 4.29 for the NEC TCP. For the Hitachi TCP, the peel strength was measured as 1400g / 40mm perpendicular to the bond length, and 150g / 2.5mm along the bond length. It is clear that some tracks on the TCP have been torn off the TCP substrate, illustrating that adhesion between the metal tracks (Ti/Mo on substrate and Cu/Sn on TCP) is comparable to the adhesion between the copper and PI layer in the TCP buildup. As for the NEC TCP, the peel strength was measured as over 2500g / 40mm (out of the set range of the bond tester) perpendicular to the bond length, and 150g / 2.5mm along the bond length. Here, the pictures show a different result: it is the ACF that is torn. The reason for the difference was not thoroughly investigated, but it may be explained by the difference in package type for the Hitachi and the NEC driver. On the one hand, the Hitachi driver is packaged on a so-called 3-layer flex. This means the metal layer, often a copper foil is attached to the foil with an adhesive, as specified in Table 4.7. In the same table, it is specified that the NEC driverpackage is based on a 2-layer flex, without adhesive layer. Depending on this type of so-called copper clad laminate, adhesive or non-adhesive, the peel strength can be different: reported peel strength values for 2-layer flex foils are typically around (higher than) 1.5 N/mm, whereas for 3-layer flex foils this is somewhat lower, around (lower than) 1.2 N/mm. This is in accordance with the observations made above that, using the same ACF, the peel strength for the bonded Hitachi TCP is slightly lower than for the bonded NEC TCP. Also, for a similar Hitachi ACF, AC-7250U-16 developed for FPC (Flexible Printed Circuit) bonding, peel strength is specified as 1.35 N/mm in standard bonding conditions, with a bonding temperature of 180°C, which is right in between the above peel strength values for 2-layer and 3-layer flex foils. This means, theoretically at least, that indeed in 2-layer flex foils the ACF will fail before the metal, whereas for the 3-layer flex, the metal will start peeling off before the ACF fails. Finally, what might also make a difference is that the metal contacts on the Hitachi TCP are thicker than for the NEC TCP: 15 μm as compared to 8 μm, referring to the figures in Table 4.7. This means the contact area between ACF and metal track is relatively bigger for the Hitachi TCP than for the NEC TCP, implying that the ACF has more "grip" on the Hitachi contacts, if only the contact area is considered, and not the fact that different kinds of materials imply different adhesion strength. The theoretical calculation is made in Table 4.9.

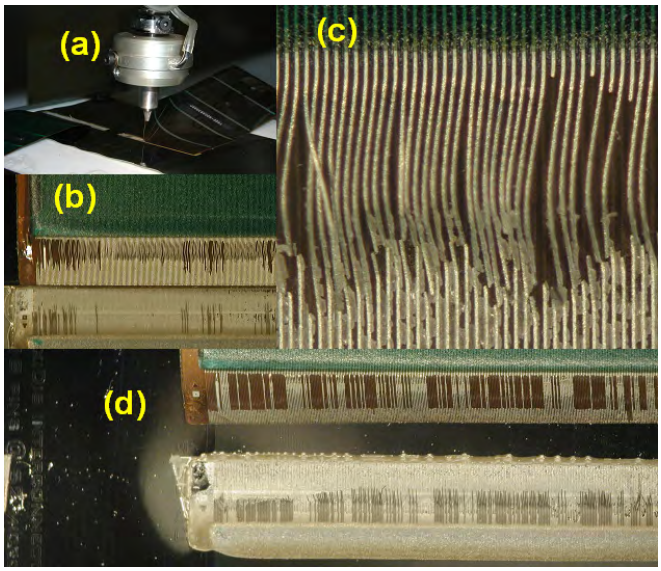

Figure 4.28: Peel strength tests on a bonded Hitachi TCP: (a) peel setup, (b) result of peeling along the bond length, (c) zoomed view and (d) result of peeling perpendicular to the bond length

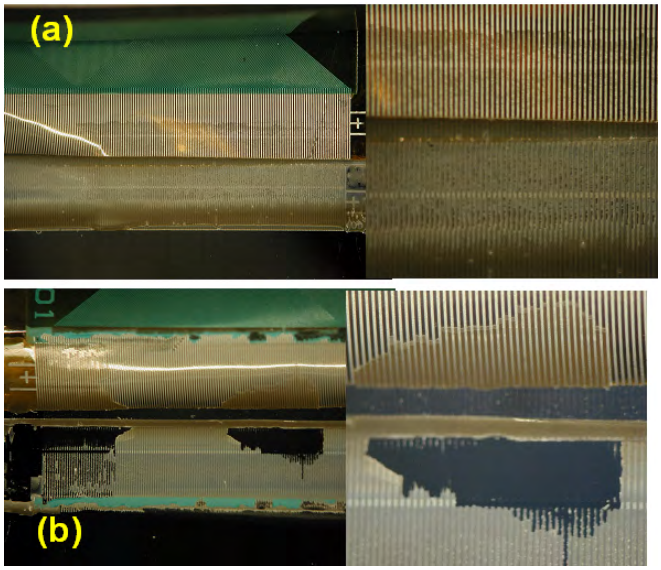

Figure 4.29: Peel strength tests on a bonded NEC TCP: (a) result of peeling along the bond length, (b) result of peeling perpendicular to the bond length

	Hitachi	NEC
Pitch [μm]	90	52
ACF/Metal interface per pitch [μm]	25 + 2x15 = 55	45 + 2x8 = 61
ACF/PI interface per pitch [μm]	27	45
ACF/Metal contact interface [%]	67	58

Table 4.9: Contact interface between ACF and metal tracks for the different TCPs

4.3.4 Outlook

This section has described how an existing industrial technology for glass-based displays manufacturing has been modified to fit the requirements introduced by switching to flexible stainless steel substrates. The technology for bonding drivers packaged as TCP has been evaluated optically, electrically and mechanically.

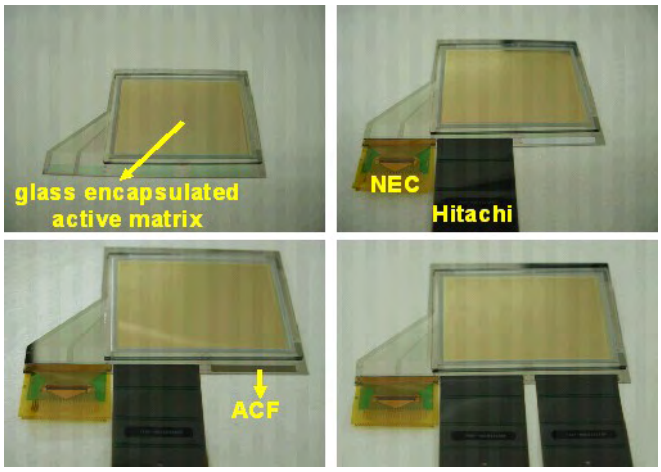

Figure 4.30: Assembly of a flexible display on a stainless steel substrate with row (NEC) and column (Hitachi) drivers packaged as TCP

For this technology, stainless steel substrates with flexible OLED displays are being prototyped and considered for, amongst others, integration in the sleeves of a jacket. Demonstrator prototypes have been assembled using the developed technology, as illustrated in Figure 4.30.

4.4 PDLC Display Assembly

References: [76], [77], [78], [79], [80]

As an extension of the work carried out within the thesis of Thomas Vervust, integrating a rigid glass display into flexible and stretchable electronic circuitry, as described in Section 3.2, the possibilities were investigated to develop a flexible display, thus potentially increasing the flexibility and robustness of the demonstrator, while at the same time decreasing its thickness and weight. This research and development work was done within the framework of another master thesis by Jeroen Goossens, "Integration of a flexible display in a stretchable wristwatch", and its underlying reasons were threefold:

- it remains very difficult to obtain existing flexible displays and/or key materials in small amounts, although many commercial products are already widely advertised and you can probably get them easily if you order them by the hundreds of thousands, for mass-production,

- to generate the knowledge and experience for flexible display assembly inhouse might greatly benefit other research within the group and/or open up new opportunities,

- already some experience was available within the group for the assembly of one type of (rigid) displays, that might be, relatively easily, adapted for manufacturing flexible displays.

4.4.1 Display Technology

In this master thesis Polymer Dispersed Liquid Crystal (PDLC) was chosen as the display technology to produce a flexible display. The goal was to make a reflective display, basically consisting of two flexible substrates with in between the PDLC material, a mixture of liquid crystal droplets in a polymer matrix. When no voltage is applied to a pixel, the PDLC has a white color. When a sufficient voltage is applied, the PDLC becomes transmissive and a black or metallic background becomes visible. The working principle is shown and illustrated in Figure 4.31[7]. No polarizers are required for the PDLC technology.

[7] alignment to the applied electric field etc., see Section 1.2.3

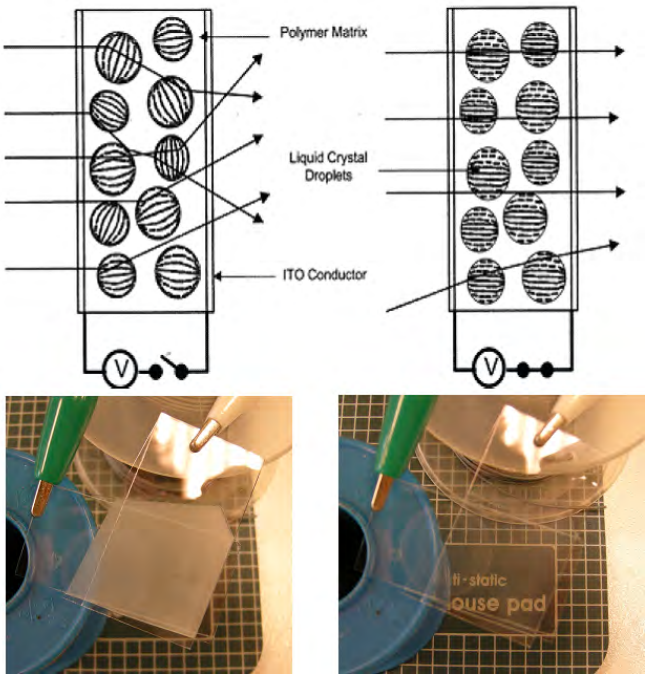

Figure 4.31: Working principle of PDLC displays: the liquid crystal is dispersed under the form of spheres in a polymer matrix, and is driven similarly as in a standard liquid crystal display

Being intended for portable applications, namely a wristwatch, the objective was to keep the necessary drive voltage as low as possible. Previous research in the framework of a doctoral thesis, "Introduction of color in reflective PDLC and PNLC microdisplays" by Filip Bruyneel, teaches that it is best to use a mixture of 20 wt% prepolymer and 80 wt% liquid crystal. This way the screen has sufficient optical properties and a relatively low drive voltage, although these properties of course still highly depend on the cell gap as well, as explained further on. The liquid crystal and prepolymer used are respectively TL213 and PN393, both produced by Merck and recommended by them for producing low-voltage displays.

The used flexible substrates consist of polyethersulphone (PES), coated with ITO as transparent conductor, with a thickness of respectively 150 μm and 115 nm. Another important factor is the cell gap, which is defined as the distance between the substrates, and is controlled by spacers. These are usually spherical or cylindrical particles, mostly of polymer or ceramic material, with well-defined dimensions that are placed between the substrates to keep them separated. A trade-off has to be made in the dimension of the spacers: bigger spacers imply a larger cell gap, and results in increased reflectance values on the positive side, but also higher driving

voltages on the negative side. Tests were carried out with different sizes, with 5.2, 10 and 40 μm spacers, and an optimum was found in 10 μm spacers: these result in a significantly better uniformity of the observed whiteness compared to 5.2 μm, as shown in Figure 4.32, and have an acceptable driving voltage in the range of tens of Volts. Also, the waviness and plasticity of the used plastic substrates too easily cause shorts between top and bottom substrate when the smaller spacers are used, and the larger spacers prove to be difficult to deposit uniformly onto the display substrate: they are relatively heavy so that they are too easily catapulted off the substrate during spincoating.

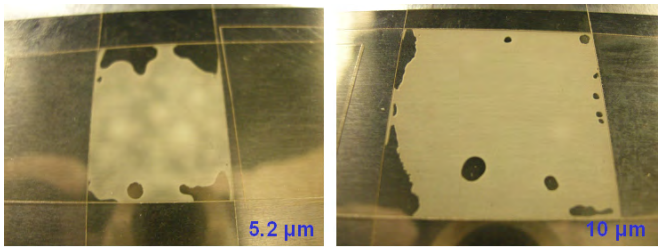

Figure 4.32: The uniformity of the PDLC is influenced by the size of the spacers, specifically when flexible substrates are used

4.4.2 Fabrication

For the application in mind, a wristwatch, first the ITO coating of bottom and top PES substrates must be patterned. This is done with standard lithography techniques and etching with a buffered HF-solution. The designed pattern results in 4 digits with 7 segments each, and the overlap between top and bottom patterns is restricted to the segment areas, carefully making sure that any interconnection tracks on top and bottom do not overlap each other. The top substrate will act as common electrode for the PDLC, so all segments on that side are connected to each other. One crossover contact ensures interconnection from this top electrode to an outside contact on the bottom substrate. Eventually, all of the display's outside contacts[8] are rerouted on the bottom substrate towards a row of contacts, each 0.5 mm wide, and spaced at a pitch of 1 mm. The design and some resulting substrates are shown in Figure 4.33.

[8] 29 contacts: 4x7 segments and 1 double-point symbol

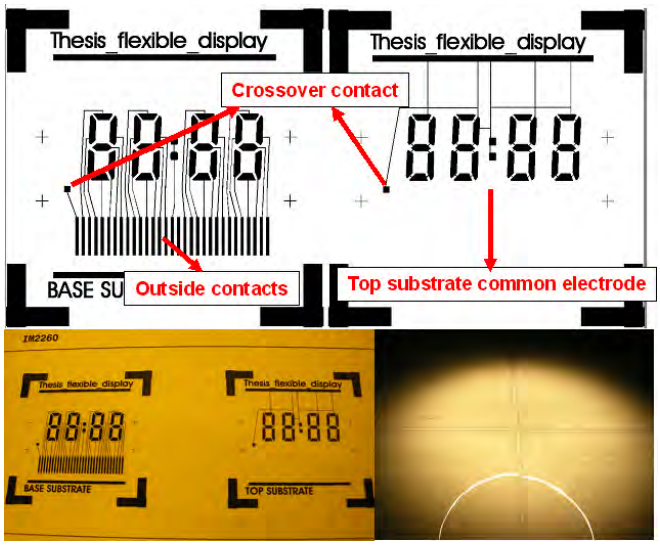

Figure 4.33: Design of the final PDLC display demonstrator (top), as well as the corresponding mask set (on foil, below left) and some patterned substrates (difficult-to-see transparent ITO patterns on PES substrates, still attached to the carrier, below right)

From a practical point-of-view, the PES substrates are attached to a rigid ceramic carrier for lithography and etching, using double-sided adhesive. A few important remarks should be made regarding processing steps at this stage:

- The substrates should be dried out completely prior to spinning on photoresist for patterning. Without this drying, approximately 2 hours at 120°C, bubble formation was observed during illumination, as illustrated in Figure 4.34.

- ITO is, unfortunately, a rather brittle material, which means that it easily cracks at low strains. Particular care should be taken when the substrate is removed from the carrier. It was found that the best way to do this is to release the substrate by carefully sliding a pair of tweezers underneath the substrate, while the carrier is heated by a hotplate at 120°C. The phenomenon of ITO cracking is shown in Figure 4.35.

Figure 4.34: The influence of drying out the PES substrates before processing: without (left), bubbles are observed after illuminating the photoresist, resulting in bite-like marks and cracks after developing

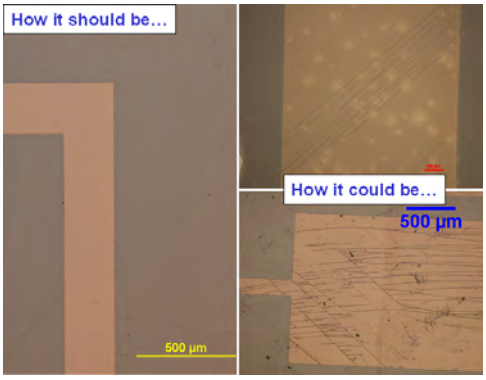

Figure 4.35: ITO is a very brittle material: cracks are easily introduced during release of the substrates (pictures on the right)

The patterned substrates can subsequently be used to assemble the displays. The spacers, dissolved in a methanol-solution, are spincoated onto the ITO side of the top substrate, which is then clamped by a mask in the mask aligner, that has been adapted to act as a vacuum chuck. The bottom substrate is placed on the aligner's substrate table and aligned to the top substrate. First, a tiny amount of conductive adhesive, a 2-component silver filled epoxy, EPO-TEK EE129-4, is applied carefully with a needle to provide the crossover. This epoxy however damages the PDLC's polymer component, so the PDLC has to be shielded from it. This is done by applying an arc of non-conductive adhesive around the crossover dot. This adhesive is Norland's optical adhesive NOA68, standardly used for sealing the edges of liquid crystal displays. Finally, a drop of the uncured PDLC-mixture is then deposited on the bottom substrate and bottom and top substrate are brought into soft contact positions. At this point, the PDLC should be flowing out towards the edges of the display. In this case, the display has an approximate area of 30 mm by 20 mm, so a rough estimation teaches that the applied drop should be around

30mm x 20mm x 10μm = 6μl. A microsyringe allows for sufficiently accurate drop volumes.

Illumination is carried out under a UV-lightsource, in this case a Hg-lamp with an intensity of 12.5 $\frac{mW}{cm^2}$, for 180 seconds. This is not a very crucial step, as it was found in previous research that "A wide range in UV curing parameters has only a small influence on the electro-optical properties. This suggests that the PDLC material of Merck is rather robust concerning UV curing parameters"[9]. Finally, the display is sealed with the aforementioned NOA68 from Norland, cured 400 seconds at an intensity of 10.5 $\frac{mW}{cm^2}$. Pictures of the display assembly process are shown in Figures 4.36, 4.37 and 4.38.

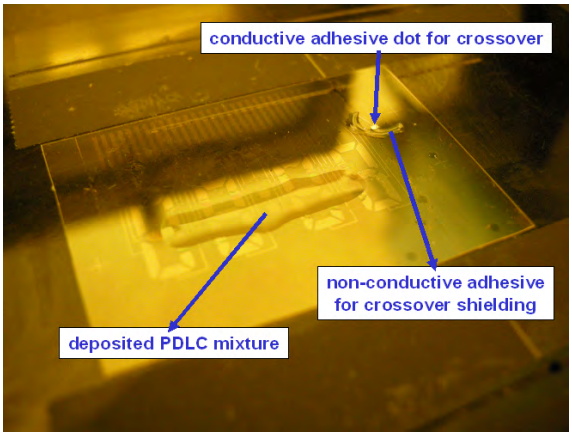

Figure 4.36: The PDLC mixture is deposited onto the bottom substrate after applying the crossover dot and an arc of shielding non-conductive adhesive

[9] from Filip Bruyneel's doctoral thesis

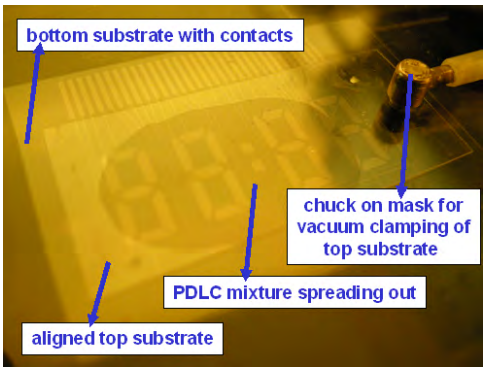

Figure 4.37: The top substrate is aligned and brought into soft contact with the bottom substrate; the drop of PDLC spreads out across the cell gap defined by the spacers

Figure 4.38: Once settled, the assembly is illuminated: after 5-10 seconds, polymerisation is visible as the PDLC turns opaque

A few observations that are worth mentioning:

- The PDLC mixture is preferably prepared just prior to deposition and has to be stirred quite thoroughly, so that it looks homogeneously transparent. No separate opaque phase should be distinguishable in the mixture, as otherwise, the display uniformity will be visibly affected, as illustrated in Figure 4.39.
- Sealing the display is necessary: apart from its usual purpose, which is protecting the PDLC from degrading outside influences, it also provides some mechanical support, which is important, considering the flexibility of the substrates.
- The resistance introduced by the crossover is negligible compared to the resistance posed by the ITO conductive tracks.
- A few experiments were done for laser-sealing the displays, similar to what has been reported by Kent Electronics, but the same techniques proved to be unsuccessful. The main reason is most probably that the used PES substrates are significantly more heat-resistant than the PET used by Kent Electronics:

the PET melts and is welded together, but the PES seems to burn rather than melt.

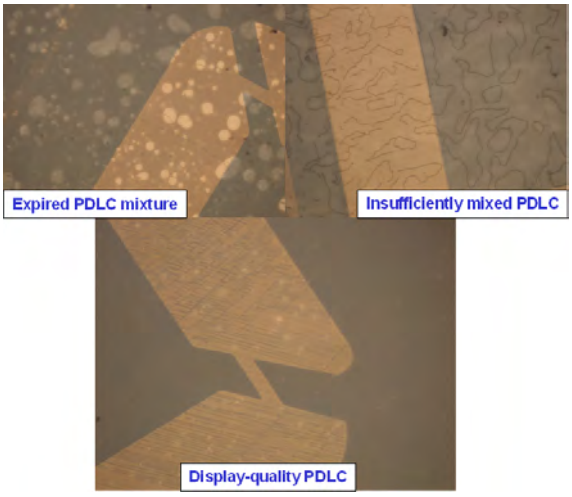

Figure 4.39: Problems encountered with the PDLC mixture

4.4.3 Characterization

The display technology has been characterized, both electrically and optically. First, this was done with a setup for measuring transmissively, as shown in Figure 4.40, together with one of the results. Also, degradation was observed and measured numerically with non-sealed displays.

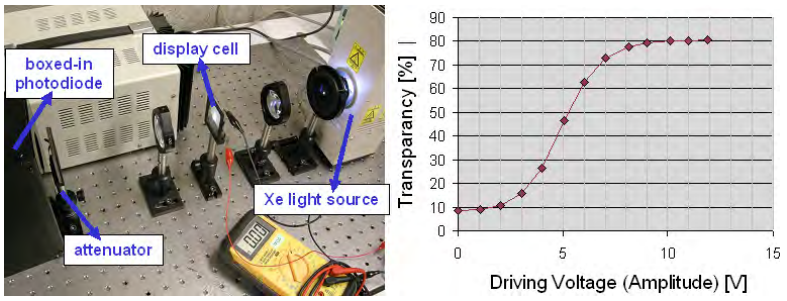

Figure 4.40: The setup for initial characterization: the photodiode is boxed-in to shield it from ambient light (preferably the measurement is carried out when the room is obscured), the incoming light spot is controlled in size by the diaphragm in front of the light source, and the attenuator (4 25-nm TiW sputtered glass substrates) is required because the used avalanche photodetector is very sensitive and would otherwise be saturated

Later on, the setup was modified for measuring the luminance of the display in reflection, depending on the driving voltage and the angle of reflection, varied between 30°, 45° and 70°. The reflection was created by attaching a piece of Al foil to the backside of the display cell. Luminance and contrast measurements were done with bundled incoming light, as well as under diffuse lighting conditions. The setup and principles are shown in Figure 4.41.

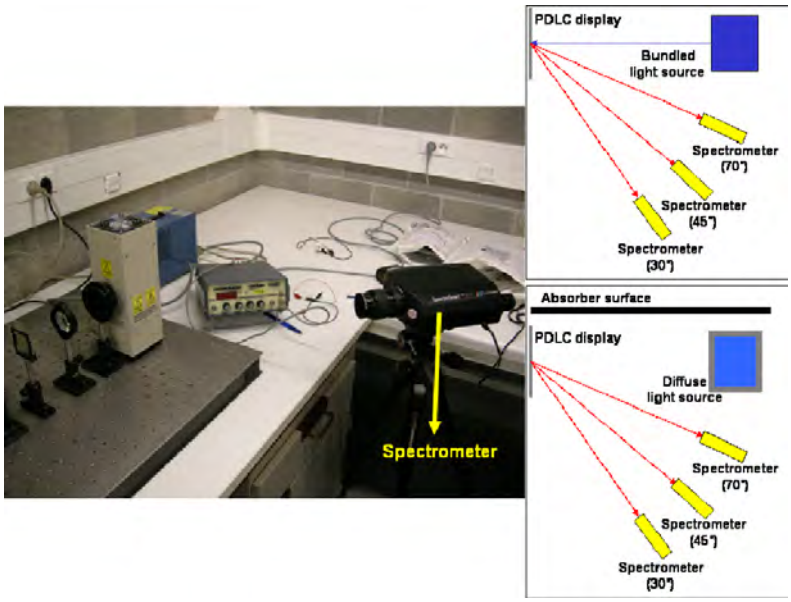

Figure 4.41: The setup for measurements in reflection, which better reflects the actual viewing experience for a user (considering the wristwatch-application in mind)

4.4.4 Interconnection

Prior to interconnecting the functional displays to any driving electronic circuitry, the interconnection technology, consisting of bonding with ACF, was tested. Corresponding daisy chain patterns were designed and fabricated on PI/Cu substrates for the electronics side and on PES/ITO substrates for the display side. Bonding was successful with the Farco bonder[10], with a pressure of 2.5 bar, with a silicone interposer and a gradually built up temperature of 200°C for 30 seconds. Tests were done for different pitches, 2000, 1000, 750, 500 and 200 μm, as shown in Figure 4.42. The electrical measurements are summarized in Table 4.10.

[10] see Section 2.4.3.4

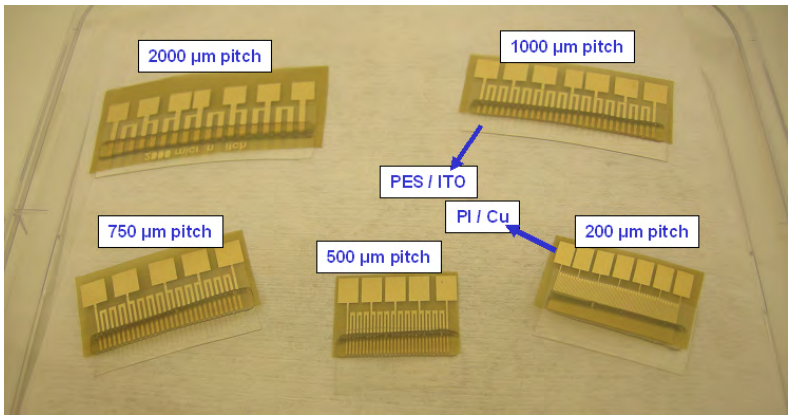

Figure 4.42: Bonded test patterns for electrical measurements

pitch [μm]	measured [Ω]	# contacts	# ITO squares	# Cu squares	verification [Ω]
2000	5750	18	117	121	5850
1000	12930 $\pm$ 679	30	255	263	12751
750	13605 $\pm$ 573	30	314	324	15701
500	20490 $\pm$ 1428	30	443	459	22151

Table 4.10: Results and measurements on assembled daisy chain patterns

The column "verification" in Table 4.10 shows the theoretical values obtained by multiplying the number of ITO squares by the approximative value for the ITO resistance, in this case 50 $\Omega/\square$ for the 115 nm thick ITO coating, and added to that the resistance calculated by multiplying the number of Cu squares with its resistance, approximately 3 m$\Omega/\square$. It is directly obvious that the Cu resistance is overwhelmed by the ITO resistance. Differences between measured and theoretically calculated resistances can be attributed to slight misalignment and variations in ITO resistivity: the uniformity of thin film layers such as this ITO has a significant influence in the track's resistivity. Another remark concerns the omission of the 200 μm pitch patterns: as they were badly aligned, the electrical measurements are not included. The bad alignment is not due to a fundamental problem, but rather a practical one, namely that it was done too fast and without enough care. Sufficient alignment can be achieved and has been proven feasible down to pitches of 100 μm, further on in Section 6.6, for the same type of interconnection.

Based on these bonding tests, and practical considerations concerning dimensions, it was decided to design the 29 contacts with a width of 0.5 mm and a pitch of 1 mm for the display demonstrator. This bonding process was implemented for

the display demonstrators and proved to provide a good interconnection between display and electronics, as elaborated in the next Section.

4.4.5 Integration

To have a functional demonstrator, in this case a (wrist)watch, of course some electronic circuitry is needed. The same line-of-thought can be used as in Section 3.2, with the integration of the rigid display, with the notable difference that the driving voltage for the display is significantly higher. This means other components are needed. Again a breadboard prototype was developed, first to test the concept with a standard LCD display, after which the same driving electronics could be used for the flexible PDLC display. The first circuitry on breadboard for testing the driving electronics is shown in Figure 4.43.

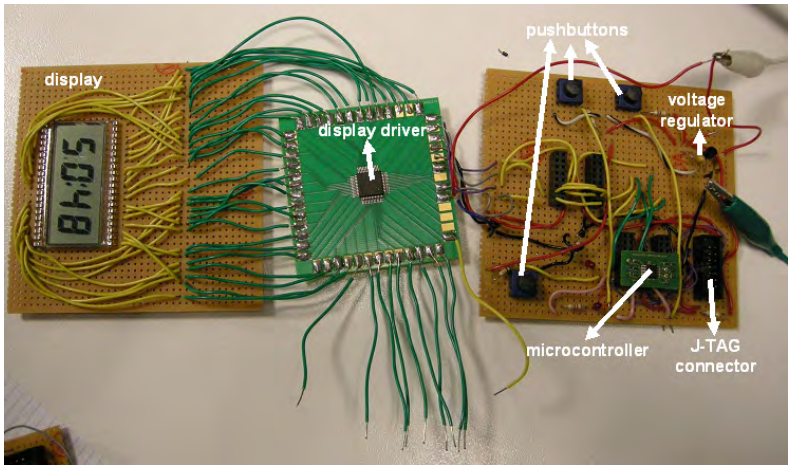

Figure 4.43: A testing prototype for the driving electronics: the standard LCD display is driven with the higher voltages needed for the PDLC display

A second, more advanced version of the electronics were made, by integrating the electronics on PCB. The display is bonded to an interposer flex, on which a connector is mounted. The connector is mounted on the PI/Cu flexfoil through soldering, BEFORE it is bonded to the display, as the display cannot withstand the high temperatures during reflow soldering. The same connector is also integrated on the electronics PCB, so that the connection between electronics and display can be made by a pluggable cable. The result is visible in Figure 4.44.

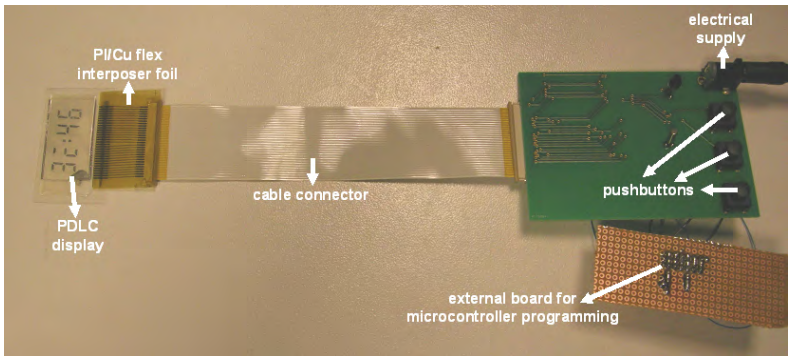

Figure 4.44: The final demonstrator of the thesis showing the PDLC display and its connected driving electronics on PCB; external power is supplied by a 12V-adapter; the pushbutton and crystal are assembled on the visible side of the PCB, the other components are mounted on the other side

4.4.6 Optimizations

This thesis had a lot of aspects, and each one of them can (and needs to) be optimized, if it is to be exploited commercially.

Figure 4.45: Illustrating the influence of the background on display performance: Al is a better mirror than TiW, but sputtering results in curling of the substrates

Firstly, a reflective or absorbing backside has to be integrated into the display assembly process. A number of possibilities exist, and a few trials have been car-

ried out. Directly sputtering a reflective metal on the backside of the PES seemed to be the most obvious solution, and both TiW and Al were tried, but this resulted in curling of the substrate[11]. Another option could be to attach aluminum foil, optical grade, or a thin PI film with sputtered Al, to the backside afterwards. The first option is illustrated in Figure 4.45, the latter two were not investigated.

Other optimizations relate to the portability of a possible commercial product. E.g., an external power supply is not suitable for portable applications, so the driving electronics should be reviewed for less power consumption, preferably adapting the PDLC display for lower driving voltages (possibly by decreasing the cell gap). Also, the PCB should be replaced with a flexible version, and embedded in e.g. silicone, in the same way as in Section 3.2. Some first promising trials were done to embed the PDLC display in silicone, as shown in Figure 4.46.

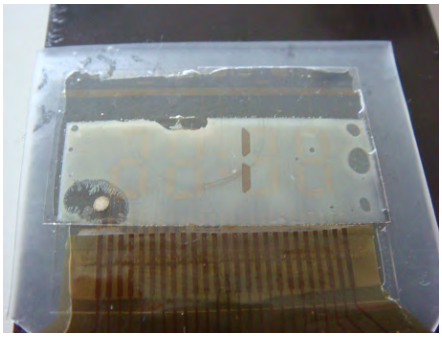

Figure 4.46: Embedding the display in silicone could be used for protecting it from degrading influences such as moisture and increasing its mechanical ruggedness, e.g. by applying a thicker silicone layer in the display area, redirecting all stresses towards the thinner silicone areas outside the display area

Here, I tried to give a comprehensive summary. For more information, I would like to refer to the thesis itself, although only available in Dutch. While a fully integrated watch, as stated in the thesis' title, "Integration of a flexible display in a stretchable wristwatch", was not finalized, the obtained resulting technology, knowhow and experience for manufacturing flexible displays can be considered an achievement in its own right. Combined with the flexible and stretchable technologies available in the research lab, amongst others the interconnection technology developed in the preceding thesis, as described in Section 3.2, display development can be further advanced towards flexibility, portability and ruggedness.

[11] although this might possibly be solved as described in [80]

5

Flexible Assembly: Issues and Solutions

"All things are difficult before they are easy."

— Dr. Thomas Fuller (1654 - 1734)

In general, flexible substrates are often an interesting alternative for rigid ones because they are light and conformable. This is especially an advantage when integrating electronic devices for wearable applications. A light and flexible substrate by itself however does not guarantee a light and flexible end result. The flexibility is often drastically reduced when rigid components are assembled onto the substrate.

Where flexible displays are concerned, their flexibility is usually hampered by the driving electronics. This is an increasing concern, considering the fact that several flexible display technologies are sprouting up and slowly but deliberately finding their way towards commercial applications. In this chapter, the encountered flexibility issues are first elaborated, after which some of the more obvious solutions are proposed and discussed. At this point, it is made clear that flexible displays, and flexible electronics in general, are not only interesting because of their flexibility, but at present they are rather being developed for their light-weight and robustness. This paves the way for introducing embedding technologies. Finally, a promising new chip embedding technology is introduced that may lead towards significantly lighter, more flexible and more robust display products.

5.1 Tackling Issues in Flexible Display Assembly

References: [81], [82], [83]

Now that flexible displays start emerging from the research and development stage to the application design stage, it is found that the driving electronics, together with the interconnection between display and driving electronics are becoming limiting factors in the flexibility of the display modules. Earlier on, delamination of the display substrates during flexing was a major difficulty, but this is slowly being conquered. Three main issues are easily identified, and illustrated in Figure 5.1.

- The flexibility is restricted by the external rigid driving electronics.
- Reliability problems occur due to flexing of the TCP interconnection area.
- Rigid Si chips mounted on the display substrate crack when flexing the display.

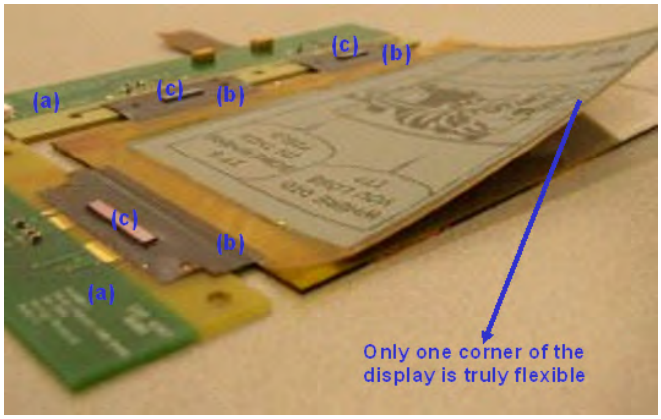

Figure 5.1: Flexibility issues in flexible display modules: (a) external driving electronics on rigid PCB, (b) TCP attachment and (c) rigid Si driverchips

5.1.1 Flexible Driving Electronics

The restriction on the flexibility posed by the external driving electronics could be partially undone by replacing the rigid PCB by a flexible one. As said at the beginning of this chapter, however, rigid assembled components reduce the flexibility of the substrate. Within the framework of FlexiDis, a flexible PCB, based on commercially used driving circuitry[1], was designed and fabricated to illustrate

[1] namely the electronics incorporated in the Iliad reader (an eBook reader)

the achievable possibilities: consisting of 4 routing layers, the components are grouped in 6 areas, so that 3 flexing axes remain free of rigid obstacles. The design, which was done in close collaboration with IRex Technologies, is shown in Figure 5.2.

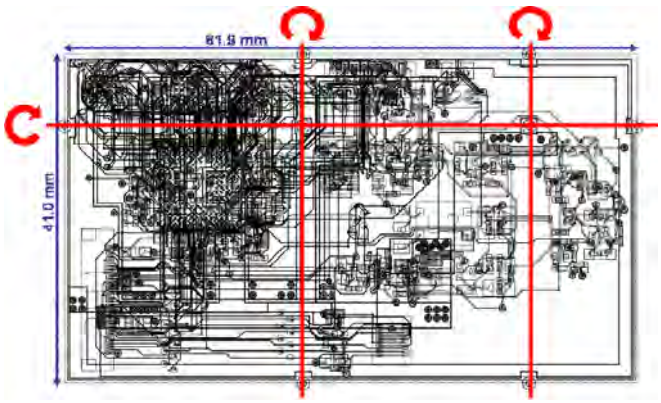

Figure 5.2: A flexible PCB for the driving electronics: the 3 flexing axes divide the substrate in 6 "rigid" islands onto which the components will be assembled, the punched holes at the intersection of the flexing axes are included to allow for bidirectional bending

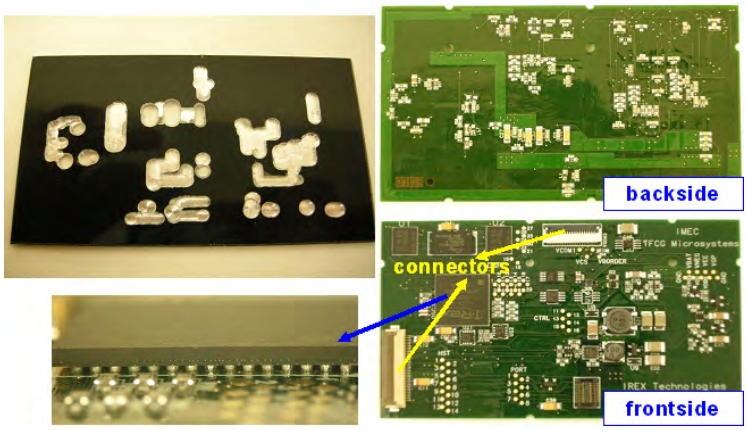

Figure 5.3: Double-sided assembly of a flexible PCB for the driving electronics: insets are created in the carrier fitting the components, namely the smaller passives, on the backside; the larger packages, including a very large IREX BGA, are assembled at the frontside

The components are then assembled onto this substrate by soldering. As this is a flexible substrate, it is fixed to a carrier for the reflow soldering process. The carrier is a metal plate covered by a black silicone layer, providing sufficient adhe-

sion by itself, which is necessary, because any double-sided tape cannot withstand the high temperatures reached in the reflow oven. Cavities are drilled to provide insets for the components on the backside, as the substrate has to be assembled on both sides. Figure 5.3 shows the carrier, as well as the result after assembly.

To be able to build this into a working flexible display demonstrator, an additional, 2-layer L-shaped foil was designed, fabricated and assembled, to interconnect the flexible driverboard with the flexible display. The final interconnection from the L-shaped foil to the display is formed by the row and column driverTCPs. The principle is shown in Figure 5.4.

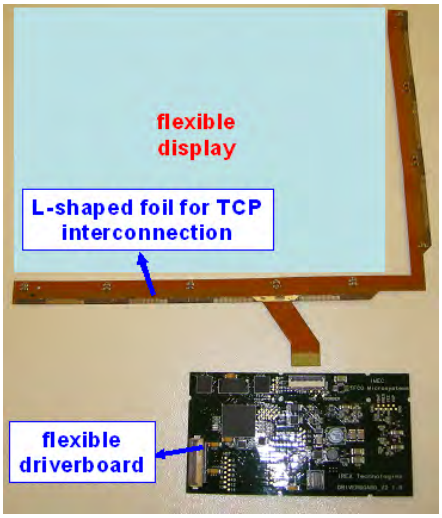

Figure 5.4: The flexible driving electronics module for driving a flexible display demonstrator, developed within FlexiDis

The complete assembly was carried out by IRex Technologies, and, after programming the electronics, was proven to work. The flexibility of the flexible PCB with driver electronics however, remains somewhat limited, as the commercially manufactured[2] 4-layer board still has a thickness of approximately 400 μm.

5.1.2 One-Sided Display Interconnection

As shown in Figure 5.1, the flexibility of the display is reduced to one corner when external driving electronics are attached directly to the rows and columns of the active-matrix busbars. This could be improved by bringing all connections to one

[2]by ACB

side of the display, so that the display will be bendable along one direction. Two possible options are slightly elaborated here.

The first and most obvious solution simply reroutes the row contacts next to the column contacts. The drawback is that the linear interconnection area on the display is increased significantly, proportionally reducing the active area of the display versus the total display backplane. This method was incorporated in one of the FlexiDis demonstrators, namely the one of which the assembly has been elaborated extensively in Section 4.3. In this case, the application in mind was a display that could be integrated in the sleeve of a ski jacket. The display would therefore be wrapped around the arm, or perhaps even curved permanently, so bendability in (only) one direction would be acceptable. The principle and application is illustrated in Figure 5.5.

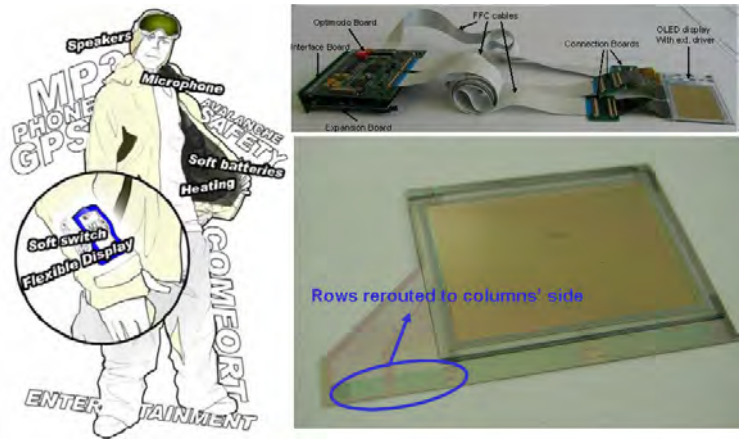

Figure 5.5: Concept (Pulsium) of a flexible display in a ski jacket's sleeve, as demonstrated within FlexiDis: rerouting the row contacts to the column side allows one-dimensional bending (electronics by Thomson)

Another solution involves including (row or column) driving electronics directly in the backplane design. This way, backplane processing can be used to integrate the drivers directly into the flexible display backplane. This is possible, because the active matrix already incorporates transistors, so that additional ones can be fabricated next to the active area. An important advantage of this method is that the number of interconnections is significantly reduced as the number of signals needed for the (row or column) driving circuitry is typically an order of magnitude lower than the number of rows or columns in high-resolution active-matrix displays: tens as opposed to hundreds of lines. There is also some proportional loss of active area to the display substrate, but much less than is the case of rerouting, as the area occupied by the driving circuitry can be made very small. A more important drawback of this integration, however, is that this driving circuitry

and the active-matrix is inherently fabricated at the same time, so they cannot be tested beforehand before assembling them together. This means that the yield is expected to drop. A design illustrating this method is shown in Figure 5.6.

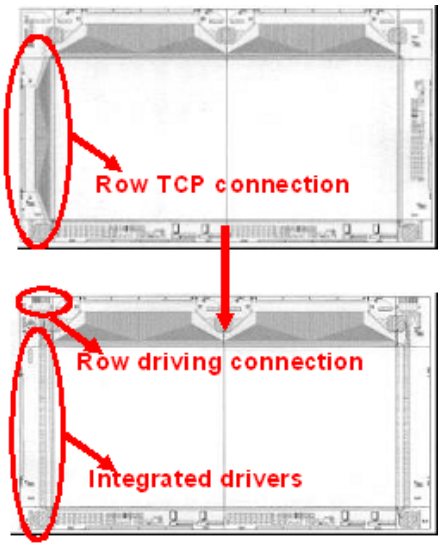

Figure 5.6: Integrating the row drivers in the backplane design greatly reduces the number of interconnections, while the space on the backplane taken away from the active area is practically negligible

Finally, a last nice example of this method of one-sided interconnection is shown in Figure 5.7.

Figure 5.7: Bridgestone's flexible QR-LPD (Quick Response - Liquid Powder Display), as shown at the FPD International 2007 exhibition in Yokohama

5.1.3 Reinforcement of the Fragile Interconnection Areas

Reinforcement is an obvious solution in the sense that the flexibility is not so much restored locally, it is on the contrary actually less flexible, but the bending and corresponding stress is rather redirected to the more flexible areas.

A first good example is given by what is common practice in standard PCB manufacturing, when bare dies are assembled. In case the chips are glued on the PCB face up, usually with electrically (and thermally) conductive adhesive to control the silicons bulk potential, the contacts on the chip are wirebonded to the pads on the PCB, and the assembly is reinforced with an encapsulant, a so-called globtop, for protection of the fragile wirebonds against mechanical damage as well as environmental degrading influences. In some cases, the dies are directly flip-chipped onto the PCB, with (conductive) adhesive forming the electrical interconnection between chip and PCB, as explained in Section 2.4.3.1. Then, the bond is often reinforced by underfilling the assembly with a non-conductive adhesive. These types of reinforcement are illustrated in Figure 5.8.

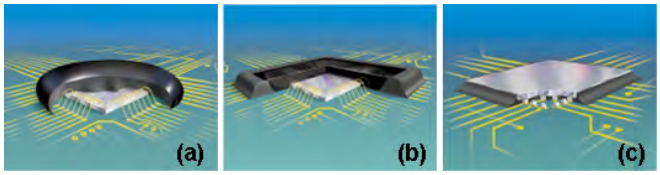

Figure 5.8: Reinforcement through encapsulation without (a) or with the aid of a damming material (b), or through underfilling (c)

Another nice illustration of reinforcement is shown in PolymerVision's first Readius prototypes, as shown in Figure 5.9.

Figure 5.9: The Readius (PolymerVision) is a nice example of how the flexibility (rollability) of the display is optimally used, while the electronics and interconnection area is reinforced and protected by the rigid casing

A final example has already been discussed in Section 3.2.3. As shown there in

Figure 3.11, the larger rigid components, such as the rigid display, microcontroller and battery, are embedded in a thicker silicone, making these parts less elastic and transferring the flexing stress to the thinner silicone encapsulated interconnection lines.

5.2 “Weight” of Flexibility in Flexible Displays

References: [81]

Although “flexible” accounts for half of the letters in “flexible displays”, it is not considered the main benefit, at least not yet. Companies that are marketing their flexible display products, are not so much emphasizing the flexibility, but rather the light-weight aspect, related to the thinness, and the robustness, as no dangerous breakage as with glass is possible. Of course the flexibility has a wide range of interesting applications, but this potential is, as with most innovations, initially exciting only to a limited amount of people. That the general public is not yet fully convinced, may very well be due to the fact that it has to adopt the notion of its possibilities, as well as that flexible displays are not widely available just yet.

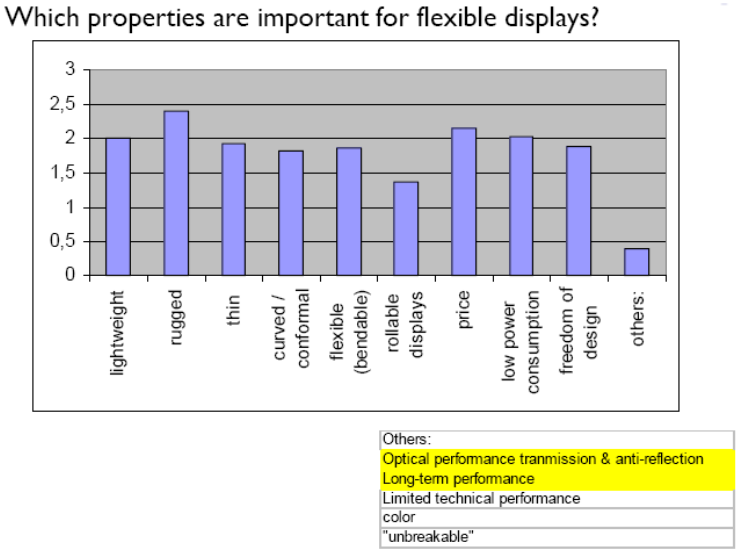

Figure 5.10: A questionnaire illustrates which properties might be important for flexible displays as considered by european flexible display consortium (FlexiDis) members

To illustrate, in Figure 5.10 is presented the result of a questionnaire filled in by the partners in the FlexiDis project. Note that price is also a very important factor: it is expected that flexible displays could be made using reel-to-reel processing

technology, which would mean high volume output, possibly cutting down on the manufacturing cost.

5.3 Embedding Technologies

References: [1], [84], [85], [86], [87], [88], [89], [90], [91]

In an attempt to overcome the aforementioned restrictions on flexible displays imposed by the driving electronics, embedding technologies are increasingly being considered as suitable candidates for integrating electronics inside advanced microelectronics (flexible) substrates.

First, a background to embedding technologies is presented, followed by some examples that illustrate its applicability. Finally, a novel embedding technology is introduced that allows for very flexible electronic circuitry.

5.3.1 Background of Embedding Technologies

Considering the current trend of increasing component density, which is of course welcomed for wearable devices, the benefit of the flexibility of the substrate is more and more overshadowed by the rigidity of the components. An obvious way of tackling this issue is to use smaller and thinner, and consequently also lighter components. This is a trend already in progress, as is clear when one looks at the evolution of packages and compares them chronologically: from DIP over SO and PLCC down to chip-size packages (CSP) such as QFPs and BGAs. Going smaller even still, we encounter assembly of bare dies, e.g. with a flip-chip (FC) technology, and even backlapping the dies before assembly, making them thinner. However, whereas the backlapping technique currently used reduces the chips' thickness to 400, maybe 200 μm, even thinner devices, down to 20 μm, are needed before they can be considered truly flexible. Such thin chips are, unfortunately, too fragile to assemble them onto a substrate with standard die assembly techniques. This evolution is illustrated in Table 5.1 and Figure 5.11.

Package Name	# Contacts N	Thickness T [mm]	Weight W [g]	Area A [mm^2]	$\frac{W}{A \cdot N}$ [g/μm^2]
DIP	24	3.68-4.64	3.55	32x14	330
SO	24	2.3-2.5	0.73	15.4x7.5	263
PLCC	44	3.87-4.38	2.4	16.6x16.6	197
SSO	24	1.75-2	0.19	8.2x5.3	182
QFP	44	2-2.45	0.56	10x10	127
SO	44	2.3-2.8	2	28.2x13.3	121
QFP	44	1-1.2	0.28	10x10	64
BGA	256	1-1.5	0.74	19x19	8
bare die	338	0.65	0.05	2.5x15	4
thinned die	172	0.02	≤ 0.002	5x5	≤ 0.5

Table 5.1: Evolution of packages (indicative examples)

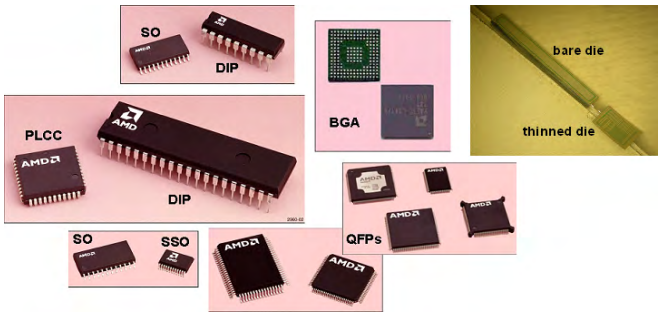

Figure 5.11: Pictures of the packages in Table 5.1

A solution for this mechanical issue, inherently linked with the brittle nature of silicon dies, is switching from assembly to embedding technologies, where the chip is sandwiched in between two layers of substrate material. This protects the chip mechanically if the stress on the chip is sufficiently transferred to the substrate, by integrating the chip close enough to the neutral axis of the layer stack, where stresses and strains are theoretically non-existent. Depending on the properties of the outer (barrier) layers, the chip may also be shielded from outer degrading influences, such as moisture, heat and chemicals. After embedding, the chip is contacted through the substrate and interconnected with a conductive pattern on top of the substrate.

Following this logic, the overall advantage of embedding is therefore three-fold: it allows for a compacter design, advantageous for reducing parasitics and improving footprint efficiency, while at the same time tolerating more mechanical flexibility, and protecting the device from outer influences (and vice versa) due to a smaller interface to the outside world.

On the downside, embedding involves more complex processes, such as thinning the chips and making the via contacts, either by punching, laser drilling or etching of the substrate as well as plating them. Also, the handling and placing of thin chips, is not yet standardized and quite delicate at the moment.

5.3.2 Examples of Chip Embedding Technologies

An application of embedding chips that is already in effect around the world, are smart cards: cards with intelligence added by incorporation of chips, e.g. credit cards, memory cards for a digital camera, SIM cards for a cellphone, ... Smart cards aren't new. They were introduced two decades ago in the form of (not so smart) memory cards, used to store critical phone information with the purpose of reducing thefts from payphones. In some areas of use, smart cards are just memory cards that merely provide protected non-volatile storage. More advanced smart cards have both microprocessors and memory, for secure processing and storage, and can be used for security applications. Currently, most smart cards don't contain a battery, and become active only when connected with a card reader, either through the card's physical contacts or contactless, when communication is achieved by means of a radio frequency signal. Figure 5.12 illustrates smart card technologies.

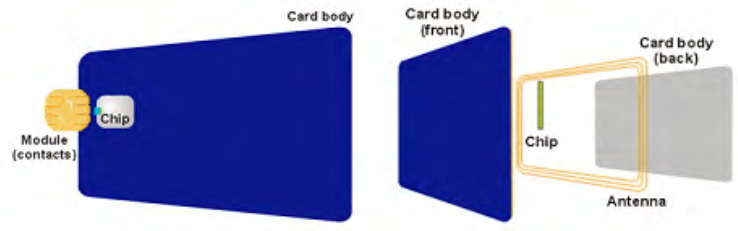

Figure 5.12: The principle of a smart card: with physical contact (left) and contactless (right)

In the latest developments, batteries and even buttons and displays are integrated in the thin cards that have to be durable, with a functional lifetime of several years. In the case of smart cards, the actual embedding usually consists of laminating the functional prefabricated electronic circuitry in between two layers of plastic, commonly polyvinylchloride (PVC) and/or polycarbonate (PC). A commercially available product here is shown in Figure 5.13.

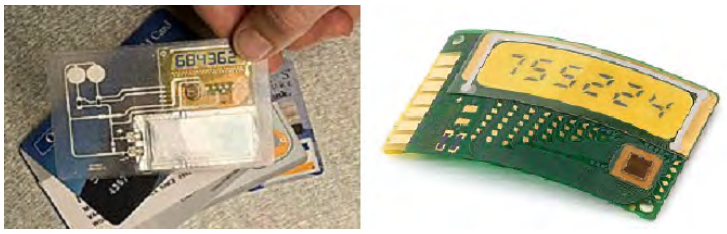

Figure 5.13: A prototype (left) and the Primero, a commercially available flexible display module for card applications (Aveso, Inc.); the used display technology is invented by The Dow Chemical Company and is based on electrochromism

Chip embedding is also interesting for application in standard PCB buildup layers. Figure 5.14 shows some results of embedding work done within the frame of another european project, aptly named "Hiding Dies". The dies embedded here are around 50 μm thick. Another embedding method, the Occam process as proposed by Verdant Electronics, is given in Figure 5.15.

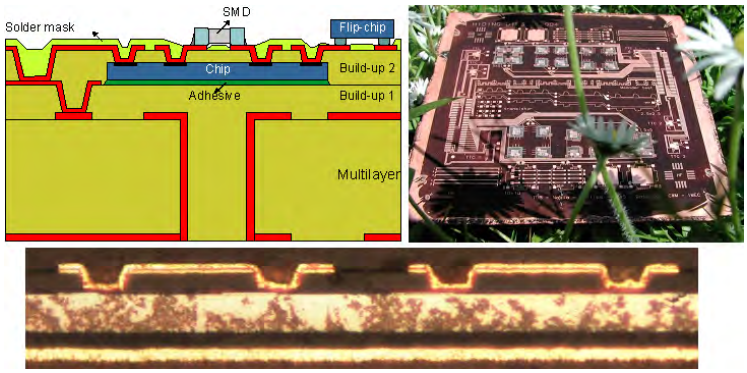

Figure 5.14: Research within "Hiding Dies" involves embedding thin dies in the buildup layers of a PCB

Of course, this approach of embedding thin chips offers opportunities for chip stacking: whereas in standard assembly chip packages with thicknesses in the range of millimeters are surface mounted onto the PCB, several thinner chips e.g. 50 μm can be stacked. This way, the total assembly would still be significantly thinner, and footprint efficiency could be dramatically increased.

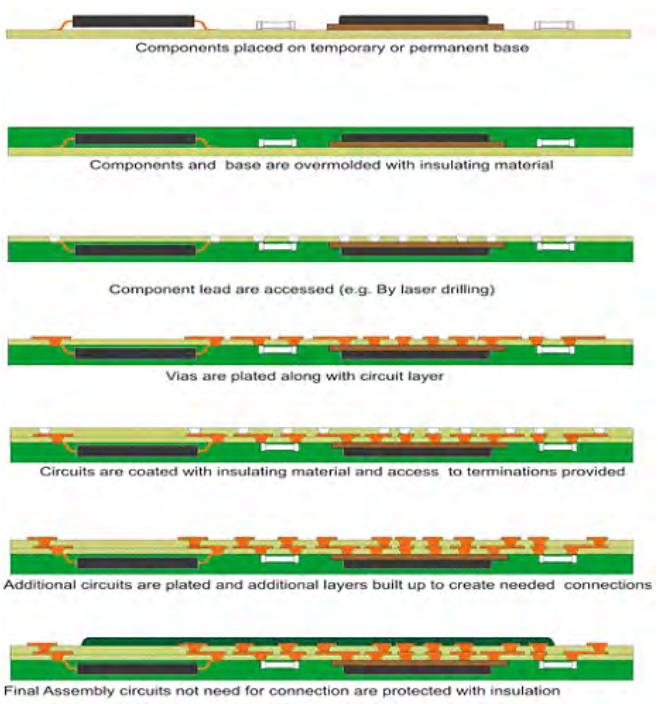

Figure 5.15: The Occam process (Verdant Electronics) proposes another route towards embedding

Where displays are concerned, the option of integrating drivers, as already brought up in Section 5.1.2, can also be considered an embedding technology, definitely. However, this kind of embedding leads for many applications to too much integration, as it means that all devices and materials are exposed to all fabrication steps, which could be problematic in some cases. This drawback was also (somewhat differently) brought up in Section 5.1.2.

5.3.3 Ultra-Thin Chip Packaging (UTCP) Technologies

The aforementioned examples clearly illustrate that chip embedding is already in effect for some applications, as well as under continuing development throughout the world. However, in pursuit of ever thinner circuitry, embedding technologies should be advanced to allow embedding of components within free-standing flexible substrates, without excessive limitations on the bendability of the result.

As a possible solution to these needs, ultra-thin chip packaging (UTCP) technologies were developed at IMEC. This was conceived within SHIFT[3], a european

[3]acronym for Smart High-Integration Flex Technologies

FP6 project working on advanced technologies for flexible electronics. First the principle was proposed, soon followed by the first trials, confirming the feasibility. The original process flow is shown in Figure 5.16, some first results in Figure 5.17 and a cross-section in Figure 5.18.

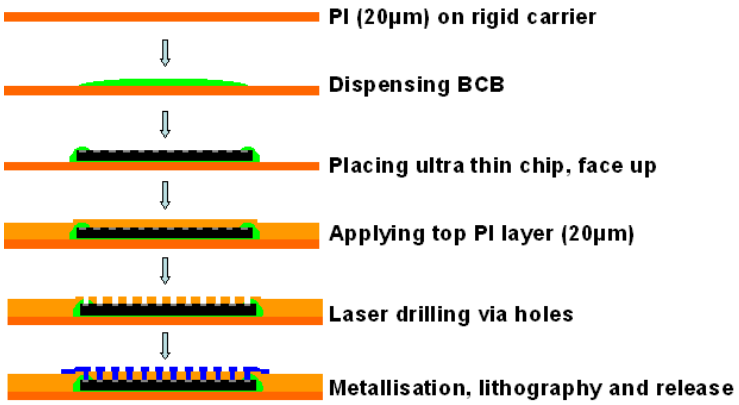

Figure 5.16: Process flow of the first UTCP techology, illustrating the principle

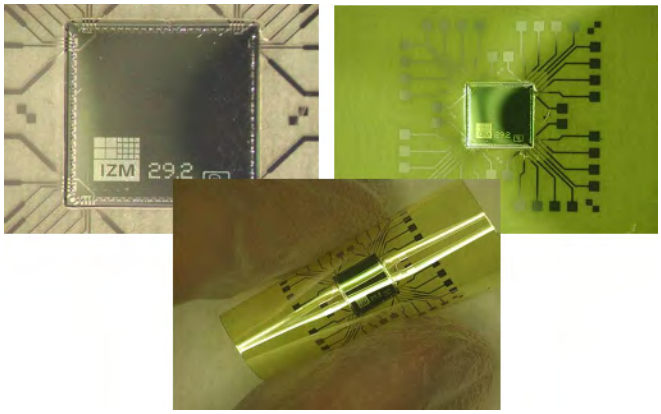

Figure 5.17: Pictures of the first results achieved for the UTCP technology

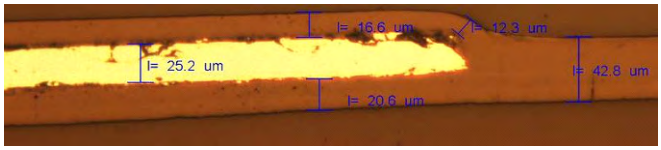

Figure 5.18: A cross-section of the fabricated UTCP illustrates the thicknesses of the different layers

The chips are thinned down, down to 25 μm, and possibly even lower, and this is where the flexibility is introduced to the functional chip itself. However, as already stated in Section 5.3.1, the flexibility also emphasizes the fragility of the silicon, resulting in difficulties for assembly and whenever handling is needed.

The PI is spun onto a rigid glass carrier, allowing standard processing steps. A drop of BCB is dispensed on the substrate and acts as an adhesive when the chip is placed on top, with the active side facing upwards. After thermally curing the adhesive, another layer of PI is spun on top, effectively sandwiching the chip between two layers. Then, via holes are drilled to the chip's contacts, and metallization ensures electrical interconnection to the chip. Finally, the whole can be released from the glass carrier.

Acknowledging the possibilities of this type of technology, the principle of UTCP was also introduced to the FlexiDis program. The technology could either be used to replace existing driverpackages, or to directly embed the chips inside the display substrate. A slightly modified version of the original UTCP technology was developed, adapted to better suit the needs for the latter purpose, embedding chips inside the display substrate. The development of this technology is extensively described in Chapter 6, together with improvements, applications and implications.

5.4 Conclusion

In summary, several routes are possible to resolve flexibility issues in flexible displays connected with the necessary driving electronics. Most of these solutions merely involve removing the symptoms, but do not really address the underlying problem: that any functional silicon chip needed for driving the display is rigid, thereby introducing a limitation to the flexibility of the entire module.

This might possibly be solved by thinning down the chips and embedding them in thin, flexible substrates. This option, with several possible variants, is under investigation and development and is better known and disseminated as UTCP, or ultra-thin chip packaging.

6
Flat UTCP Technology

"Engineers are all basically high-functioning autistics who have no idea how normal people do stuff."

— Cory Doctorow (1971 - ...)

6.1 Process Flow

The technology investigated here is an enhanced version of IMEC's first UTCP technology, as discussed in Section 5.3.3, with an updated process flow to realize a symmetrical substrate sandwich. The updated process flow is depicted in Figure 6.1. Polyimide (PI) is used as substrate material, because it is a high-quality plastic, capable of withstanding high temperatures.

The base PI layer is spincoated onto a rigid (glass) carrier substrate and cured. Then the photodefinable PI is spincoated, illuminated through a mask and developed to define the chip cavity. After curing, the thinned-down chip is placed face up, using BCB in the cavity as adhesive. The BCB is cured, and the top layer of PI is spincoated and cured in the same way as the base PI layer (thus creating a symmetrical substrate sandwich). The via holes to the chip's contacts are laser drilled and after the metal pattern is realized on top, the substrate can be released from its carrier.

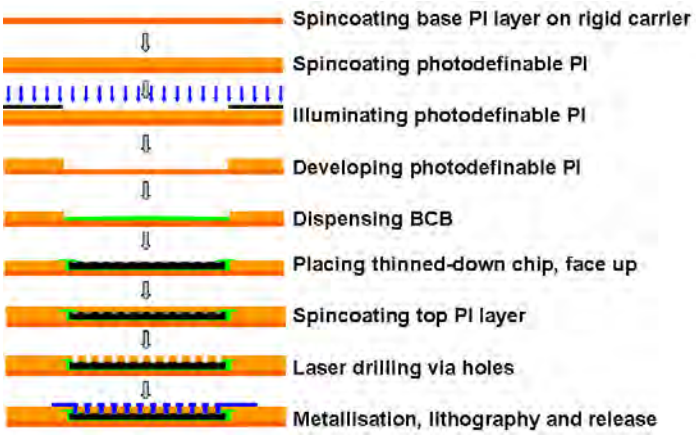

Figure 6.1: Process flow design for the flat UTCP technology

6.2 Setup and Design

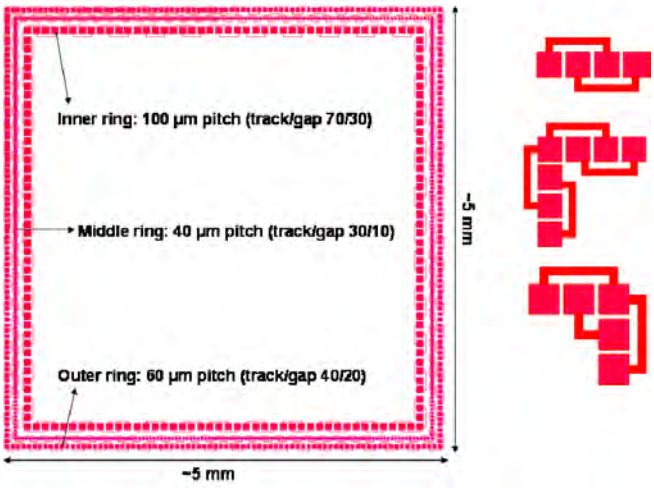

Figure 6.2: The bond pads of the PTCK test chips are located at the periphery and come in 3 pitches, 100, 60 and 40 µm, a more zoomed view on the right shows the different interconnection schemes on the chip

To test the feasibility of the technology a design for the UTCP metallization was made based on the layout of the test chips. The chips used for the embedding trials are thinned-down test chips available at IMEC. They are specified as PTCK chips,

which stands for “Packaging Test Chip version K”, and measure 5 mm by 5 mm. There are four different versions of PTCKs, but all have the same peripheral bond pad layout, which is all that is of interest here. This bond pad layout, and how they are connected, is shown in Figure 6.2.

The metal on the substrate is to be patterned so that, fitting the test chips, a daisy chain (DC) can be measured at several points, as well as contact resistance with a 4-point-probe method (4PT). The principle is illustrated in Figure 6.3.

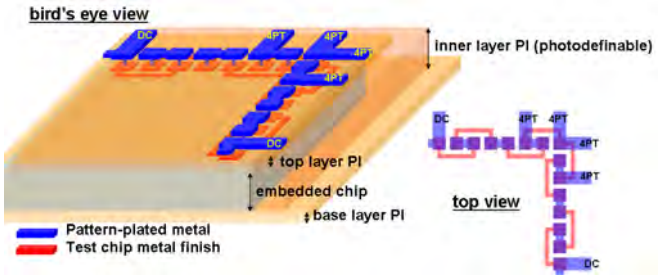

Figure 6.3: Interconnection test pattern design

The chips themselves have been thinned down from about 500 μm to approximately 20 μm. The result of this thinning process is given in Figure 6.4, for a functional chip. Also it is illustrated in Figure 6.5 how thin the test chips really are, by illuminating one from the back: the silicon has become somewhat transparent so that the metal patterns on the front can easily be identified with illumination only from the backside. The bond pads of the test chips have been bumped with NiAu, approximately 5 μm; this acts as a buffer layer for the laser drilling, to protect the Al contacts. The test chips' peripheral bond pads are designed with several pitches 100, 60 and 40 m, with corresponding bondpads 70 μm by 70 μm, 40 μm by 40 μm,and 30 μm by 30 μm.

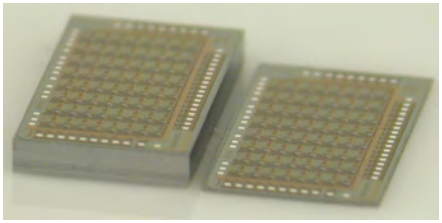

Figure 6.4: A functional chip before and after thinning

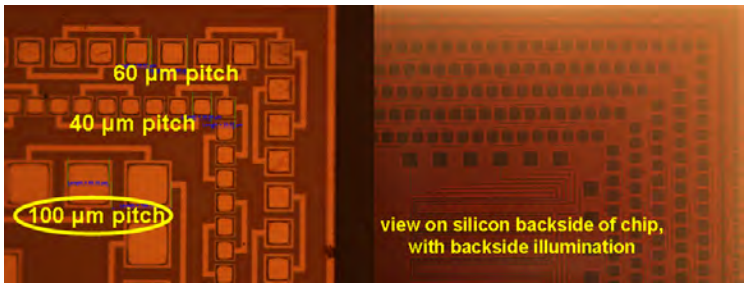

Figure 6.5: A thinned-down test chip: zoom on the different peripheral bond pads to be used (left) and a view of a backlit test chip illustrating the thinness (right)

6.3 Substrate Materials

References: [92]

The substrates in which the chips are embedded consist of three layers of PI, a high-quality plastic that can withstand temperatures well in excess of 300°C, and have a symmetrical layer build-up. The materials used come from HD microsystems and are both spincoatable PIs. The layers are built up on a clear glass carrier, where adhesion promotor is applied at the edges to keep the substrates attached to the carrier during processing. Afterwards, the fully processed UTCP is released by cutting out the part of the substrate that is not attached to the carrier.

The outer layers, base and top PI layer, are Pyralin PI2611, and the inner layer is HD7012, a photodefinable PI, wherein the chip cavity is defined by a lithographic step. Both are spincoated at 3000 rpm for 60 seconds, but as HD7012 is more viscous, this inner layer will be thicker: 36 μm after curing, as opposed 5 μm for the outer layers. The curing step is also the same for both materials: from room temperature to 200°C at a rate of 4°C/min, then waiting at 200°C for 30 minutes, after which the temperature is increased to 350°C at a rate of 2.5°C/min and this temperature is kept for 60 minutes. The oven should then be allowed to cool off to room temperature. The curing is done in a vacuum-oven with a nitrogen flow of 5 sccm to drive out the solvents.

The cavities in HD7012 are defined as follows. After spincoating, the substrates are dried on a hotplate. After illumination, the samples should be laid to rest for an hour (this is an important step). Finally, developing the PI is done with a dedicated developer and then rinsed. The manufacturer recommends using spray-etching, but as this was not an option in the lab it was done in a beaker with ultrasonic agitation (USA). Some pictures are given in Figure 6.6 to show the possibilities.

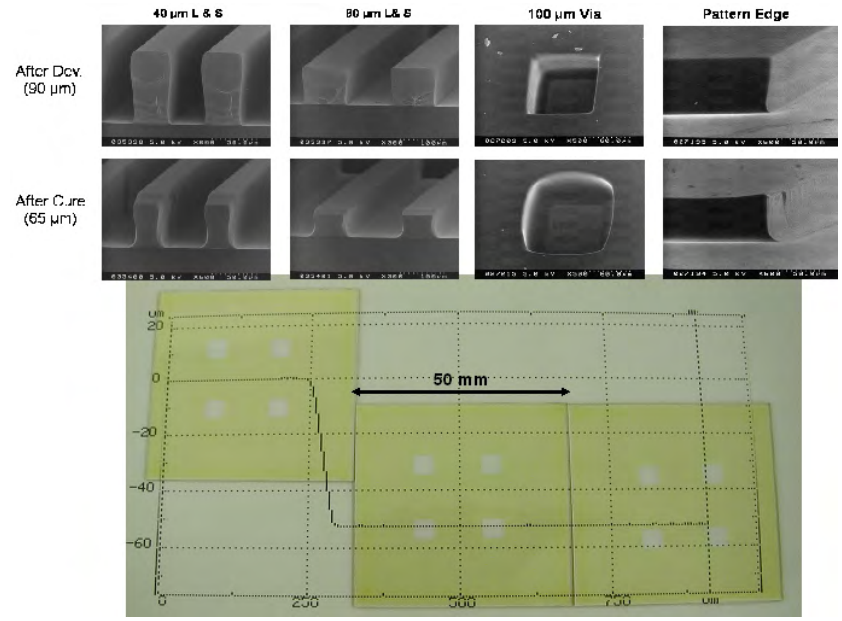

Figure 6.6: Defining cavities with the photodefinable HD7012: SEM pictures from results in the datasheet (top) and cavities achieved (bottom)

6.4 Flat UTCP Fabrication

References: [1], [93], [94]

The device is built up on a glass substrate, 5 cm by 5 cm. Three layers of spin-on PI, all supplied by HD Microsystems, are involved, and in what follows, they are referred to as, from bottom to top, the base PI layer, the inner (photodefinable) PI layer and the top PI layer. This layer buildup is symmetrical, with both base and top layer being PI2611 and the inner layer being HD7012, to avoid problems with CTE (Coefficient of Thermal Expansion) mismatch, usually resulting in curling of the substrate when the release is carried out. The base layer is attached to the rigid glass carrier with adhesion promotor only at the edges of the carrier, so that later on, the middle area can be cut out and removed off its rigid carrier.

Before spinning the base PI at the final speed, shortly spinning at a lower speed, say 500 rpm for a few seconds, is preferable to spread the highly viscous PI a little. Following this, the spinning speed is increased to 3000 rpm for 45 seconds to get a 5 μm thick layer after curing. The curing is done in a vacuum oven (with 5 sccm nitrogen flow), with the following temperature profile: from 20°C (also known as room temperature) to 200°C with a ramp of 4°C per minute, then holding this 200°C for 30 minutes, another increase to 350°C with a ramp of 2.5°C per

minute and finally keeping this 350°C for 60 minutes. The whole curing process takes about 7 hours. This includes the time needed for cooling down, when the substrate is left in the vacuumoven until the temperature has dropped back to room temperature.

The next layer consists of photodefinable PI, wherein the cavities for the chips are to be made. The PI used for this is HD7012. This layer is applied in a similar way, on top of the base PI layer, but before spinning, it is preferable to plasma-etch the base layer to improve adhesion. This is done by RIE (Reactive Ion Etching), first 2 minutes with a 5 sccm-CHF_3 / 20 sccm-O_2 plasma and next another 2 minutes with a 25 sccm-O_2 plasma, both at a power setting of 150W and a pressure of 100 mTorr.

Spinning the HD7012 is done with the same parameters, namely 5 seconds at 500 rpm followed by 45 seconds at 3000 rpm, although this now results in a thickness after curing of approximately 36 μm (HD7012 is with 31.5 Pa·s still more viscous than PI2611 with 11-13.5 Pa·s). As this is the photodefinable layer, the following process steps are somewhat different. First a soft-bake is introduced to the PI on a hotplate: 4 minutes at 60°C, then 4 minutes at 90°C and ultimately 4 minutes at 110°C. Photodefining the cavities means lithographic processes are involved, and in this case illumination is needed for 28 seconds. At this point it is crucial that the substrate is illuminated on a black background: since the substrate, a glass carrier with a PI base layer, is transparent, the UV-light should be absorbed to avoid random scattering when it is reflected on a white background (resulting in poorly defined edges). It is then advisable to wait for approximately half an hour, allowing the PI to take in the effect of the illumination.

Development should then be successful when the substrate is put in PA400D for 90 seconds with ultra-sonic agitation (USA) and then rinsed in PA400R for 15 seconds. Both chemicals PA400D and PA400R were again obtained from HD Microsystems. After this dry carefully but thoroughly with a nitrogen pistol. If this is done properly, the cavities in the PI can easily be identified. The next step is again to cure this layer as well and the same curing setup and profile can be used as with PI2611, solidifying the layer at 350°C. Figure 6.7 shows the results at this point.

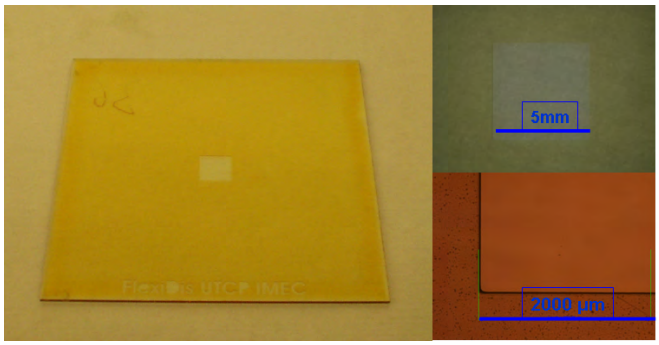

Figure 6.7: A cavity created in the photodefinable PI layer: two close-up top views of the cavity are shown on the right

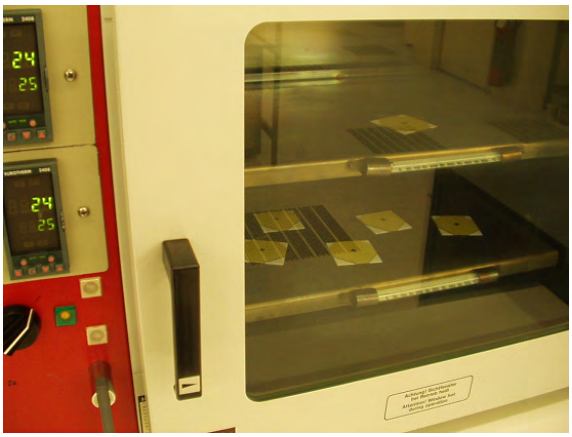

Figure 6.8: After aligning and placing the chip, the BCB is cured in an oven

The chip is then placed inside the cavity using a mask aligner. The cavity of the substrate is dotted with BCB that will act as adhesive: one drop of 30 nL, applied by micropipette, is sufficient for 5 mm by 5 mm cavities. The substrate is then hung upside down in a mask adapted for vacuum holding of substrates, while the chip is placed face down on the movable substrate table of the mask aligner. When aligning is done (under the microscope), the substrate is lowered carefully onto the chip and the drop of BCB should flow out evenly under the backside of the chip. The substrate can be released from the mask holder and turned over (the adhesion between chip and cavity bottom is at this point already strong enough due to the BCB. To cure the BCB, heating up to 250°C is sufficient from the BCB's point-of-view, but since the next cure step will again go up to 350°C (curing of the top PI layer), it is preferable to also use the same curing scheme here as for the PI layers. In Figure 6.8 the curing step is shown, and in Figure 6.9 a height

measurement of the result. It is clear that the PI cavity, 36 μm deep, is actually too thick with regards to the chip, being only 20 μm thick.

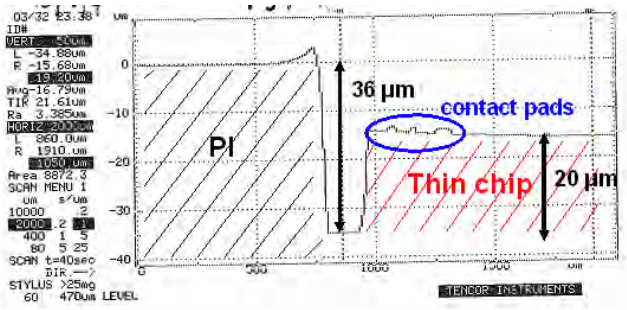

Figure 6.9: An AFM (Atomic Force Microscopy) measurement shows that the PI layer is thicker than the thin chip, and even the bumped contact pads can be spotted

Now that the chip is safely inserted, the top layer needs to be applied to cover it all up. Again the substrates are plasma-etched to improve adhesion, and as PI2611 is not self-priming, in contrast to HD7012, also adhesion promotor has to be spun onto the plasma-etched active surface. This is done for 30 seconds at 3000 rpm, and is followed by a 1-minute softbake at 120°C. The top layer is spun and cured in the same way as the base layer, to have the same layer thickness and a symmetrical package (in cross-section).

Now that the chip is embedded and covered up by the top PI layer, holes have to be drilled through 5 μm PI so that the chip's bumps (5 μm thick electroless NiAu, as mentioned earlier) can be contacted. The drilling is done with a 355-nm-YAG-laser (laser via drilling)[1] outside of the cleanroom, using 26 A and an attenuation to 300 mW, a circular mask of 200 μm diameter and a Gaussian beam, 100 pulses at 10000 Hz. The resulting vias have a diameter of on average 12 μm, and are shown in Figure 6.10 below. This combination of attenuation and via size corresponds to a laser beam power received by the PI of approximately 111 mW, as can be calculated by supposing a Gaussian beam intensity profile[2].

[1] more specifically, a Nd:YAG-laser (Neodymium-doped Yttrium Aluminium Garnet; Nd:Y_3Al$_5$O$_{12}$) was used

[2] the beam's irradiance distribution

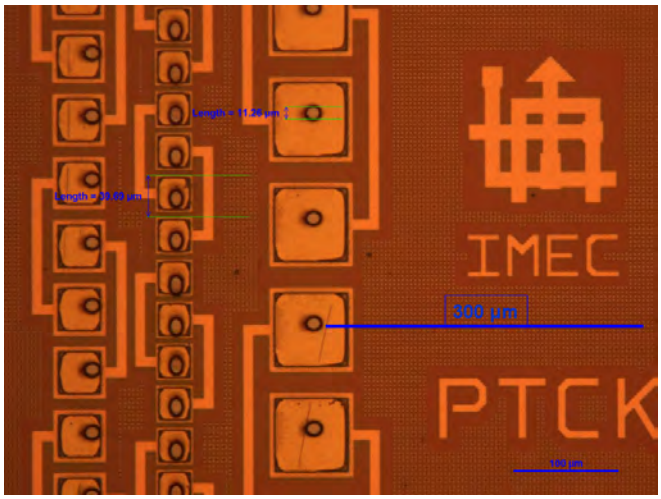

Figure 6.10: Laser drilled via holes in the top PI layer to contact the bumped contact pads of the chip underneath, for all three types of bond pads

The next layer that needs to be put in place is the metallization layer, that has to route the chip contacts across the substrate. To achieve this, pattern plating is the preferred option, as bare chips typically have fine features, in this case bond pad pitches down to 40 μm. First, the surface with the top PI layer is prepared by plasma-etching to enhance adhesion in the same way as described above. Then a metallization seed layer is deposited by sputtering: 50 nm of TiW as interface followed by 500 nm Cu for electroplating. Then the (inverted) pattern is aligned and defined in a photoresist layer by standard lithography. Note that, as the Cu will be plated into the holes, it is important to have a sufficiently thick layer of photoresist. Aiming for a Cu thickness around 6 μm, the photoresist is spun at 2000 rpm, nominally resulting in a 7.5 μm thick photoresist layer. This layer is soft-baked in an oven, 30 minutes at 90°C and then illuminated for 20 seconds under a UV-lamp with an intensity of 10.5 $\frac{mW}{cm^2}$.

After the photoresist has been developed, approximately 2 minutes in a standard developer, and baked for 30 minutes at 120°C in an oven, the substrate is ready for electroplating. There is a formula used in practice[3] that allows calculating the time needed for plating a certain thickness at a certain current intensity and a certain area to be plated. Relying on this formula, plating would be sufficient (over 6 μm) at 10 $\frac{mA}{cm^2}$ for 30 minutes (so 30 mA if a plating area of 3 cm^2 is used). However, this proved to be false in the used setup, as too little plating was achieved and, even worse, this plating was very inhomogenously divided over the surface. Instead, for the same plating area of 3 cm^2, 15 minutes at 120 mA gave satisfy-

[3] to be found e.g. in [94]

ing results: approximately 7 μm over the whole surface area. The electroplating process is illustrated in Figure 6.11.

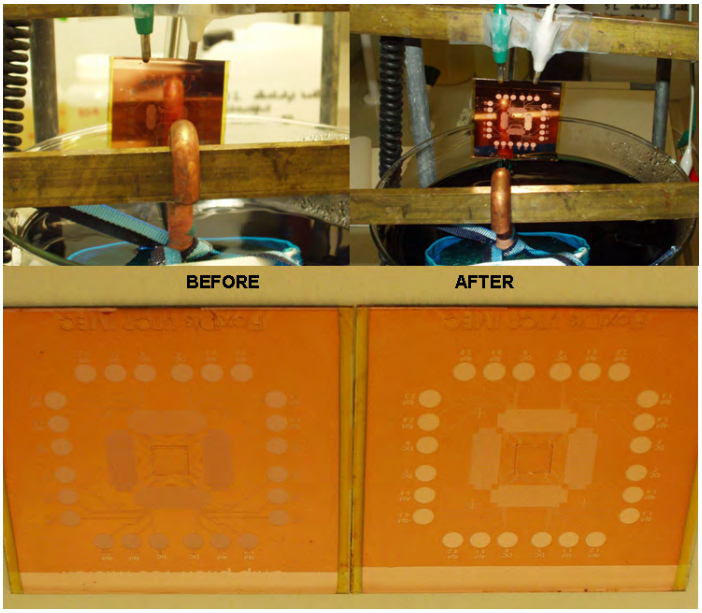

Figure 6.11: Electroplating the UTCP for the metallization layer by pattern plating

At this point, the whole surface is evidently still shorted by the remaining seed layer, so this remains to be etched. After stripping the photoresist pattern that has been used for the pattern plating process, the seed layer is available for etching. Some standard ways of etching Cu (which is the top seed layer in this case) involves warm solutions of $FeCl_3$ and $CuCl_3$, but these turned out to be too aggressive and wiped out most of the plated patterns, even when diluted four times and at less elevated temperatures. A simple solution can however be found, by using a standard micro-etch solution. An 80-seconds-dip, followed by 10 seconds in a 10%-HCl-solution to clear any remaining Cl^--ions from the surface, is sufficient for the used 500 nm Cu seed layer. The TiW seed layer should then be clearly visible, and can be etched, 10 seconds in warm H_2O_2 (52°C) and then 15 seconds in cold H_2O_2 (room temperature). Especially the warm etch process has to be carried out very carefully, as this is a very quick process, meaning that the processing window is rather narrow, and underetch can be a problem. Rinsing and drying then concludes the process steps needed for the metallization layer. The metallization process is summarized in Figure 6.12, including soldermask deposition and plating of the contacts on the substrate. Figure 6.13 shows some results after the last step of the metallization process, being the seed layer etch.

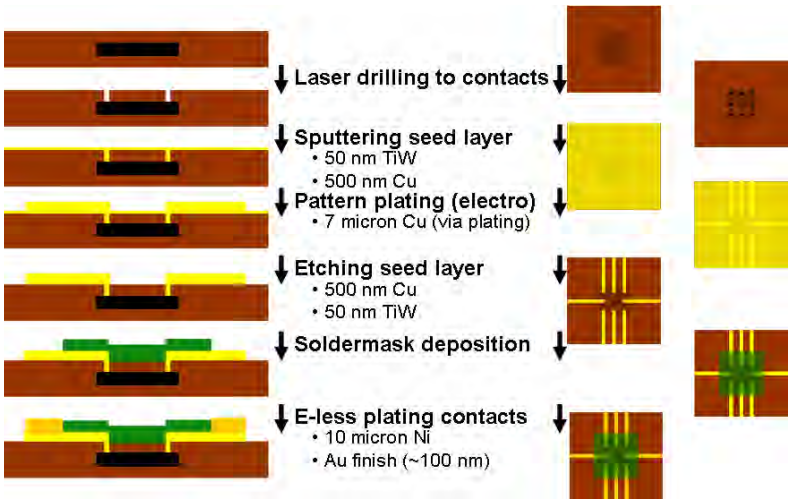

Figure 6.12: Schematic representation of the metallization process

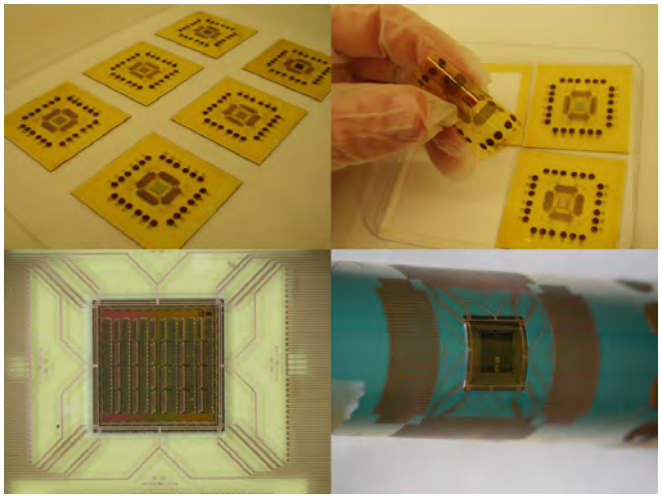

Figure 6.13: The results after the seed layer etch

As is common in PCB and flex technologies (and this is therefore not elaborated here), soldermask is then applied to cover up everything but the contact areas, so as to protect the Cu tracks against oxidation and corrosion, and the contacts can then be plated up electrolessly with Ni to the desired thickness, typically a few μm. A Au finish is finally applied on the Ni surface of the contacts to improve (i.e. lower) the contact resistance of the contacts.

Now the finished substrate can be cut out and released from the glass carrier.

6.5 Characterization

The electrical measurements done on the first batch of fabricated UTCPs can be found in Tables 6.1 and 6.2. DCx-y in Table 6.2 means that the resistance between the contact pads marked with DCx and DCy has been measured. Please note that DC8-7 is mentioned twice in Table 6.2, and it should be mentioned that the 4-point measurements are uncomfortably close to the lower limit of the SMU's range, meaning that it is significantly below 10 mΩ.

# Measurements	Mean value [Ω]	Remarks
18 (out of 44)	0.0016 ± 0.0007	done @ 100 mA

Table 6.1: 4PT-measurements for the 100 μm patterns [Ω]

DC	# Measurements	Mean Value [Ω]	# Connections	# UTCP Squares	# chip Squares
8-7	8 (out of 11)	18.78 ± 0.53	42	448	506
8-5	9 (out of 11)	35.80 ± 1.19	84	322	1012
8-3	9 (out of 11)	53.00 ± 2.55	126	472	1518
8-1	10 (out of 11)	70.12 ± 4.32	168	346	2024
7-6	8 (out of 11)	1.28 ± 0.23	0	562	0
5-4	9 (out of 11)	1.08 ± 0.88	0	298	0
3-2	10 (out of 11)	1.32 ± 0.18	0	562	0
8-7	8 (out of 11)	18.78 ± 0.53	42	448	506
6-5	8 (out of 11)	18.49 ± 0.33	42	436	506
4-3	10 (out of 11)	18.53 ± 0.41	42	448	506
2-1	9 (out of 11)	18.84 ± 0.40	42	436	506

Table 6.2: DC-measurements for the 100 μm patterns [Ω]

The first batch contained 15 substrates, of which 4 failed in the course of processing. Each substrate was patterned with 4 four-point-probe patterns, and one complete peripheral daisy chain, measurable at 8 contacts. The batches used here for characterization still suffer from a lot of problems bridging the gap at the chip-cavity interface, explained in 6.7.1. This means not all patterns on all substrates have been measured, as indicated in the second column of the tables.

Table 6.1 shows consistent results for the contact resistance of 1.6 ± 0.7 mΩ. This represents the contact resistance of 9 parallel via holes[4]. Table 6.2 teaches

[4]this is clarified in Section 6.7.1, around Figure 6.33

that the metallization on the UTCP, as measured in DC7-6, DC5-4 and DC3-2, has a somewhat larger resistance value per square, being approximately 2.75 $\pm$ 0.76 m$\Omega/\Box$. Using these figures, and the measurements in Table 6.2, a recalculation results in a value for the on-chip metallization resistance of, again approximately, 34 $\pm$ 0.3 m$\Omega/\Box$, which is acceptable for the standard metal (aluminum) layer of the test chips.

Similar measurements were done for the 60 μm patterns and the 40 μm patterns, and the results are listed in Tables 6.3, 6.4, 6.5 and 6.6.

# Measurements	Mean value [Ω]	Remarks
9 (out of 12)	0.006 $\pm$ 0.005	done @ 100mA

Table 6.3: 4PT-measurements for the 60 μm patterns [Ω]

DC	# Measurements	Mean Value [Ω]	# Connections	# UTCP Squares	# chip Squares
8-7	1 (out of 3)	26.00	78	525	500
8-5	2 (out of 3)	46.70 $\pm$ 4.81	156	436	1000
8-3	1 (out of 3)	74.50	234	575	1500
8-1	1 (out of 3)	98.80	312	486	2000
7-6	3 (out of 3)	1.40 $\pm$ 0.40	0	612	0
5-4	2 (out of 3)	1.10 $\pm$ 0.42	0	386	0
3-2	3 (out of 3)	1.40 $\pm$ 0.36	0	612	0
8-7	1 (out of 3)	26.10	78	525	500
6-5	2 (out of 3)	23.70 $\pm$ 2.97	78	523	500
4-3	2 (out of 3)	23.75 $\pm$ 3.04	78	525	500
2-1	3 (out of 3)	27.93 $\pm$ 7.68	78	523	500

Table 6.4: DC-measurements for the 60 μm patterns [Ω]

# Measurements	Mean value [Ω]	Remarks
12 (out of 20)	0.013 $\pm$ 0.004	done @ 100mA

Table 6.5: 4PT-measurements for the 40 μm patterns [Ω]

DC	# Measurements	Mean Value [Ω]	# Connections	# UTCP Squares	# chip Squares
8-7	4 (out of 5)	24.58 ± 1.08	112	652	560
8-5	2 (out of 5)	47.80 ± 1.70	226	558	1140
8-3	1 (out of 5)	68.60	338	706	1700
8-1	1 (out of 5)	91.10	452	612	2280
7-6	5 (out of 5)	2.32 ± 0.44	0	746	0
5-4	5 (out of 5)	1.86 ± 0.38	0	504	0
3-2	5 (out of 5)	2.60 ± 0.78	0	746	0
8-7	4 (out of 5)	24.65 ± 1.11	112	625	560
6-5	2 (out of 5)	25.25 ± 0.78	114	625	580
4-3	3 (out of 5)	23.93 ± 0.32	112	625	560
2-1	2 (out of 5)	24.75 ± 0.07	114	625	580

Table 6.6: DC-measurements for the 40 μm patterns [Ω]

Similarly as above, results for contact resistance, UTCP metallization resistance and on-chip metallization resistance can be deducted from the numbers in the tables. All this is summarized in Table 6.7.

Pitch patterns	$R_{contact}$	R_{UTCP}	R_{chip}
100 μm	2 mΩ	3 mΩ/□	34 mΩ/□
60 μm	6 mΩ	3 mΩ/□	47 mΩ/□
40 μm	13 mΩ	3 mΩ/□	37 mΩ/□

Table 6.7: Overview of resistances in flat UTCP packaging trials

These results in Table 6.7 seem to be consistent. On the one hand, the resistivity of the UTCP and chip metallization is comparable for the different pitches. This is fortunate, since these values should be independent of the UTCP test design and are only linked to the thickness of the metallization layers. On the other hand, the values obtained for the contact resistances of the different pitches, can be recalculated for comparison: while the 40 μm pitch contacts consist of single 12.5 μm plated vias, the 60 μm pitch contacts consist of 4 (a 2-by-2 array) of the same vias, and similarly the 100 μm pitch contacts consist of 9 (a 3-by-3 array) of those vias. Ideally, this would mean that the 4 (resp. 9) parallel vias of the 60 (resp. 100) μm pitch contacts, should show 4 times (resp. 9 times) less resistance than the single vias.

In terms of current loading capacity, one daisy chain was tested, and it was found that when 180 mA (corresponding to more than 2W) was fed through the daisy chain of a UTCP, still attached to its carrier, the soldermask started burning. Some pictures are shown in Figure 6.14. This thermal "treatment" caused the chip

to crack (perhaps due to thermally induced tensions between chip and soldermask). Worth mentioning is that all this seems not to have had any repercussions on the electrical functioning of the device, although it should be said that since this is only a test chip, the same might not be true for a functional chip with active n and p doped areas.

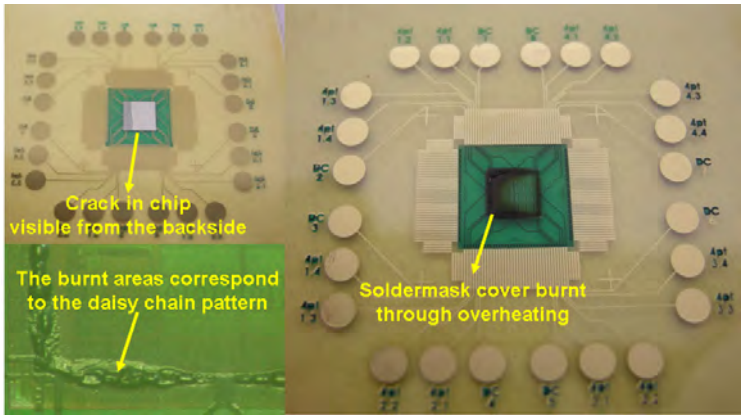

Figure 6.14: Burning the soldermask by electrically overheating through the daisy chain did not affect the electrical performance

6.6 Flat UTCP Assembly

The previous UTCP's layout, used for the fabrication tests as described and characterized in respectively Sections 6.4 and 6.5, has also been designed to test the possibilities of assembling UTCPs onto patterned flexible substrates. The assembly could be carried out with Anisotropic Conductive Film (ACF) bonding, offering the advantages of fine-pitch connection possibilities and low-temperature curing, often a requirement for flexible display backplanes. Furthermore, the UTCP has been designed with contacts at the four sides of the (square) package, where a matching thermode allows for all four sides to be bonded at the same time.

The described work relates to research that has been carried out, assembling UTCPs onto flexible substrates in the frame of interconnecting drivers to displays. The assembly of flexible packages on flexible substrates has already been described extensively in this thesis: e.g. in Chapters 3 and 4 where drivers packaged as TCP (Tape Carrier Package) or COF (Chip-On-Flex) have been bonded to displays, both rigid and flexible, but the driving chips in these packages are thick and rigid and hamper the flexibility of the display significantly. On the other hand, thinned-down chips can and have also been embedded directly in rigid and

flexible displays, e.g. as integrated drivers, described in Chapter 5, but the UTCP approach, allows to fully test the driver chip without having to manufacture the active-matrix of the display backplane at the same time, meaning that if the driver is not functioning properly it can be rejected without losing the whole backplane. The technology thus combines the benefits of a TCP/COF package with the benefits of integrating the drivers.

6.6.1 Test Setup and Design

Test chips from IMEC were packaged as UTCP for processing trials for the UTCP technology, described extensively in Section 6.4. The layout for the metal layer of this UTCP was designed with test pads for testing the interconnection to the chip inside the UTCP, as well as output contacts for assembling this UTCP onto another substrate. This also demonstrates the possibility of the UTCP technology of testing the die within before it is assembled. The general layout of the thus described UTCP is illustrated in Figure 6.15.

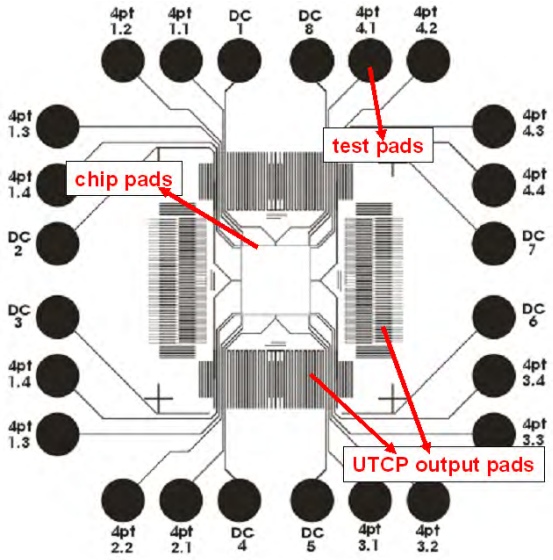

Figure 6.15: General layout of the UTCP design

The same principle was used in designs for different dimensions, given in Table 6.8, and corresponding patterns were designed for the substrates on which the UTCPs had to be assembled.

Chip pitch [μm]	Output pitch [μm]	Pad width [μm]	# output pads
100	250	150	4x36=144
60	150/100 (2x200 staggered)	80/90	2x57+2x(2x43)=286
40	100	50	4x85=340

Table 6.8: Details of designed UTCP dimensions

To summarize, the test design is illustrated in Figure 6.16: the UTCP is visible in the middle (with the ultra-thin chip embedded in the centre area of the package), the bonding area is where the chip's output contacts are aligned to the contacts patterned on the display substrate, and the test points test the interconnection to the package (rectangular pads) or to the chip (round pads). The bonding area matches the thermode and defines a 2.5 mm wide square perimeter around the embedded chip.

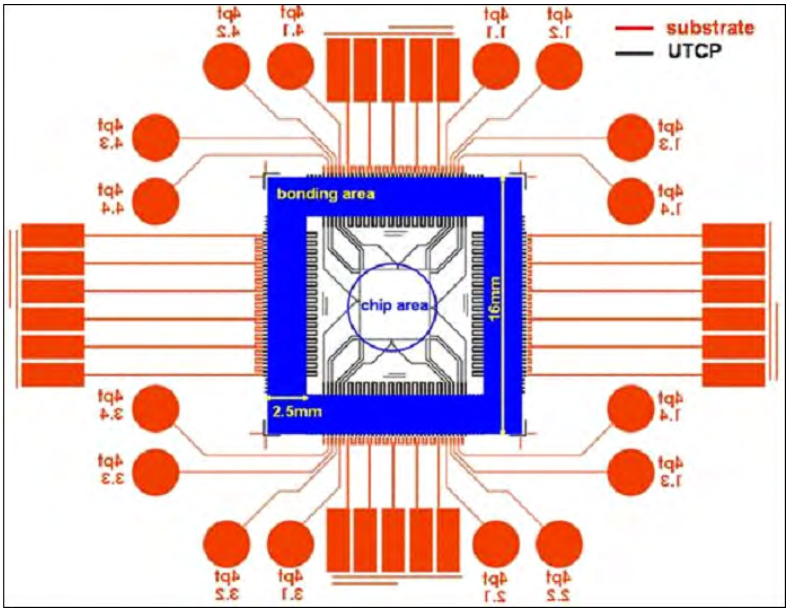

Figure 6.16: General layout of the UTCP assembly design

6.6.2 UTCP Assembly Process

Assembly of the UTCPs is done through bonding with ACF. The temperature of the thermode was programmed to start at 50°C, then ramp up with 20°C/s to 200°C,

and hold this for 30s. Then the electrical heating is stopped, and the thermode is lifted when the temperature has dropped below 100°C.

The thermode is calibrated beforehand to the substrate table with pressure-sensitive paper to prevent uneven bonding. During bonding, the pressure is set at 3.5 bar, and a silicone interposer is used to redistribute any remaining (small) pressure differences that may be due to surface roughness of the surfaces to be bonded. All this is similar to the assemblies with ACF already described in several previous sections.

A notable difference with earlier bonding trials, is that all peripheral contacts are bonded at the same time, requiring a specifically designed thermode. A dummy UTCP, without chip embedded, together with the thermode, that fits the bond contacts, is shown in Figure 6.17.

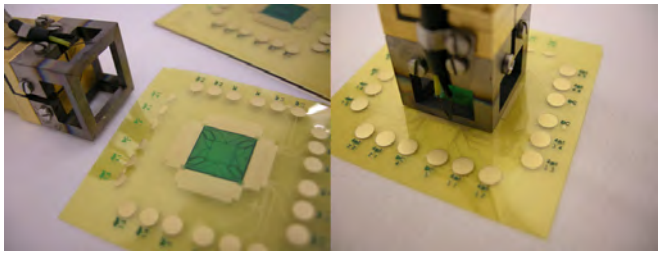

Figure 6.17: The thermode for UTCP assembly matches the outputs' area of the UTCP; the round test pads on the package can be used for testing the embedded chip after packaging and are cut off prior to bonding

6.6.3 PI display substrates

The first set of bonding trials was done on PI substrates. PI is a high quality plastic that can withstand relatively high temperatures (350°C and above, and can therefore even be used in soldering processes, unlike most other plastics). PI is used in the fabrication of flexible displays, e.g. as barrier layer on stainless steel, or even directly as display substrate, e.g. in Philips' EPLAR process.

The PI substrates used are flex foils commercially available as Upilex-25s from UBE Industries. They are 25 μm thick and are already coated with a 9 μm Cu layer. This Cu layer is patterned with the substrate layout by spray-etching, and is subsequently plated with a NiAu finish (to protect the Cu from oxidation).

There were some difficulties etching the staggered outputs, where the very thin line width of 30 μm was either overetched or underetched[5]. This is shown

[5] and subsequently overplated

in Figure 6.18. Patterns with corresponding (and therefore similar) feature sizes were fabricated on the UTCPs, but this was less problematic (20 μm features are possible on the UTCP), as the metallization there is pattern-plated instead of spray-etched.

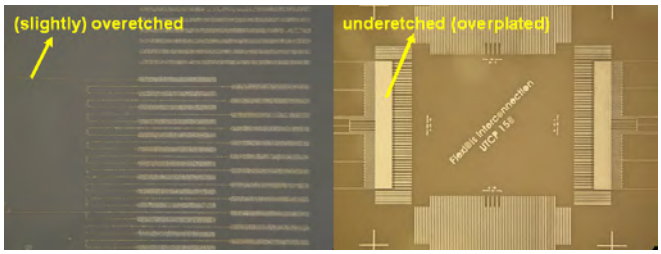

Figure 6.18: Issues etching the thin staggered output patterns on the PI substrates: either overetching (left) or underetching (right) was observed

Optically, a resulting assembly is shown in Figure 6.19. Inspection teaches that alignment is sufficient down to the smallest fabricated patterns at 100 μm pitch.

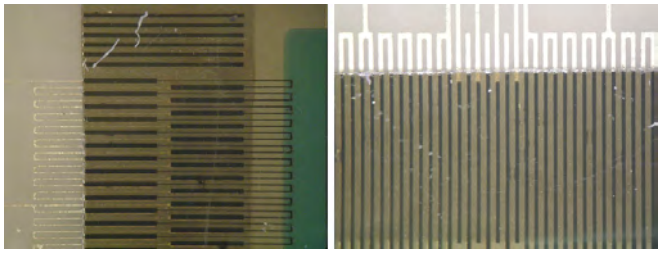

Figure 6.19: Assembly close-up with successful alignment for the smallest pitches

Electrical tests consist of daisy chain segments, formed by UTCP and substrate, that can be measured after assembly. The principle is shown in Figures 6.20 and 6.21. If the assembly is successful, one long daisy chain is measurable at each of the four sides of the assembled UTCP.

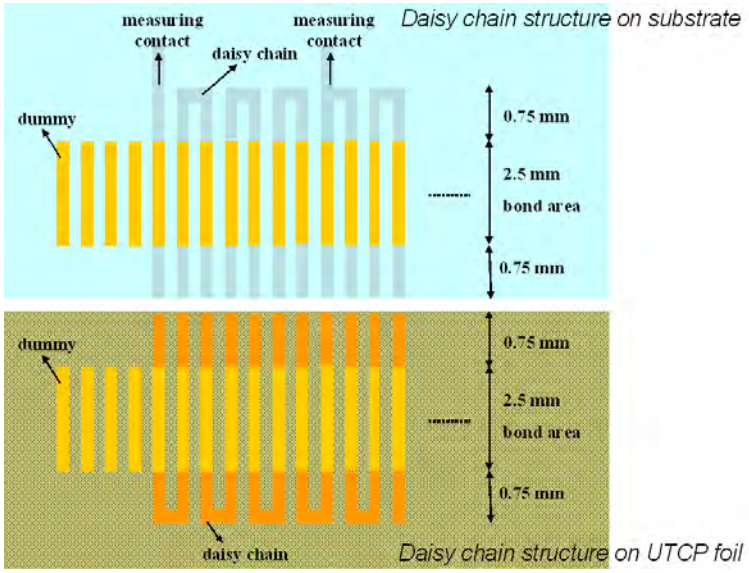

Figure 6.20: Matching designs for UTCP and substrates

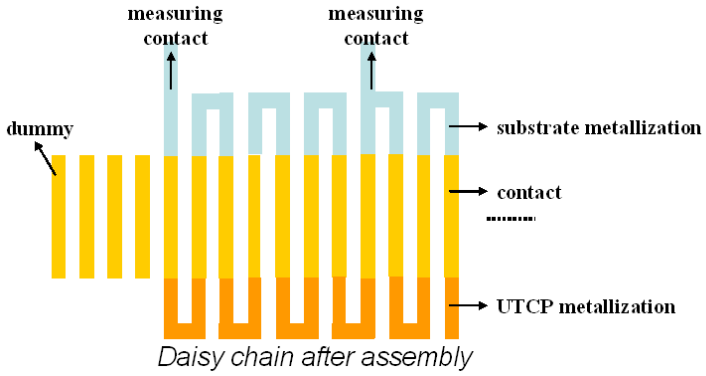

Figure 6.21: A daisy chain is formed between UTCP and substrate after assembly

A summary of the resulting electrical measurements is listed in Table 6.9. For each interconnection pitch, segments of the daisy chain with different length and number of contacts are available for measuring. In Table 6.9, each time the measured resistance value for these daisy chain segments is given, as well as the characteristics (number of contacts, number of squares on substrate and on UTCP) and how many of these segments have been measured.

The theoretical value at the right end of Table 6.9 is a coarse approximation

based on the (approximative) values of the square resistances of the substrate and UTCP metallization, in this case both 3 mΩ/□. The contact resistance is typically expected in the range of the number of squares of the contact area multiplied by the square resistance of the lowest resistive metallization at either side of the contact. In this case, this amounts to respectively 0.05, 0.094 and 0.15 Ω for the 250, 150 and 100 μm pitch interconnect patterns.

Pitch [μm]	# measurements	Value [Ω]	# contacts	# □ on substrate	# □ on UTCP	Theoretical Value [Ω]
250	16	0.7 ± 0	6	86	33	0.66
	12	1.13 ± 0.12	8	191	181	1.52
	8	1 ± 0.11	6	181	34	0.95
150	4	2.14 ± 0.62	10	198	98	1.83
	4	1.86 ± 0.59	8	179	79	1.53
	2	0.8 ± 0	2	122	30	0.64
100	7	9.27 ± 2.80	16	326	244	4.11
	7	9.2 ± 2.97	16	320	244	4.09
	4	2.08 ± 0.13	2	180	38	0.95

Table 6.9: Resulting electrical measurements of UTCP assembly on PI substrates (□ is used as short alternative for square)

Inconsistencies between the theoretical values and the measurements are most likely due to the approximations used for calculating the theoretical values. The variation in the measured values can be attributed to (minor) misalignment, and is in accordance with the observation that the relative variation increases as the interconnect pitch gets smaller, making aligning somewhat more difficult.

6.6.4 PES display substrates

Another set of bonding trials was done on PES substrates. This is a more transparent plastic than PI, but at the same time of a significantly lower quality, in the sense that it cannot withstand such high temperatures, and is less chemically resistant (e.g. against acetone).

The substrates were supplied by Sheldahl, are 150 μm thick and have a sputtered layer of 115 nm indium-tin-oxide (ITO) on top[6]. ITO is transparent and sufficiently electrically conductive, so that it is commonly used as frontplane electrode for displays. One important disadvantage for flexible applications is that it tends to crack rather easily when stressed. This is illustrated in Figure 6.22.

[6]they are in fact the same ones as were used in Section 4.4, for the fabrication of PDLC displays

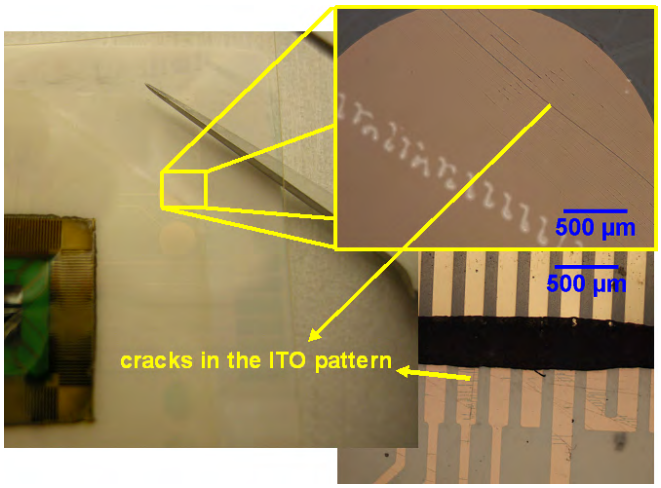

Figure 6.22: ITO cracking is a problem that can already occur during release of the PES substrate from the carrier

The issue of etching the small features as encountered with the PI/Cu substrates, was not such a problem with the PES/ITO substrates. The reason for this is that the ITO is deposited as thin film (115 nm), as opposed to the thick-film Cu (9 m).

Figure 6.23 shows some pictures of the optical inspection of assembled UTCPs on PET.

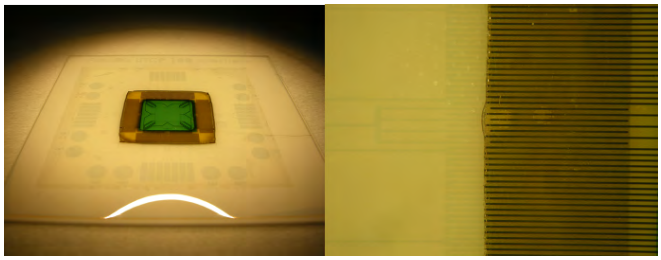

Figure 6.23: A UTCP assembled onto a patterned PES substrate

A summary of the electrical measurements is listed in Table 6.10, built up in the same way as Table 6.9. Again, the theoretical value is a coarse approximation based on the (approximative) values of the square resistances of the substrate and UTCP metallization, in this case respectively 50 Ω/□ and 3 mΩ/□. In the same line-of-thought as with the PI/Cu substrates, the contact resistance is typically defined by the lowest resistive metallization, and therefore depends mainly on the Cu

metallization of the UTCP, resulting in similar values for the contact resistance as in Section 6.6.3 above. It is at once clear that the measured resistance is mainly due to the high ITO resistivity.

Pitch [μm]	# measurements	Value [kΩ]	# contacts	# $\square$ on substrate	# $\square$ on UTCP	Theoretical Value [kΩ]
250	7	4.12 ± 0.48	6	86	33	4.30
	4	9.43 ± 0.79	8	191	181	9.55
	3	8.48 ± 0.22	6	181	34	9.05
150	4	9.53 ± 1.95	10	198	98	9.90
	4	8.65 ± 1.82	8	179	79	8.95
	2	5.49 ± 0.09	2	122	30	6.10
100	7	20.9 ± 5.49	16	326	244	16.3
	7	21.5 ± 5.80	16	320	244	16.0
	4	8.43 ± 0.30	2	180	38	9.00

Table 6.10: Resulting electrical measurements of UTCP assembly on PES substrates ($\square$ is used as short alternative for square)

The same remarks can be made regarding variations as above (misalignment). Furthermore, it should be mentioned that variations are also partly due to the variations in ITO resistance itself, due to non-uniformity and partial cracking.

As an illustration of the bonding process and the final result, some pictures are shown in Figures 6.24 and 6.25.

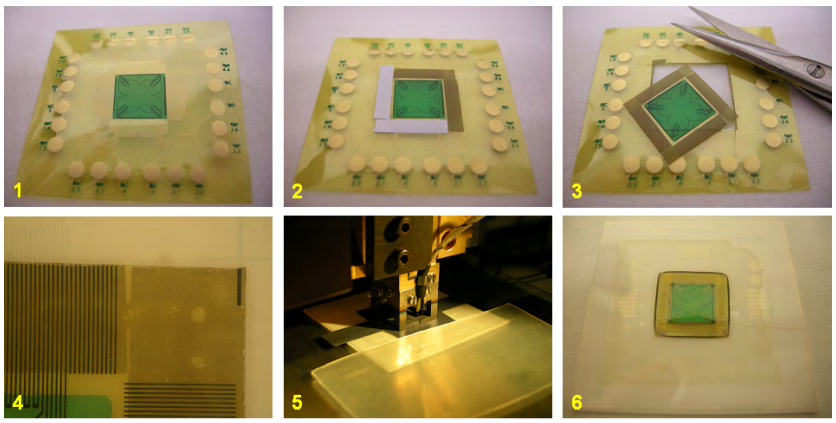

Figure 6.24: The assembly process in pictures

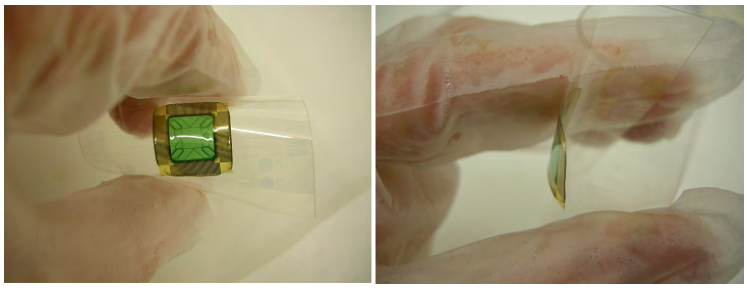

Figure 6.25: The resulting assembly, illustrating its bendability

6.7 Evolution of flat UTCP Technology

References: [95], [96], [97]

6.7.1 Optimizations

The fabrication, as described above, evidently involves a lot of processing steps, each of which has its own parameters and sensitivities. This implies that a lot of work can be done on optimizing the processes individually as well as integrating them in an optimal way.

As a general remark, the substrate material PI absorbs significant amounts of moisture, called swelling, when left out in the open (or in the cleanroom), and this can affect certain process steps. To avoid these effects, the substrates should always be treated in an oven before processing to dry them completely (or as good as completely). A few hours at 200°C is usually sufficient.

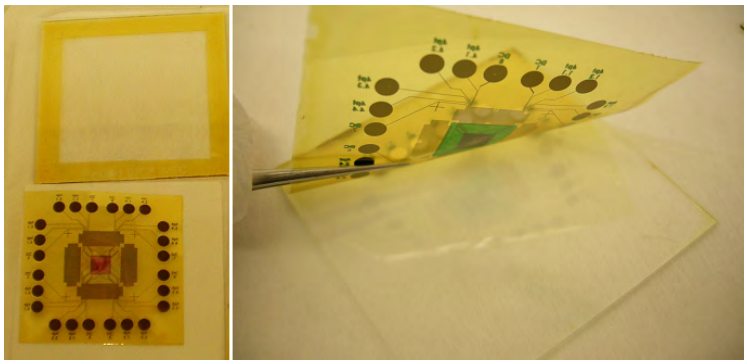

Figure 6.26: Optimized UTCP release: formerly by cutting out the middle part (adhesion promotor applied at the sides of the glass carrier, left picture), currently the glass can be reused after release of the UTCP (right picture)

In the original process, adhesion promotor was used at the sides of the glass carrier to prevent foreseeable curling of the substrate (due to CTE, Coefficient of Thermal Expansion, mismatch). At the end of the process, the middle area was then cut out for release. However, it was found that, in this case, the adhesion promotor is not necessary and the processing can be done on the bare glass carrier without risking a premature release. Moreover, this means the glass carrier is no longer wasted since it might be re-usable after cleaning. This is illustrated in Figure 6.26.

It is also very important to carefully match the chip to the cavity in the PI, for the mechanical robustness (it is preferable in this sense to have smooth layers rather than edges and singularities where stresses are focused), but especially for the metallization afterwards. The matching has to be done both in the lateral dimensions and in thickness. The thickness of the photodefinable layer can be reliably adjusted by changing the spinning parameters. For example spinning at 4000 rpm results in a 26 μm deep cavity, and 4250 rpm corresponds to 24 μm, better suiting the 20-μm-thin chips. The spin speed curve is given in Figure 6.27 and can be used to match cavity depth to chip thickness.

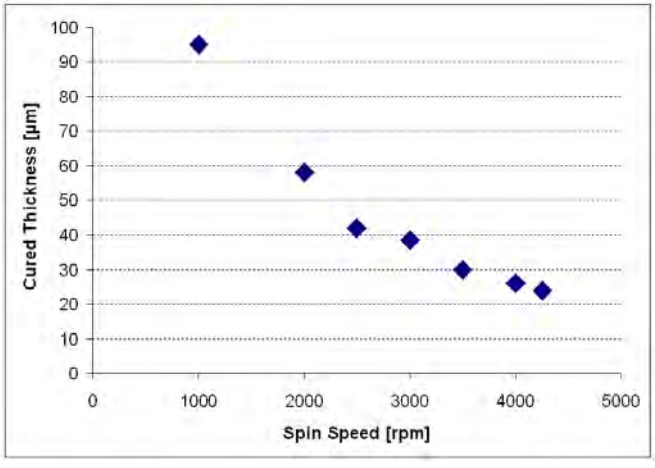

Figure 6.27: Spin speed curve for HD7012: useful for matching chip thickness and cavity depth

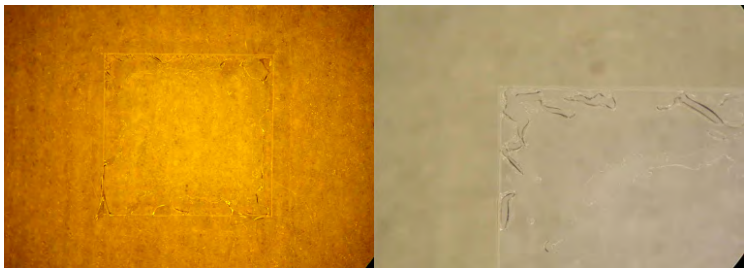

Figure 6.28: Bad results after lithography of PI on a white ceramic background: traces remain at the edges of the cavity (5 mm by 5 mm)

Further on, there were recurring problems with photolithography and development of the photodefinable PI: often traces of PI remained at the edges of the cavity, as illustrated in Figure 6.28. This was found to be introduced during illumination. In some runs, illumination was done with a white ceramic carrier underneath the glass carrier, and since the glass carrier, as well as the base PI layer is transparent, the UV light was reflected on the white background, scattering back partly underneath the mask foil. This could easily be solved by taking care to always illuminate on a black absorbing background.

The placement of the chip has also changed, from using a complex setup involving a mask aligner equipped with a vacuum holding mask, to a more straightforward manual placement with tweezers under the microscope. The latter technique is easier and faster by far, but it should be mentioned that it is less accurate and somewhat more chips get damaged during handling. For future developments, it is very much desirable to use better suited pick-and-place equipment for this step, to improve accuracy and reproducibility, and reduce the risk on breakage due to handling.

A lot of problems occur at the chip-cavity interface, where any gap causes difficulties for the metallization that has to bridge this gap. This is shown in Figure 6.29. Ideally the chip and the chip cavity should match perfectly, but in reality this is hard to achieve. The problem is introduced during lithography and developing of a photoresist layer on a non-flat surface, because the layer will not have the same thickness everywhere: it will be significantly thicker near the edges of the gap, as is illustrated in Figure 6.29. Figures 6.30, 6.31 and 6.32 respectively show some pictures of the problematic areas, evidently more common in the finer pitch patterns, and some pictures of good results for the somewhat coarser pitch patterns.

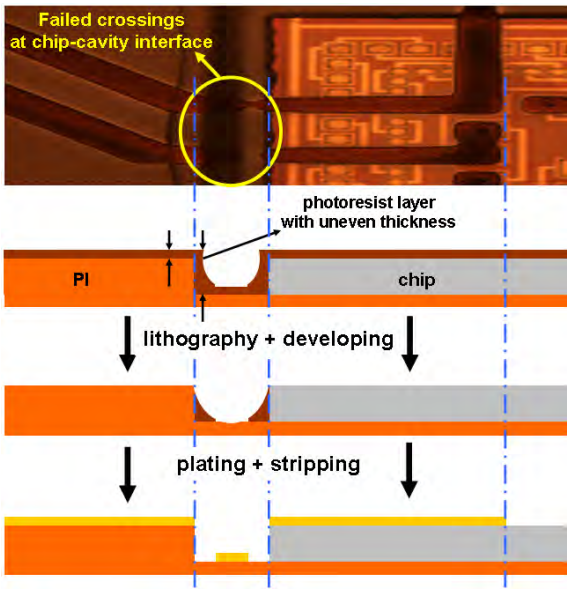

Figure 6.29: Bridging the gap at the chip-cavity interface is a challenge that needs to be addressed

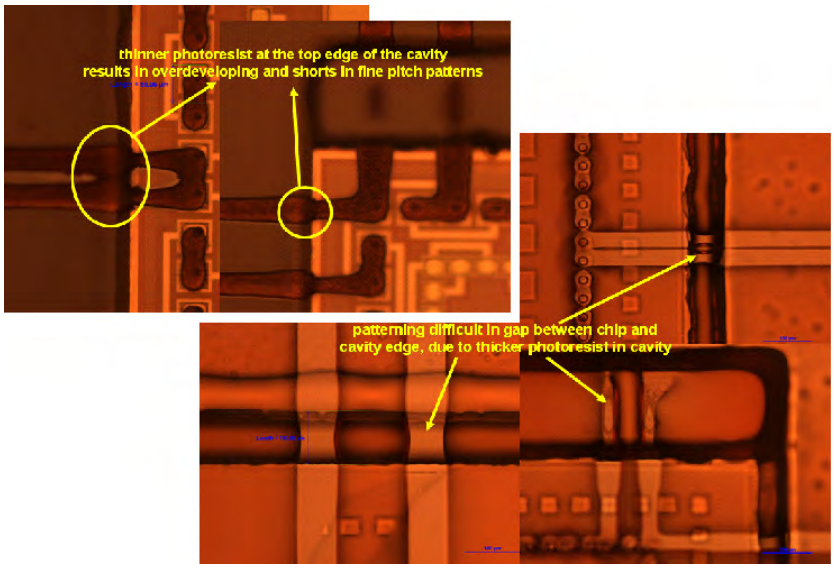

Figure 6.30: Problems arising in lithographic steps due to height differences between chip and PI layers

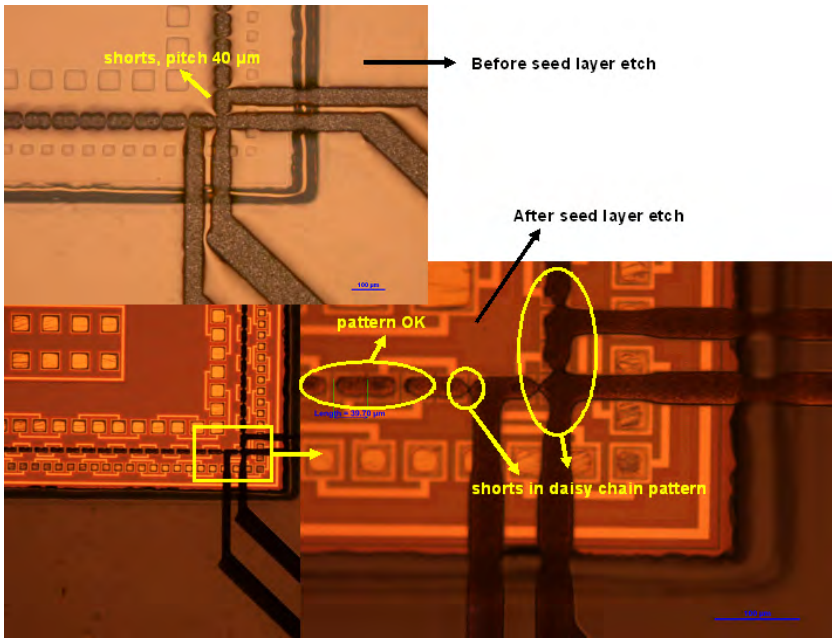

Figure 6.31: Fine pitch limitations in pattern definition (40 µm pitch tracks)

Figure 6.32: Good results with adequate gap crossings at a coarser pitch of 100 µm

Problems with insufficiently developed tracks in the gap interface can be largely countered by increasing illumination and developing time. Of course, this also

affects the areas that are not supposed to be illuminated, resulting in broader tracks and possibly causing short-circuits between neighbouring tracks. Therefore, this phenomenon at the cavity interface results in limitations to achievable minimum track widths and spacing at the gap crossing. It seems that for the described technology, 40 μm can be considered the lower limit for the achievable pitch[7], as at this point, it becomes a problem, even when optimizing illumination and developing times.

Of course, a number of possible solutions could be conceived to lower this limit, or even eliminate this phenomenon, by altering the described flat UTCP technology in more or less drastic ways. A few suggestions:

- The buildup could be reversed and be made completely flat by placing the chip face-down, then depositing a thick PI top layer and subsequently backlapping this PI to the same thickness as the base layer. After this, the package has to be released from the glass, reversed and re-attached to a temporary carrier, so the active side is free for processing. Vias cab then be drilled, followed by similar metallization steps. This way, there is no cavity or interface to cross. This is arguably a solution, because the problem might very well persist in the via holes, although probably in a diminished form, if the base PI layer is not too thick.

- Less drastically, the metallization could be done using only thin film, so with only the seed layer. This way, pattern-plating is eliminated, and a thin photoresist layer is sufficient for etching. Much finer features could be achieved thus, although the interconnection might not be as reliable, considering that the vias have not been plated, and the conductivity might suffer.

One more optimization was introduced in the laser drilling process, where vias are drilled through the top PI layer to the chips' contacts. As the via holes drilled with the YAG laser are very small, 12 μm on average, there is room for several vias on the larger contacts of the test chips. Therefore, this could be optimized by introducing an array of 2 by 2, and 3 by 3 vias for the 60-μm-pitch and 100-μm-pitch contacts respectively. This is illustrated by the pictures in Figure 6.33, and ensures more contacting possibilities for the following (sputtered and plated) metallization layer.

[7] corresponding to 30 μm track width and 10 μm spacing

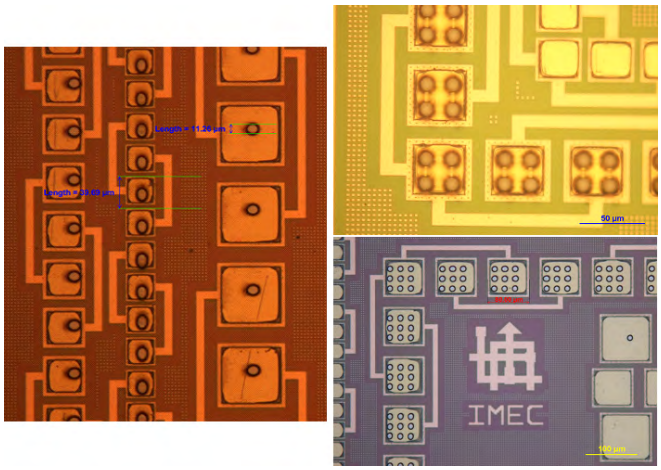

Figure 6.33: Laser drilled via holes in the top PI layer: from a single via for each contact (left), to a number of parallel vias, 2 by 2 and 3 by 3, to reduce contact resistance (right)

Finally, electroplating, used to define the metal interconnection layer, was optimized from a time-is-money point-of-view: the plating time has been reduced to 2 minutes by increasing the plating current (the electroplated surface always being 3 cm^2). The figures are to be found in Table 6.11. The applied charge here equals the product of plating time and current and should be somewhat consistently linear with regards to the plated thickness.

Time [min]	Plating Current [mA]	Applied Charge [C]	Plated Thickness [μm]
15	120	108	5.5
20	120	144	7
25	120	180	8.5
10	250	150	9
5	500	150	8.5
3	750	135	8
2	1000	120	7
2	1250	150	8.5

Table 6.11: Electroplating trials for the metallization layer

6.7.2 Actual Functional Driver Chips

As a next step, first trials have been done to embed functional chips with the developed UTCP technology.

6.7.2.1 Preparation of Functional Chips

The functional chips used for embedding trials were supplied by ST Microelectronics (STM). It involves the eDrive021, a driver chip for e-paper applications, developed within FlexiDis for Plastic Logic. The dies measure 22.55 mm by 1.66 mm and have 320 outputs for dot-matrix display driving. All pads measure 53 μm by 71 μm and the finest pitch, at the output side, is 68 μm. Some pictures are shown in Figure 6.34.

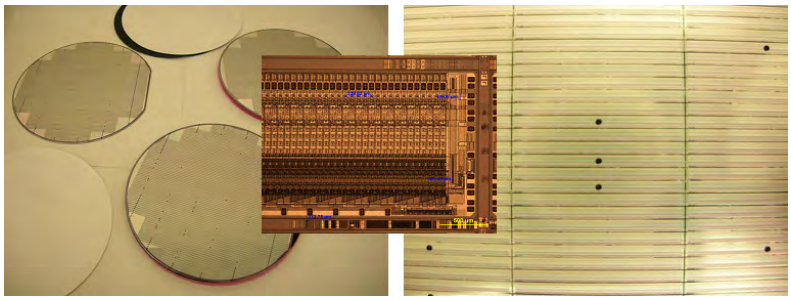

Figure 6.34: Wafers of the eDrive021 as supplied by ST: two were tested, one wasn't (the dots mark the faulty dies)

The driver chips, as said above, were delivered on a wafer (actually 3 wafers), and were electroplated with gold to 20 μm bumps. Before they can be embedded with the flat UTCP technology, these wafers still have to be fly-cut (a sort of polishing to shorten the bumps), diced and thinned. This flycutting is needed to shorten the bumps, to prevent too much of the bumps sticking out of the package after having applied the top PI layer, approximately 5 μm thick. The asked specifications as well as the results are shown in the Figure 6.35. The fly-cutting was carried out by the DISCO corporation, a company manufacturing this type of equipment[8].

[8] amongst others

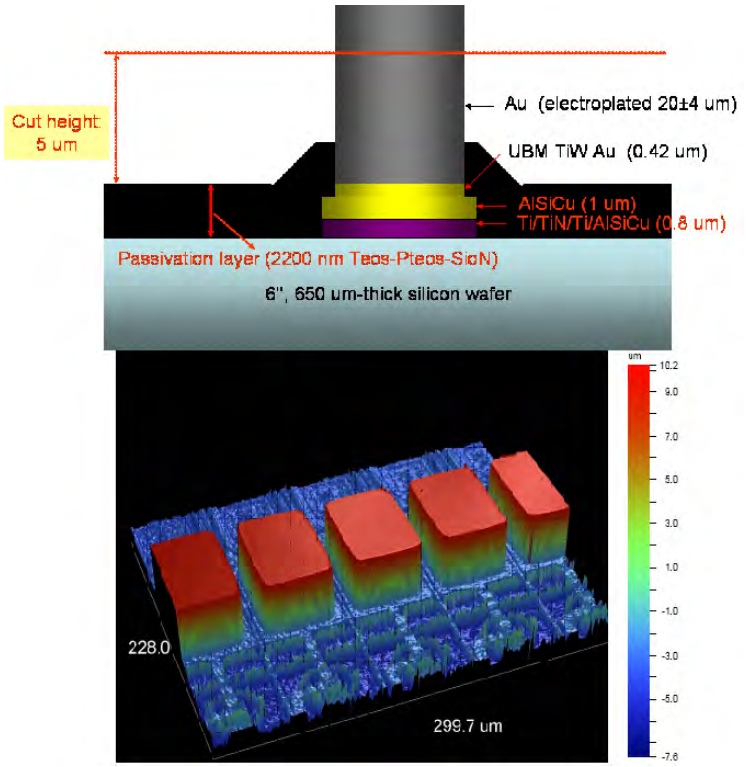

Figure 6.35: Specifications and results of flycutting the STM wafers: instead of the asked 5 µm, the bumps were fly-cut to approximately 12 µm

After fly-cutting one wafer was diced, so that the chips could be individually thinned. These processes are illustrated in the Figures 6.36 through 6.40, as this gives a better idea of what has been done than just a textual explanation.

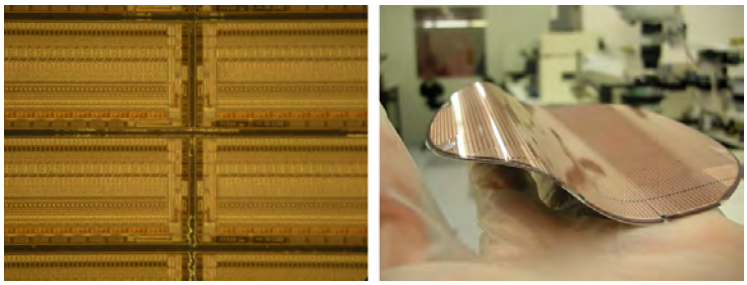

Figure 6.36: A diced wafer (with the sawing lanes visible left) gives a false impression of flexibility (right)

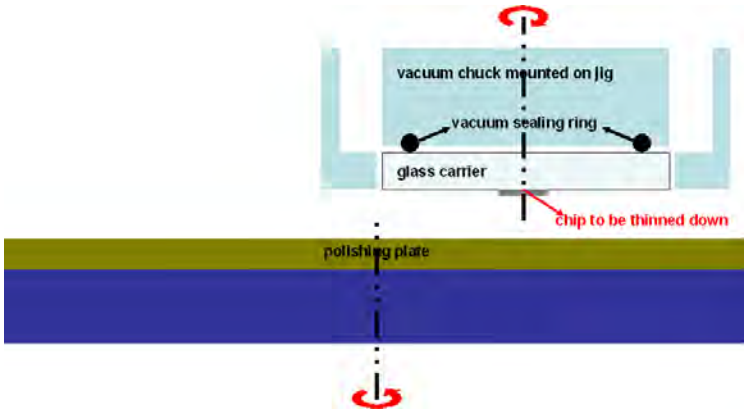

Figure 6.37: A cross-section view of the chip thinning process, based on lapping and polishing

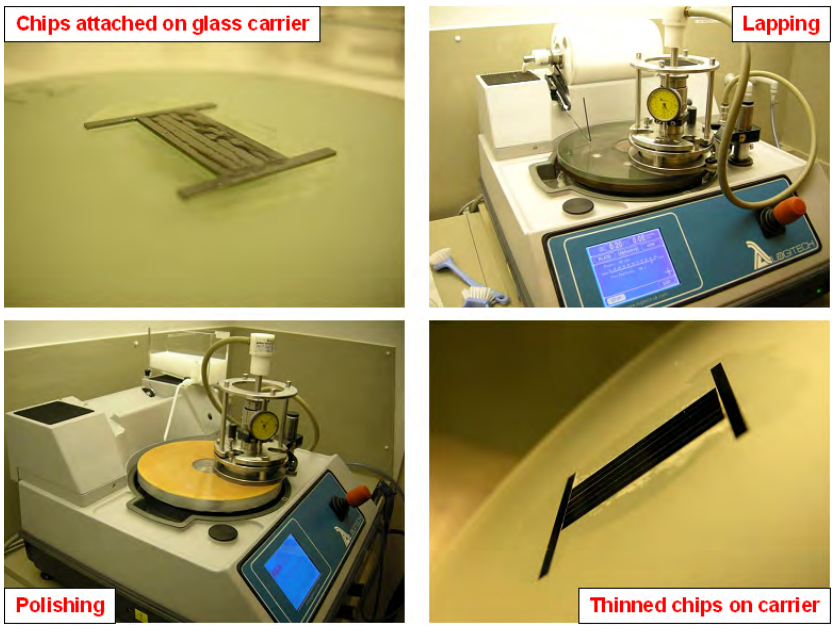

Figure 6.38: Illustration of the process of thinning the dies: here 8 dies are thinned at the same time (of which the outer 4 are dummies)

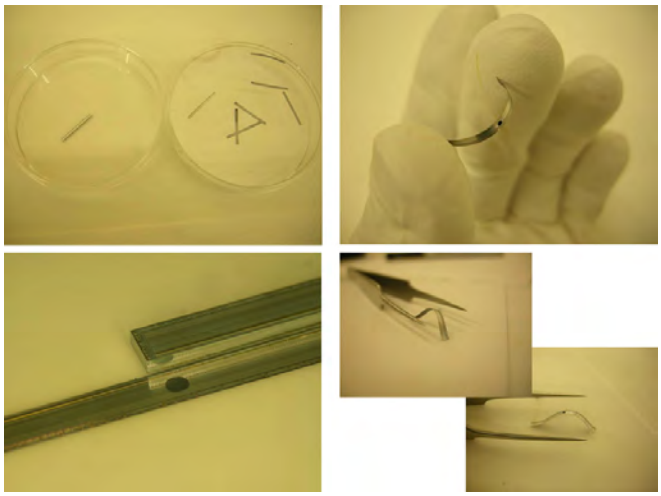

Figure 6.39: Results of the thinning process: note the flexibility of the thin dies

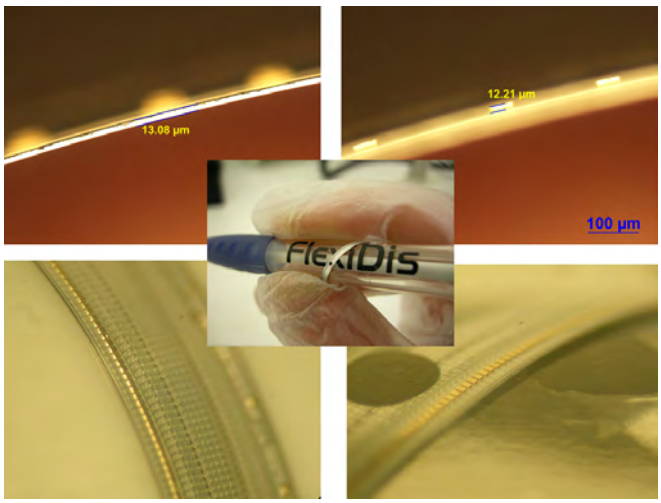

Figure 6.40: Some more results of the fly-cutting and thinning process: chip thinned down to 13 µm, chip bumps are 12 µm

6.7.2.2 Setup and Design

For the package itself, a UTCP design has been made, with a cavity to fit the chip, a metallization to wire out the inputs and outputs of the driver chip, and a soldermask to cover and protect the chip area afterwards. These designs are given in Figure 6.41.

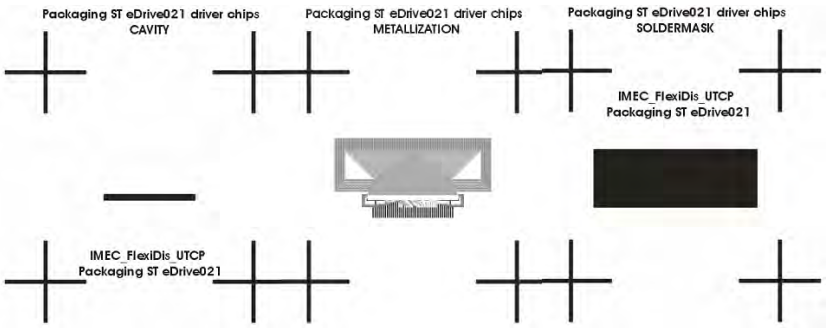

Figure 6.41: Designed masks for the UTCP to match the eDrive021 chip

The UTCP is designed with exactly the same outer leads as the TCP designed for the chip by STM. This offers the possibility of testing the functionality of the UTCP by using the same setup as STM uses for its TCPs. The leads have a pitch of 120 μm at the output side (320 contacts), and a pitch of 500 μm at the input side (40 contacts).

6.7.2.3 Fabrication Status

At this point, thin chips are available and substrates with cavities are ready, with the first eDrive021 UTCPs embedded and in the processing pipeline. Some pictures illustrating the status are shown in Figure 6.42.

The fabrication process still has to be optimized very little to accomodate for the differences in chip size and bump dimensions. Next to this, of course the resulting packages still have to be characterized, and compared with the basic functionality of the chip. This will evidently involve the assistance of STM.

Figure 6.42: First UTCP trials with functional driver chips embedded

6.7.3 Multiple Chip Embedding

Instead of fabricating a separate flexible package for chips, the UTCP technology could also be used for directly embedding multiple thinned-down chips in a PI substrate. This could be interesting as it might be an important enabler for industrial mass-production of UTCPs, where several ultra-thin chips could be embedded using large carrier-substrates. Then further processing is done simultaneously on all embedded devices at once, and finally, the substrate can be separated. This is a common technique similarly practiced in e.g. flat panel display fabrication. Another interesting option could be to use the UTCP technology to embed the driver chips directly in the flexible (PI) display substrates. This would also require embedding several driver chips in the same substrate, and it is a very attractive possibility, especially considering the fact that this could be developed to be compatible with the EPLaR technology, where flexible displays are being made on an industrial scale with very thin PI backplanes.

The idea here is to embed several chips in the same PI substrate sandwich. With the feasibility of the technology proven to work at chip bump pitches down to 40 μm, as reported in Section 6.5 above, the alignment possibilities when placing chips needs to be investigated. In this view, the flat UTCP technology is interesting in such a way that it offers the possibility of photolithographically defining all the cavities, wherein the chips are to be placed, at the same time in one masked illumination step. If the chip then adequately matches the dimensions of the cavity, the placement error should be small enough to ensure good alignment between the (in the cavity) placed chips, and the chips can be interconnected by the routing layer on top.

6.7.3.1 Setup and Design

The test has been set up with four chips, again PTCK chips, as described in Section 6.2, to be embedded and interconnected in the same substrate. The chips are placed in cavities in the four corners and the layout is designed to form two daisy chains on each separate chip. Additionally, a daisy chain runs between each two neighbouring chips. The mask designs are shown in Figure 6.43. The trials have been designed for the (coarsest) chip pitches of 100 μm.

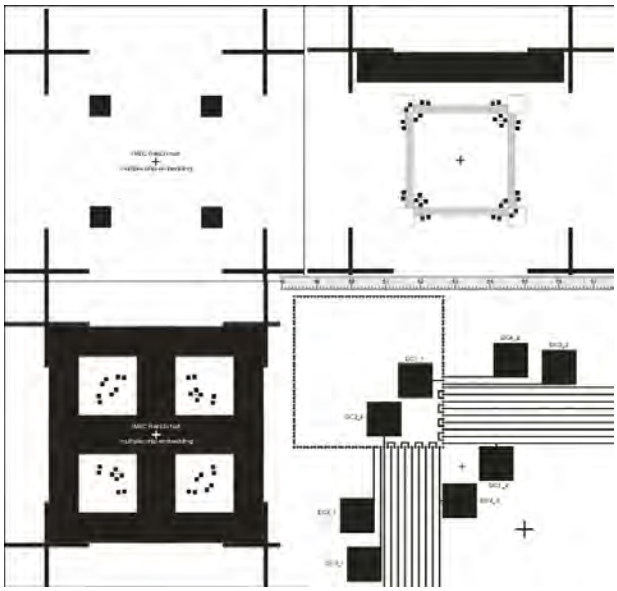

Figure 6.43: Mask layouts for multiple chip embedding: the cavities (upper left), metallization layer (upper right) and soldermask (below left); additionally the design of the upper left corner is shown more in detail (below right)

6.7.3.2 Fabrication

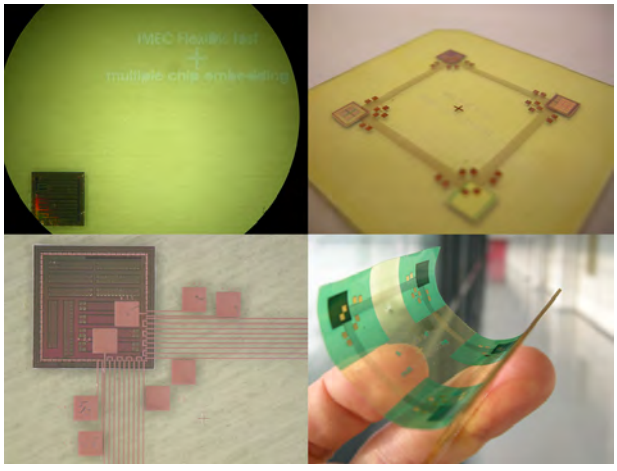

Figure 6.44: Several pictures of the fabricated substrates with embedded chips: a placed chip (top left), 4 embedded chips interconnected by the Cu metallization layer (top right), a close-up (bottom left) and the end result, with soldermask and NiAu finish (bottom right)

The whole fabrication process is evidently very much the same as the one extensively elaborated in Section 6.4. One (minor) difference is the plating area, resulting in different plating parameters. Here, the plating area is approximately 1 cm^2, and plating at 100 mA for 10 minutes gave satisfying results of approximately 6 μm thick Cu. Another difference is of course the location of the chips: in the single chip setup, the chip was placed in the middle, whereas in the case of multiple chips, they are located outside of the centre. This might have implications when spincoating the top PI layer. To minimise the risk on introducing any possible marks degrading the uniformity of the top PI layer during spinning, the PI is applied with a pipette and spread out carefully, making sure all chips are covered before the spinning cycle is initiated.

The first results for embedding multiple chips are promising. A number of problems did arise during processing, such as a substrate table lagging behind during laser drilling, a cavity design not matching the metallization design mask and chip breakage during placement, but all these could be overcome. To give an idea of the result, some pictures of the fabrication can be found in Figure 6.44.

6.7.3.3 Results

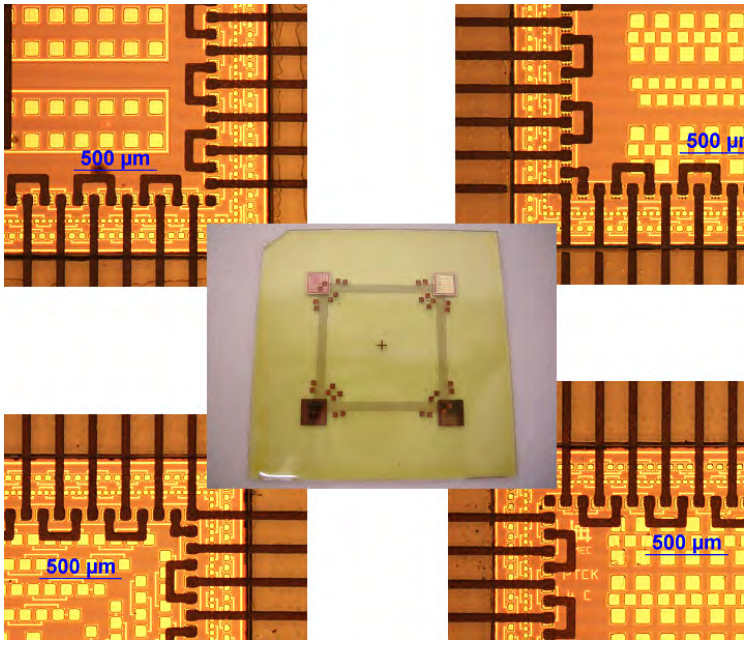

Figure 6.45: Alignment of the chips at the four corners to the metallization is sufficient for interconnection

The result, as clarified in the Figure 6.45, shows that the alignment accuracy of the process is sufficient to interconnect the 100 μm-pitched contacts of the four thin chips embedded in the cavities of the PI substrate. However, closer inspection teaches that, with the described technology, it is difficult to achieve interconnection below 100 μm pitch. The current accuracy is limited by the manual placement of the chips to somewhere in the range of tens of microns: the cavities are necessarily somewhat larger than the chips due to the rounded corners of the cavities, as shown in Figure 6.46. The accuracy might therefore definitely be enhanced with more advanced (read: more accurate) pick-and-place equipment, with current alignment and placement accuracies easily reaching well below 10 μm, even down to submicron accuracies. Another option might be to pre-compensate the rounding of the corners in the cavity design.

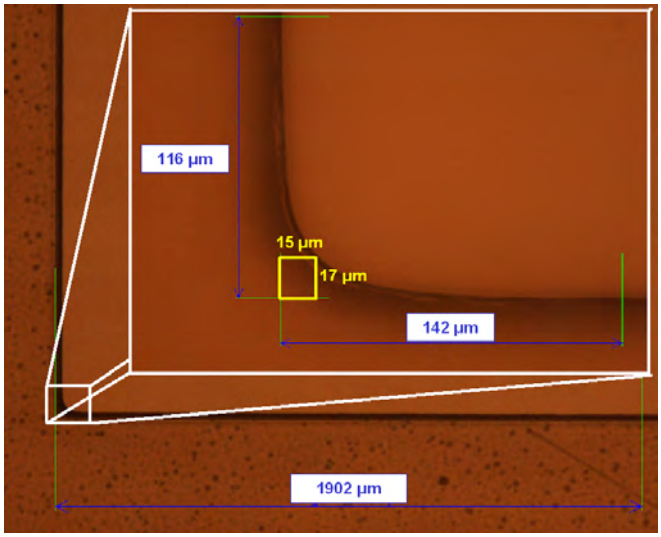

Figure 6.46: Picture of a cavity: zooming in illustrates how the rounded corners require the cavities to be larger than the chip

Electrical measurements also confirm the feasibility of this technology, although so far only one substrate has been completed and measured. The measurements are given in Table 6.12.

Measurement	Value [Ω]	# connections	# □ on UTCP	# □ on substrate	Theoretical Value [Ω]
DC1_1-2	19.1	18	3498	216	17.874
DC1_2-3	X	2	804	48	4.048
DC1_3-4	X	18	3498	216	17.874
DC2_1-2	16.8	18	3498	216	17.874
DC2_2-3	4.2	2	804	48	4.048
DC2_3-4	17	18	3498	216	17.874
DC3_1-2	8.5	18	175	240	8.721
DC4_1-2	53.4	129	95	1632	56.031
DC5_1-2	9	18	175	240	8.721
DC6_1-2	53.9	129	95	1632	56.031
DC7_1-2	8.6	18	175	240	8.721
DC8_1-2	54.3	129	95	1632	56.031
DC9_1-2	8.4	18	175	240	8.721

Table 6.12: Electrical measurements on UTCP with four chips embedded (□ is used as short alternative for square)

Two daisy chain structures, namely DC1_2-3 and DC1_3-4 could not be fully measured due to the fact that a few interconnection tracks were interrupted at the chip cavity interface. This is the same phenomenon as described earlier in Section 6.7.1, that can be attributed to a combination of insufficient illumination and development of the photoresist pattern for pattern plating, and ill-matching chips and cavities.

The verification column in Table 6.12 (Theoretical Value column) shows what the expected value is for the resistance, based on earlier results from the UTCP measurements with 100 μm-pitch contacted thin chips, as given higher in Tables 6.1 and 6.7. These values are 2 mΩ for the contact resistance, 3 mΩ/□ for the resistance of the UTCP's Cu metallization, and 34 mΩ/□ for the resistance of the Al metallization on the chip. Comparing the second and last column in Table 6.12, a good correspondance can be noted between the theoretically expected values and the measured ones.

6.8 Outlook

Here, a technology for embedding thin chips in flexible substrates, the so-called flat UTCP technology, has been intensely investigated and partially developed. It is an interesting technology for integrating drivers in flexible display substrates for several reasons. First of all, it offers the possibility for integrating externally manufactured drivers, so that these can be tested beforehand, eliminating the need

to throw away the whole substrate when one driver is found to be defective. This is the advantage of using a separate driver(package). Furthermore, several driver-chips can be integrated at the same time, with minimalised alignment issues since the cavities for the chips are, all at the same time, photolithographically defined. Finally,the cavities can be matched to the chips' thickness, allowing for a flat substrate. This is especially interesting for flexible display substrates, because the thin film processing in display backpanel manufacturing requires flat surfaces.

Still, a lot remains to be investigated before large-scale manufacturing can be considered. From a technical point-of-view, for example the materials should be characterized extensively, as well as the adhesion between the different layers and their behaviour in different environmental and mechanical conditions. Also the reliability of the complete resulting package is evidently important on the road to commercialisation. Finally, the effect of flexing and electrical stressing on the functional behaviour should be tested as well, depending on the application.

From an economical point-of-view, of course there is the question of scalability of the technology, including its cost, yield, overall efficiency and environmental-friendliness. Next to this, suitable applications and markets have to be defined, and the competitiveness of the technology compared to alternatives should be investigated. As PI is a relatively expensive material, high-end applications should probably be targeted.

Depending on what is encountered in all this, processing steps might have to be adapted or even replaced, for example for high volume throughput, it might be worth investigating the possibilities of reel-to-reel-processing.

Postface

"Now this is not the end. It is not even the beginning of the end. But it is, perhaps, the end of the beginning."

— Sir Winston Churchill (1874 - 1965)

Justification of Gaps in the Experimental Research

As you may have noticed, there is an apparent gap in between the practical research in Chapters 1 through 4 and Chapter 6. As it is, this has been taken care of by incorporating Chapter 5, dealing with this gap in a (mostly) theoretical way: it is explained that flexibility issues in flexible displays are predominantly caused by the rigidity of the interconnected driving electronics. This can be coped with in several ways: either by limiting the flexibility in certain (confined) areas, by diminishing the importance of flexibility and instead focusing on light-weight and ruggedness as main benefits, or by flexibilising the electronics.

However, this explanation is not rigorously substantiated by experiments[9]. To do this, the best option would probably be to set up extensive tests on flexing capabilities and limitations. This was skipped for several reasons: the FlexiDis demonstrators showed ample evidence of display line-outs that could be attributed to damaged column- and row-interconnections, it is a returning issue with assemblies on flexible substrates, and it would take considerable time to prove a point that seems logically acceptable anyway, time that might therefore be better invested in developing an alternative to partially sidestep the problem, in casu the UTCP technology.

In a similar way, reliability measurements were also not incorporated directly in this thesis: for the adhesive assembly technologies used in Chapters 3 and 4, this was postponed to focus on UTCP development; for the UTCP technology, I preferred to put the focus on the fine-pitch capabilities and the multiple chip embedding possibilities.

For the former case, some reliability measurements have been performed two years later. Tests include thermal cycling and hot humidity storage (as mentioned,

[9] although some examples were made and shown

no flexing tests were performed), and were based on standards defined within Carbine, a european project on a "smart CARd dedicated BIstable NEmatic display", by ASK, a contactless smart card manufacturer. The results are given, in short, in Figure 6.47 for thermal cycling and in Figure 6.48 for hot humidity storage. Although the technology qualified for these tests, they also, and expectedly, revealed that the more stringent limitation would come from the side of the mechanical flexibility: even only during release, a lot more defects were introduced than during the whole reliability testing cycles.

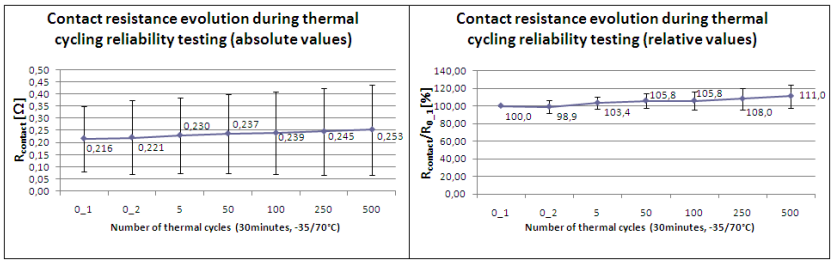

Figure 6.47: Thermal cycling reliability in absolute and relative values

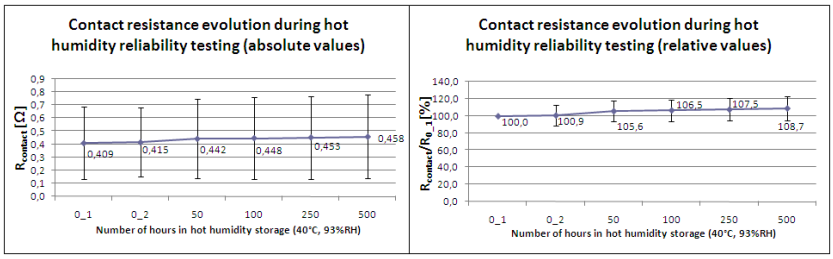

Figure 6.48: Hot humidity storage reliability in absolute and relative values

For the latter (UTCP) case, I should also mention that Wim Christiaens spent a lot of effort investigating the reliability of the original UTCP package, which I would expect to be highly comparable to the flat variant elaborated here. This work will no doubt be published far more extensively in his doctoral thesis[10], entitled "Active and Passive Component Integration in Polyimide Interconnection Substrates", than what I can write down here.

[10] coming soon

Acknowledgment of Lab Contributors

In this doctoral thesis, a lot of research has been done in collaboration with other people, inside as well as outside of the lab. The part that is my own contribution mostly encompasses the practical aspect developing the technology, together with some necessary basic design and characterisation work. For more advanced designs and measurements, especially functional devices, I could rely on the expertise of several co-workers. In this Section I try to give a comprehensive overview of which co-workers were involved and where.

Starting from Chapter 1, Figure 1.1 is a disassembly of my own laptop at home. It still functioned after re-assembly[11]. The microdisplay on the right in Figure 1.15, is a result achieved as a joint work at the lab well before my time, and the examples of driver chips in Figure 1.26 were photographs I made of devices supplied by partners from several projects. The rest of the chapter, including all other figures, is a literature study, where I have indicated the used references at the beginning of each section.

In Chapter 2, Figures 2.1, 2.2 and 2.3 show work done within Thomas De Prycker's master thesis, which was supervised by myself and Fabrice Axisa; part of the work in producing the stretchable version was done by Frederick Bossuyt. Figure 2.4 shows an assembled PCB that was designed by San Lam as part of his doctoral research. Trials with fine-line stencilprinting were coordinated by myself in the framework of FlexiDis: stencils and SEM pictures in Figures 2.9 and 2.10 were supplied by MicroStencil Ltd, to whom stencil fabrication was outsourced, and screenprinting was done by Tomáš Podprocký. Further research and reporting were done by myself, as well as the initial trials with inkjetting silver inks with the newly acquired Dimatix printer, Figure 2.21, for the thesis of Barbara Vanlandeghem. The samples shown in Figure 2.23 were given to us by Tom Judge as representative of Precisia, and the examined 5 euro note in Figure 2.24 was entirely mine, but isn't anymore. A visit to the people IGT Testing Systems NV familiarised us with the high speed printing technologies from the graphical industry. Inkjetprinting trials with the etch mask, Figure 2.31 was done together with Tomáš Podprocký. Figures 2.34 and 2.36 show some assembly work by Björn Vandecasteele, the latter one being a wirebonded chip, designed within the doctoral research of Jodie Buyle for testing xDSL driver circuitry. Figures 2.40 and 2.41 illustrate adhesive assembly possibilities at the lab, and were made by Björn Vandecasteele. Figures 2.42, 2.43 and 2.46 gives an impression of the bonding equipment and principles I used in Chapters 3 and 4. Figure 2.44 shows the stud bumps of the earlier mentioned driver chips Mjöllnir, designed by Herbert de Pauw and bumped by IMEC in Leuven.

[11] however approximately half a later year the display started failing (not directly related to my disassembling it, I think)

Interconnection of rigid displays in Chapter 3 begins with some assembly work I did for San Lam, Figures 3.1 and 3.2, to interconnect his developed driving circuitry to a cellphone display, and continues with some display assemblies I dismantled to illustrate the principles: Figures 3.3 and 3.5 of a (somewhat older) cellphone display, and, together with Björn Vandecasteele, Figure 3.6 of a somewhat larger machine display. The next section, 3.2, gives the result of Thomas Vervust's master's thesis, to integrate a commercial display into a wristwatch based on flexible and stretchable technologies. There, I mostly coordinated and developed the technology for interconnecting the display to the assembled flex, Thomas Vervust designed, programmed and characterized the electronics, Steven Van Put was brought in for lasercutting the meander shaped wires out of the flex, and Fabrice Axisa and Eva De Leersnyder supplied the stretchable technology including the embedding process. Bonding experiments and demonstrator bonding for the sensor matrix were carried out by me, with sensor matrix test and demo substrates, and demo test chips provided by Augusto Nascetti, as well as the principle and measurements in Figures 3.20 and 3.27. The last rigid example, the helmet display, was developed within the HeMind project, and within our lab mainly by Herbert De Pauw. He designed and characterized the Mjöllnir driver chip, designed the rerouting PCB and prepared the display substrates. After filling with liquid crystal mixtures, the displays were sent back to our lab and I did the described assembly work supervised by Herbert De Pauw.

Chapter 4 describes mainly technology development for assembly on flexible substrates and was for the most part done by me, assisted by the expertise of Björn Vandecasteele. The first section involves some basic trials for IMEC in Leuven, while the assembly work on PET and stainless steel was carried out within the FlexiDis framework. Here the design of the experiments, the setup and the substrates and chips was my task, as well as the fabrication of the test chips and flex foils. The display substrates and actual TCPs, as well as their experience, were supplied by partners in the program: Plastic Logic, Thomson and CEA-LETI. The final part of this chapter, on PDLC display assembly, is the reporting of the result of Jeroen Goossens' master's thesis, supervised by myself. As with Thomas Vervust's thesis, I mainly developed the technology for contacting the display, as well as fabricating the PDLC display with flexible PES substrates, based on the doctoral thesis of Filip Bruyneel and backed by Dieter Cuypers' experience with PDLC assembly, while Jeroen Goossens designed the display masks and electronics and characterized the resulting displays. Optical measurements were done by Jeroen Goossens supervised by Dieter Cuypers and Herbert De Smet.

As Chapter 5 is mainly a theoretical chapter, elaborating encountered flexibility issues and suggesting possible solutions, not much practical work was involved here. However, a few significant contributions should be mentioned. Firstly, there are the flexible driving electronics that were developed within FlexiDis, a flexible driverboard and an L-shaped foil. These were designed by Lieven Degrendele and assembled by Björn Vandecasteele, based on information and components pro-

vided by IREX Technologies. Secondly, the work that was carried out in our lab for the Hiding Dies project, of which a tiny bit is shown in Figure 5.14, was done by Maarten Cauwe, An Gielen and Bart Reekmans. Thirdly, the proposed original UTCP concept was conceived by Jan Vanfleteren and Wim Christiaens within the SHIFT-consortium, and Figures 5.16, 5.17 and 5.18 show the principle and first results of Wim Christiaens' work.

Finally, Chapter 6 is my contribution to the development of the UTCP technology, namely the flat variant, primarily conceived for flexible display purposes, but also useful for embedding multiple chips in the same substrate. Fortunately, I did not have to start from scratch, but the initial work could be based on the expertise and materials of Wim Christiaens for basic UTCP processing. Furthermore, thinned down test chips were supplied by IMEC in Leuven, and vias were laser drilled by Erwin Bosman and Steven Van Put. Lastly, the functional driver chips were supplied on wafers by ST Microelectronics, were flycut by the DISCO corporation through IMEC in Leuven, and were thinned down, the principle and pictures of which are shown in Figures 6.37 and 6.38, at our lab by Peter Geerinck.

Contributing to the Awakening Field of Flexible Displays

The research that has been conducted within this thesis has been framed largely within the field of flexible display interconnection, currently still an emerging field, with very little products commercially available as yet. Fortunately, the work can be -and has been- based on two solid foundations of knowledge: on the one hand, existing interconnection technologies for rigid displays, as already widely used in flat-panel commercial display fabrication, and on the other hand, technologies for assembly of components on flexible substrates.

Building upon these foundations, the research has first focused on advancing these technologies, by combining the fine-pitch capabilities of ACF bonding, used in rigid display interconnection, with flexible backpanel substrates based on low-cost and low-temperature plastics as PES and PET, with all the associated problems. These investigations resulted in the first innovative contributions that were achieved as part of this doctoral thesis.

After ascertaining the fact that the interconnection area remains the most fragile part of the flexible display, several possibilities have been proposed and discussed to overcome this weakness in the assembly. The most promising technological approach was chosen, where very thin chips can be embedded inside the display substrate itself, and the development of this embedding technology can be considered as the second major contribution of this doctoral thesis to the advancement of flexible display fabrication.

Placing the Results in Perspective

As said, in the previous pages were described several technologies to interconnect driving electronics to displays. These technologies range from standard and existing assembly technologies with rigid displays to newly developed techniques for embedding electronics in flexible displays. The assembly of displays has been elaborated here as an illustration of different interconnection technologies[12], but of course the described interconnection technologies are more widely usable in (micro-)electronics...

The encountered evolution towards flexible displays can be fitted within a more general evolution towards more flexible and even stretchable electronics. Obvious examples are smart cards, intelligent clothing, implantable electronics and so on; all of which are aplications where portability is highly valued. This portability is seemingly defined by several properties, mainly the ruggedness, the compactness, the light-weight, the conformability and the power consumption of the device. Considering that the technologies described and developed within this thesis focus on high-density, low-temperature interconnection using flexible substrates and components, and where embedding is used for increased ruggedness, they might provide significant contributions to the aforementioned evolution. Power consumption has not been addressed, as it is in most cases not affected by the interconnection, but rather by the system design and choice of components, as long as we are able to neglect the high-frequency behaviour, that is. As for power supply, flexible solutions ranging from organic solar cells to flexible batteries are also being investigated, with some promising developments being reported.

In short, most devices would benefit greatly from compacter, lighter, and more rugged electronics, as is already clear when looking at the evolution in computers, cellphones, etc. With electronics being a very competitive market, as always where a lot of money is involved, and even more difficult to predict due to the high-tech nature of the business, new technologies are at the same time critical for innovation and very risky to push through. That is why, in my opinion, (fundamental and applied) research should be carried out permanently so that it can be evaluated and compared to alternatives before it is developed thoroughly, scaled up and commercialized.

Dissemination

The bulk of the research was carried out and has been reported within the European project FlexiDis, and was therefore disseminated in deliverables and reports

[12] the display application was chosen chiefly because it is a well-known device, already available worldwide, and still growing in importance

to the European Commission, as well as in more general newsletters to the general public[13]. Some parts described in this thesis were also done within other European projects, namely HeMind and SHIFT. Next to this contractual research funded by the European Commission (and the participating industrial partners), some of the work was done as subcontractor for Rome's Sapienza University, Dipartimento di Ingegneria Aerospaziale e Astronautica, and another significant amount of knowledge was generated within a few theses over the course of two years.

The public dissemination can therefore be divided into theses, journal articles and conference contributions[14].

Theses

- Wim Christiaens and Jonathan Govaerts. **Biocompatibele, flexibele elektronische schakelingen voor medische toepassingen** (Biocompatible, flexible electronic circuits for medical applications). 2003-2004.
- Thomas De Prycker. **Elastisch verwarmingselement met ingebouwd flexibel display** (Stretchable heater with built-in flexible display"). 2006-2007.
- Jeroen Goossens. **Integratie van een flexibel display in een uitrekbaar polshorloge** (Integration of a flexible display in a stretchable wristwatch). 2007-2008.
- Barbara Vanlandeghem. **High frequency RFID tag coil design: a comparative study on manufacturing processes"**. 2006-2007.
- Thomas Vervust. **Realisation of a flexible and stretchable wristworn display**. 2006-2007.

Articles

- Jonathan Govaerts, Björn Vandecasteele and Jan Vanfleteren. **Interconnecting Drivers to Flexible Displays**. Journal of the Society for Information Display. Vol. 16, Issue 7, pp. 765-775. July 2008.
- Jonathan Govaerts, Wim Christiaens, Erwin Bosman and Jan Vanfleteren. **Fabrication Processes for Embedding Thin Chips in Flat Flexible Substrates**. IEEE Transactions on Advanced Packaging. Accepted for Publication (July 2008).

[13] freely available on the website http://www.flexidis-project.org
[14] next to the public FlexiDis newsletters of course

- Jonathan Govaerts, Erwin Bosman, Wim Christiaens and Jan Vanfleteren. **Fine-Pitch Capabilities of the Flat Ultra-Thin Chip Packaging (UTCP) Technology**. Submitted to IEEE Transactions on Advanced Packaging (September 2008).

Conferences

- Tom Bert, Jan Vanfleteren, Björn Vandecasteele, Stefaan Maeyaert, Jan Doutreloigne, Jonathan Govaerts, Herbert De Smet and André Van Calster. **Advanced Technologies in Fabrication and Interconnection of Flexible Displays and Substrates**. Proceedings of Flexible Displays and Electronics (FDE). June 2005.

- Jonathan Govaerts and Jan Vanfleteren. **Electrical Interconnection by Means of Conductive Adhesives and Inks**. Proceedings of the 6^{th} UGent-FirW Doctoraatssymposium. November 2005.

- Björn Vandecasteele, Jonathan Govaerts and Jan Vanfleteren. **Embedding of thinned chips in plastic substrates**. Proceedings of the 12^{th} Annual SMTA Pan Pacific Microelectronics Symposium. January 2007. 30-35.

- Jonathan Govaerts. **Interconnecting Drivers to Flexible Displays**. IMAPS BeNeLux spring event 2008. April 2008.

- Jonathan Govaerts, Wim Christiaens, Erwin Bosman and Jan Vanfleteren. **Multiple Chip Integration for Flat Flexible Electronics**. Proceedings of the 7^{th} IEEE Conference on Polymers & Adhesives in Microelectronics & Photonics (Polytronic 2008). August 2008.

- Jonathan Govaerts and Jan Vanfleteren. **Assembly of Ultra-Thin Chip Packages (UTCPs) for Enhanced Flexibility of Flexible Displays**. Proceedings of the 2^{nd} Electronics System-Integration Technology Conference (ESTC 2008). September 2008.

- Jonathan Govaerts, Wim Christiaens and Jan Vanfleteren. **Ultra Thin Chip Packaging (UTCP): a Promising Technology for Future Flexible Display Interconnection**. Submitted to Display Week, International Symposium of the Society for Information Display (SID 2009). June 2009.

Thank You... Bedankt...

"It is said that pessimists see difficulties in any opportunity, while optimists see opportunities in any difficulty..."

— Mikhail Gorbachev (1931 - ...)

First of all, assuming you have been reading all the way up to here[15], I thank you for that and hope you did not regret it. If you did come up against any peculiarities, encountered some possible mistakes, or simply feel some important questions remain unanswered[16], please feel free to contact me, and I will try to enlighten you. You deserve some of my time in exchange for the time you sacrificed reading my book.

Research is, in some ways, quite a bit like going out for a beer: as long as you like the choice of beers, are in good company, have sufficient amounts of money available and are having a fruitful discussion going, it's difficult to let go. In this view, the environment makes for a valuable contribution in any person's achievements, which is a roundabout-way of expressing my appreciation for mine. On the one hand, I thoroughly enjoyed the welcoming and friendly atmosphere lingering in the offices and labs of TFCG Microsystems, in the meantime transformed into the Cmst research institute, as well as the available equipment and its availability[17]. On the other hand, I could rely on a comfortable entourage outside of working hours as well.

Regarding work, I enjoyed working, almost as much as idling, with a lot of the people in and around Cmst; I hope I do not wrong anyone because not all are mentioned below. A bit more specifically, and somewhat chronologically, I would like to thank Björn and Jan (Vf) for sharing their experience and knowledge in packaging and interconnection, Herbert (DP) for the chance to widen my ACF bonding experience and a first eye-opening introduction to the practicalities of display assembly, Wim for showing me the initial ropes in UTCP processing, Erwin and Steven for shooting at my delicately-prepared samples, Dieter for the guidance with PDLC assembly, and also (indirectly) for reminding me to thank the taxpayer, Tomáš for screenprinting, but more so for starting up trials with the inkjet

[15] did you?

[16] and I'm sure there are: I have some myself

[17] although it is getting increasingly crowded in the cleanroom

printer, an interesting and versatile piece of equipment[18], Peter (G) for reducing functional chips to next-to-nothing, Lieven for converting and ordering quite a lot of masks, Bart for etching copper and the nice picture on the next page, and Kristof for plating chips as well as flex foils.

More indirectly related to my doctoral research, I want to express my gratitude to André, Jan (Vf), Nadine and Katrien respectively for politically struggling for the survival of TFCG Microsystems / Cmst as a self-supporting research lab, managing the fan-out activities of the flexible and stretchable electronics team, running a tight ship in and around cleanroom world and helping out with messed-up logistics. Next to my own research, my work also consisted in part of supervising a few theses, which I thoroughly enjoyed for their intriguing topics and students: Thomas (V), Thomas (DP), Barbara en Jeroen. Finally, I could not leave out Nina for providing a happy note to our grim 8-person office with ever-thirsty plants and a perpetual humming noise (from my computer notably), and Geert for posing as unfortunate, multiply-injured victim during first-aid training.

Outside of the lab in Zwijnaarde, there are definitely some more people I wish to thank, in particular the people I collaborated with on the FlexiDis project. These include the project management Eliav Haskal, Willemien van der Linden and Roger van Galen, and research partners Seamus Burns and Sharjil Siddique (Plastic Logic), François Templier and Christophe Prat (CEA-LETI). Also, I would also like to mention Akiko Takayama (Hitachi Chemical), who went to great length to supply me with ACF, in a very short amount of time, Augusto Nascetti (Rome University La Sapienza) for providing materials for some interesting trials, Ghent University for providing me with a grant (and IMEC for extending it) and each taxpayer for his selfless contributions to research in general. Finally, I would like to thank the members of my jury, for the time they invested without clear nor direct profit, especially those in the reading commission. I sincerely hope it was worth your time...

Bezijden het werk, en ik geef toe: de grens is bij momenten wat vaag, zowel qua tijd en plaats als mensen, voel ik mij gesteund door een niet te verwaarlozen hoopje naasten. Alhoewel het misschien niet altijd zo rechtstreeks zichtbaar is, hebben zij ongetwijfeld een belangrijke invloed op niet alleen wat ik doe, maar ook waar, wanneer en waarom. Vandaar dat ik deze mensen toch ook minstens enige dank verschuldigd ben. Vooreerst en vooral is er mijn naaste familie: mijn vader en moeder alias papa en mama, die nogal eens voor vanzelfsprekend genomen worden en daarom niet steeds de lof krijgen die ze verdienen, mijn oudste broer en grootste voorbeeld (ahem) Patrick, mijn middelste broer en beste bioloog-steenkapper van Oost-Vlaanderen Christophe, en mijn jongste en tevens luidste broer Thomas die mij voluit gesteund heeft door met plezier zijn belastinggeld in mij te investeren. Daarnaast wil ik ook nog Stijn expliciet bedanken, een voorhistorische vriend en vroege en tevens langste studiegenoot die het in de privé al ver aan het schoppen

[18] although caution is in order (as well as a protective mask) when filling the ink cartridges

is, en tante Lien, voor een rustig onderkomen in drukkere tijden, en nog tal van mensen, voor wie het er wellicht minder toe doet hier vermeld te worden.

Ten slotte, maar niet in het minst, dank u Jodie, voor de enthousiaste muzikale begeleiding, maar vooral: ge zijt met voorsprong het beste resultaat van mijn doctoraat, hoewel ik er het minst over geschreven heb. Ge verdient beter dan wat ik ook maar zou kunnen bedenken...

Yours truly,
Jonathan
January 8^{th}, 2009

"For all that has been, thanks. For all that will be, yes."

— Dag Hammarskjöld (1905 - 1961)

List of Abbreviations

"Better to light a candle than to curse the darkness."

— Chinese proverb

ACA	Anisotropic conductive adhesive
ACF	Anisotropic conductive film
AZO	Aluminum-doped zinc oxide
BCB	Benzocyclobutene
BGA	Ball grid array
Cmst	Centre for microsystems technologies
CNT	Carbon nanotube
CoC	Chip-on-chip
CRT	Cathode ray tube
CSP	Chip-size package
CTE	Coefficient of thermal expansion
CtP	Computer-to-plate
DC	Direct current / Daisy chain
DIP	Dual in-line package
DLP	Digital light processing
DMD	Digital micromirror device
DNA	Deoxyribonucleic acid
dpi	Dots per inch
EL	Electroluminescent
EPLaR	Electronics on plastics by laser-assisted release
FC	Flip-chip
FED	Field emission display
FlexiDis	European FP6-project on flexible displays
FPD	Flat panel display
FR4	Flame-retardant 4, a substrate material
GPS	Global positioning system
HeMind	European FP5-project on helmet-mounted miniature information display systems
IC	Integrated circuit
ICA	Isotropic conductive adhesive
IPS	In-plane switching
ITO	Indium tin oxide

IZO	Zn-doped indium oxide
LCD	Liquid crystal display
LCoS	Liquid crystal on silicon
LED	Light emitting diode
NCA	Non-conductive adhesive
NED	Nano-emissive display
OLED	Organic light-emitting diode
PC	Personal computer
PCB	Printed circuit board
PDLC	Polymer dispersed liquid crystal
PDP	Plasma display panel
PEDOT	Poly(3,4-ethylenedioxythiophene)
PEN	Polyethylene naphthalate
PES	Polyethersulfone
PET	Polyethylene terephtalate
PI	Polyimide
PLCC	Plastic leaded chip carrier
PLL	Plastic Logic Limited
PoP	Package-on-package
ppi	Parts per inch
PTCK	Packaging test chip version K
PTFE	Polytetrafluoroethylene
PVC	Polyvinyl chloride
QFP	Quad flat package
RCP	Redistributed chip package
sccm	Standard cubic centimeters per minute
SED	Surface-conduction electron-emitter display
SHIFT	European FP6-project on smart high-integration flex technologies
SIM	Subscriber identity module
SiP	System-in-package
SO	Small-outline
TAB	Tape automated bonding
TCO	Transparent conductive oxide
TCP	Tape carrier package
TDM	Time division multiplexing
TFCG	Thin film components group
TFD	Thin film diode
TFT	Thin film transistor
TN	Twisted nematic
USA	Ultra-sonic agitation
UTCP	Ultra-thin chip packaging
VA	Vertical alignment
VLSI	Very-large-scale integration
YAG	Yttrium aluminium garnet

References

"Often it's best for the unwise man to sit in silence. His ignorance goes unnoticed until he tells too much. It's the ill fortune of unwise men that they cannot keep silent."

— Odin (Hávamál, 800)

[1] **http://en.wikipedia.org/**, 2008.

[2] **http://www.etymonline.com/**, 2008.

[3] H. Berkwits, **LCD Transition Gains Traction**, ViewSonic Corporation white paper, September 2001.

[4] A. Khan, T. Schneider, E. Montbach, D.J. Davis, N. Miller, D. Marhefka, T. Ernst and J.W. Doane, **Invited Paper: Recent Progress in Color Flexible Reflective Cholesteric Displays**, SID International Symposium, June 2006, pp. 54-56.

[5] I. Underwood, **A different view**, New Electronics (http://www.newelectronics.co.uk/), January 2008.

[6] **http://www.sonystyle.com**, 2008

[7] **http://trappist.elis.ugent.be/ELISgroups/lcd/tutorials/**, 2008.

[8] F. Mugele and J. Baret, **Electrowetting: from basics to applications**, Journal of Physics: Condensed Matter, Vol. 17, July 2005, pp. R705R774.

[9] R. A. Hayes and B. J. Feenstra, **Video-speed electronic paper based on electrowetting**, Nature, Vol. 425, September 2003, pp. 383-385.

[10] **http://www.liquavista.com/**, 2008.

[11] **http://www.varioptic.com/**, 2008.

[12] M. R. Douglass, **DMD reliability: a MEMS success story**, Proceedings of SPIE, Vol. 4980, January 2003.

[13] G. Van Doorselaer, D. Cuypers, H. De Smet, J. Van den Steen, A. Van Calster, K. Ten and L. Tseng, **A XGA VAN-LCoS Projector**, Proceedings of the 22nd International Display Research Conference (IDRC) (Eurodisplay 2002), October 2002, pp. 205-208.

[14] **http://www.est-kl.com/projection/elumens/**, 2008.

[15] J. Gurski and L. M. Quach, **Display Technology Overview**, Lytica White Paper (http://www.lytica.com/), July 2005, pp. 1-37.

[16] P. Compo, **Display Technology at DuPont**, Displaybank (http://www.displaybank.com/), July 2007.

[17] R. M. Soneira, **Display Technology Shoot-Out: Comparison of CRT, LCD, Plasma, DLP and LCoS Technologies**, DisplayMate Technologies Corp. (http://www.displaymate.com/), 2008.

[18] **Display Technology Comparison**, Echostar Satellite LLC, (http://tech.dishnetwork.com/departmental_content/techportal/images/pdf/hdtvdisplay.pdf), January 2006.

[19] **http://www.i-techcompany.com/**, 2008.

[20] R.C. Liang, **Microcup Electrophoretic and Liquid Crystal Displays By Roll-to-Roll Manufacturing Processes**, Flexible Display and Microelectronic Conference, February 2003.

[21] **AVR241: Direct driving of LCD display using general IO**, Application Note 8-bit AVR Microcontrollers (Atmel Corporation), 2004.

[22] **Using the DS89C450 as a Static LCD Display Controller**, Application Note 4039 (Maxim Integrated Products), April 2007.

[23] **Driving LCD Displays**, Golden View Display Incorporated (http://www.goldenviewdisplay.com/), 2008.

[24] A. Lovrich, **Using PIC16C5X Microcontrollers as LCD Drivers**, Application Note 563 (Microchip Technology Inc.), 1997.

[25] L. E. Tannas, W. E. Glenn, T. Credelle, J. W. Doane, A. H. Firester, M. Thompson, **Display Technologies in Japan**, WTEC (World Technology Evaluation Center, http://www.wtec.org/loyola/), June 1992.

[26] P. M. Alt and P. Pleshko, **Scanning Limitations in Liquid Crystal Displays**, IEEE Transactions on Electronic Devices, Vol. 21, 1974, p. 146.

[27] **http://www.agc-group.com/**, 2008.

[28] **http://www.corning.com/**, 2008.

[29] **http://www.displaysearch.com/**, 2008.

[30] **Toppan Annual Report 2004**, Toppan (http://www.toppan.co.jp/english/ir/annual/04/), September 2004.

[31] **http://www.tok.co.jp/**, 2008.

[32] T. Ryoichi, **Coater & Developer for large size LCD: Tokyo Ohka Kogyo expands its market share with spinless coater**, Semiconductor FPD World, March 2005.

[33] M. LaPedus, **Call to slam brakes on 450-mm fabs**, EETimes (http://www.eetimes.com/), October 2007.

[34] **http://www.intel.com/**, 2008.

[35] Denis Nothern, **Emerging Plastic Films for Flexible Electronics Substrates**, Materials, Science and Engineering (MSE 542, University of Michigan), Cornell Flexible Electronics Initiative (FEI), 2006.

[36] A. Jones, I. McDowall, H. Yamada, M. Bolas and P. Debevec, **Rendering for an Interactive 360° Light Field Display**, Proceedings of the 34^{th} International Conference on Computer Graphics and Interactive Techniques (SIGGRAPH 2007), August 2007.

[37] A. Chekhovski and H. Toshiyoshi, **3-dimensional water display**, IEICE Electronics Express, Vol. 4, 14, July 2007, pp. 430-434.

[38] L.A. Rodert, **An Investigation of the Prevention of Ice on the Airplane Windshield**, N.A.C.A. (National Advisory Committee for Aeronautics) Technical Note 754, Washington, 1940.

[39] C. Weeks, **Carbon nanotube transparent electrodes for touch screens**, Touch Panel (Veritas et Visus), Vol. 1, 9, October 2006, pp. 34-37.

[40] **http://www.eikos.com/**, 2008.

[41] S.A. Bashar, **Study of Indium Tin Oxide (ITO) for Novel Optoelectronic Devices**, Doctoral Thesis, 1998.

[42] M.G. Kang and L.J. Guo, **Nanoimprinted Semitransparent Metal Electrodes and Their Application in Organic Light-Emitting Diodes**, Advanced Materials, Advanced Materials, Vol. 19, 10, April 2007, pp. 1391-1396.

[43] W.A. MacDonald, **Latest Developments in Substrates for Flexible Electronics**, FlexiDis training workshop, February 2006.

[44] D.P. Webb, D.A. Hutt, D.C. Whalley and P.J. Palmer, **A Substrateless Process for Sustainable Manufacture of Electronic Assemblies**, Proceedings of the 2^{nd} Electronics System-Integration Technology Conference (ESTC 2008), September 2008, pp. 511-516.

[45] C.A. Harper (chief editor), **Electronic Packaging and Interconnection Handbook**, New York (4th edition), McGraw-Hill, 2005.

[46] C.Q. Cui, **High Density Interconnect on Flexible Substrate**, SCV (Santa Clara Valley) CPMT Society Chapter Meeting, June 2004.

[47] S.R. Breed and R.F. Pernice, **Stencil Printing SMT Adhesives: A Technology Review**, MPM Corporation white paper, February 2003.

[48] V. Shah, R. Mohanty, J. Belmonte, T. Jensen, R. Lasky and J. Bishop, **Process Development for 01005 Lead-Free Passive Assembly: Stencil Printing**, Speedline Technologies white paper (http://www.speedlinetech.com/), 2008.

[49] H. Kipphan, **Handbook of Print Media**, Berlin, Springer-Verlag, 2001.

[50] B. de Gans, P. C. Duineveld and U. S. Schubert, **Inkjetprinting of Polymers: State of the Art and Future Developments**, Advanced Materials, Vol. 16, 3, February 2004, pp. 203-213.

[51] DELTA, IVF, SINTEF, VTT **The Nordic Electronics Packaging Guideline**, developed with support from the Nordic Industrial Fund (downloadable from http://extra.ivf.se/ngl/), September 2000.

[52] J. Vanfleteren, **Adhesive flip-chip technology**, IMAPS BeNeLux Spring Event, May 2004.

[53] M. Paulasto-Kröckel and T. Hauck **Flip Chip Die Attach Development for Multichip Mechatronics Power Packages**, IEEE Transactions on Electronics Packaging Manufacturing, Vol. 24, 4, October 2001, pp. 300-306.

[54] H. Kristiansen and J. Liu, **Overview of Conductive Adhesive Interconnection Technologies for LCDs**, IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, Vol. 21, 2, June 1998, pp. 208-214.

[55] B. Vandecasteele, J. Määttänen, T. Podprocký and J. Vanfleteren, **Low temperature flip chip attachment for flexible display applications**, Proceedings of the International Conference on Electronics Packaging, 2004, pp. 307-312.

[56] H. Duran, **Chip-on-Foil: An Emerging Technology for Display Driver Electronics**, Technology Leadership Day (TLD) 2002, HTA Lucerne, Horw, October 2002.

[57] H. Kim, S. Hong, S. Jang, Y. Moon and K. Paik, **Bubbles Formation in Rigid-Flexible Substrates Bonding using Anisotropic Conductive Films (ACFs) and Their Effects on ACFs Joints Reliability**, Proceedings of the IEEE Electronics Packaging Technology Conference, 2005, pp. 734-739.

[58] M. Yim, H. Kim, C. Chung and K. Paik, **Degradation Mechanism and Reliability of Flip Chip Interconnects using Anisotropic Conductive Adhesives for High Current Density Packaging Applications** Electronic Components and Technology Conference, 2006, pp. 338-343.

[59] M. Yim and K. Paik, **Recent advances on anisotropic conductive adhesives (ACAs) for flat panel displays and semiconductor packaging applications**, Elsevier International Journal of Adhesion & Adhesives, Vol. 26, July 2005, pp. 304313.

[60] M. Yim, J. Hwang and K. Paik, **Anisotropic conductive films (ACFs) for ultra-fine pitch Chip-On-Glass (COG) applications**, Elsevier International Journal of Adhesion & Adhesives, Vol. 27, March 2006, pp. 77-84.

[61] J. Liu, **Recent advances in conductive adhesives for direct chip attach applications**, Microsystem Technologies, Vol. 5, 1998, pp.72-80.

[62] J. Kim, D. Kim, Y. Lee and S. Jung, **Analysis of Failure Mechanism in Anisotropic Conductive and Non-Conductive Film Interconnections**, IEEE Transactions on Components and Packaging Technologies, Vol. 31, 1, March 2008, pp. 65-73.

[63] **http://www.hitachi-chem.co.jp/english/products/do/index.html**, 2008.

[64] M. Richardson, **Packed and Stacked**, New Electronics (http://www.newelectronics.co.uk/), December 2007.

[65] **http://www.plasticlogic.com**, 2008.

[66] **http://www.eink.com/**, 2008.

[67] **http://www.st.com/**, 2008.

[68] M. Yim and K. Paik, **The Contact Resistance and Reliability of Anisotropically Conductive Film (ACF)**, IEEE Transactions on Advanced Packaging, Vol. 22., 2, May 1999.

[69] US Department of Defense **Method 2019.7: DIE SHEAR STRENGTH**, Test Method Standard Microcircuits Mil-Std-883, March 2003.

[70] **http://www-leti.cea.fr/**, 2008.

[71] X. Fohrer and R.E. De Caro, **OLED Display System Performance Considerations**, SID-ME Chapter Spring 2002 meeting on Polysilicon technology and applications for AM-LCDs and AM-OLEDs, March 2002.

[72] Y.T. Yen and Y.C. Lin, **Study peeling strength of tape carrier packaging and chip scale packaging**, Elsevier Sensors and Actuators A, Vol. 139, February 2007, pp. 330336.

[73] H. Yamaguchi, **Development of Non-Adhesive Type Flexible Copper Clad Laminate "UPISEL®-N"**, Journal of Photopolymer Science and Technology, Volume 16, 2, May 2003, pp. 233-236.

[74] **Hitachi Anisotropic Conductive Film ANISOLM® AC-8408Y**, Hitachi Chemical Data Sheet R&D Department Goshomiya Works, 2004.

[75] **Hitachi Anisotropic Conductive Film ANISOLM® AC-7250U-16**, Hitachi Chemical Data Sheet R&D Group, Goshomiya Production Center, 2004.

[76] **http://www.lci.kent.edu/boslab/projects/reflective_displays/sc_mode.html**, 2008.

[77] D. Coates, **Polymer-dispersed Liquid Crystals**, Journal of Materials Chemistry, Vol. 5, 12, 1995, pp. 2063-2072.

[78] T. Schneider, D.J. Davis, S. Franklin, N. Venkataraman, D. McDaniel, F. Nicholson, E. Montbach, A. Khan, and J.W. Doane, **New Developments in Flexible Cholesteric Liquid Crystal Displays**, Proceedings of SPIE, Vol. 6487, 64870J-1-5, 2007.

[79] E.A. Büyüktanýr, A. Glushchenko, B. Wall, J.L. West, M. Mitrokhin and B. Holter, **Flexible Bistable Smectic-A LCD Based on PDLC**, SID Symposium Digest of Technical Papers, Vol. 36, 1, May 2005, pp. 1778-1781.

[80] K. O'Donnell, J. Kostetsky and R.S. Post, **Stress Control in NiV, Cr and TiW Thin Films used in UBM and Backside Metallization**, Proceedings of IMAPS Flip Chip Technology Workshop and Exhibition 2002 (http://www.flipchips.com/tutorial22.html), June 2002.

[81] **http://www.flexidis-project.org**, 2004-2008.

[82] J. Brill, **Technologies for plastic LCDs**, 4^{th} Flexible Display and Microelectronics Conference, February 2005.

[83] **Underfills and Encapsulants**, Loctite and Hysol brochure (http://www.loctite.com), 2008.

[84] J. Balde (editor), **Foldable Flex and Thinned Silicon Chips for Multichip Packaging**, Boston, Kluwer Academic Publishers, 2002.

[85] J. Fjelstadt, **Flexible Circuit Technology (Addendum)** Seaside (3th edition), BR Publishing, 2008, pp. 62-78.

[86] C. Banda, R.W. Johnson, T. Zhang, Z. Hou, Member, and H.K. Charles, **Flip Chip Assembly of Thinned Silicon Die on Flex Substrates**, IEEE Transactions on Electronics Packaging Manufacturing, Vol. 31, 1, January 2008.

[87] D. Manessis and A. Ostmann, **Embedding Technologies for SiP Manufacturing**, Advanced Packaging, July 2008, pp. 28-32.

[88] **http://lalehcomputer.20un.com**, 2008.

[89] **PRIMERO 6/7 6-Digit, 7-Segment Numeric Display Module DATA SHEET**, Aveso Printed Electronic Displays (http://www.avesodisplays.com/), 2008.

[90] **http://www.verdantelectronics.com/**, 2008.

[91] W. Christiaens, B. Vandevelde, E. Bosman, and J. Vanfleteren, **UTCP: 60 um thick bendable chip package**, Proceedings of IWLPC (San Jose), November 2006, pp. 114-119.

[92] **http://hdmicrosystems.com/**, 2008.

[93] Melles Griot, **Gausian Beam Optics: Gaussian Beam Propagation**, Melles Griot Catalog X (http://www.mellesgriot.com/pdf/CatalogX/X_02_2-5.pdf), pp. 2.2-2.5.

[94] M. Schlesinger and M. Paunovic (editors), **Modern Electroplating**, New York (4^{th} edition), Wiley, 2000.

[95] E.I. Haskal, I.D. French, H. Lifka, R. Sanders, P. Bouten, T. Kretz, E. Chuiton, G. Gomez, F. Mazel, C. Prat, F. Templier, M.D. Campo, F. Stahr, **Flexible OLED Displays Made with the EPLaR Process**, Proceedings of EURODISPLAY 2007, September 2007.

[96] I. French, **EPLaR and FlexiDis**, FlexiDis Newsletter n^o 3 (downloadable from http://www.flexidis-project.org), December 2007, p. 6.

[97] Finetech, e.g. **Press release on Fineplacer FEMTO**, Assembly & Packaging SMT 2008 (downloadable from http://www.finetech.de), June 2008.

[98] L. Lamport, **LaTeX A Document Preparation System**, Addison-Wesley, California 1986.