

Ontwerp van intelligente aanstuurcircuits in een hoogspanningstechnologie voor het minimaliseren van het vermogenverbruik in bistabiele beeldschermen

Design of an Intelligent High-Voltage Display Driver to minimize the Power Consumption in Bistable Displays

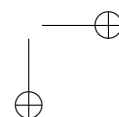
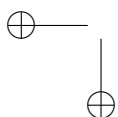
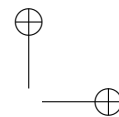
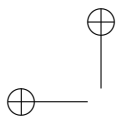
Ir. Ann Monté

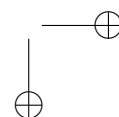
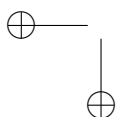
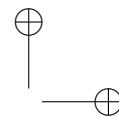
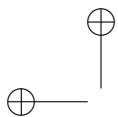
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Proefschrift ingediend tot het behalen van de graad van
Doctor in de Ingenieurswetenschappen
Elektrotechniek

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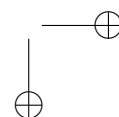
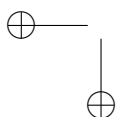
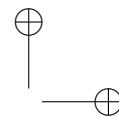
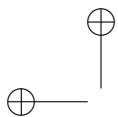
NUR code:

Depot nummer:

Promotor:

Prof. dr. ir. J. Doutrelaigne

Onderzoeksgroep CMST
Vakgroep Electronics and Information Systems
Technologiepark 914A
B-9052 Zwijnaarde



Dankwoord

In het eerste en waarschijnlijk meest gelezen stukje van dit doctoraat, heb ik de eer iedereen te vermelden die op een professionele of iets minder professionele wijze heeft meegeholpen aan het tot stand komen van dit werk. De vier jaar die dit werk omhelsd hebben, waren niet enkel technologisch heel verrijkend, het was ook een aangename periode. De leuke sfeer die heerst in gebouw 914 zorgt ervoor dat de eenzaamheid van een doctoraat in het niets verdwijnt.

De eerste belangrijke personen die ik graag zou vermelden, zijn André Van Calster en Jan Doutreloigne. Aan André: dank u voor de kans die ik gekregen heb om dit doctoraat te mogen doen! Ook heel erg bedankt voor de sponsoring van allerlei leuke en lekkere etentjes.

Dit werk zou niet gelukt zijn zonder mijn promotor Jan. Hij heeft ons meermaals doen perplex staan met zijn intelligente opmerkingen, de tijd die hij vrijmaakt voor ons, het geduld waarmee hij te werk gaat en al die andere dingen die soms te snel tot een evidentie herleid worden.

De leuke werksfeer was er niet geweest zonder de collega’s! Daarom in volgorde van luid naar stil:

Wim, hopelijk heb je al veel plezier beleefd aan uw nieuw huisgenootje! Erwin, kom gerust maar eten moest er een frituursaturatie optreden. Steven en Liesbeth, het etentje voor jullie trouw was zeker één van de hoogtepunten. Geert, merci voor het LaTeX en ander advies. Jona: hoe het geven van een emailadres tot zoveel veranderingen kan leiden! Verder wil ik de andere middag eet-genootjes bedanken voor hun gezellige compagnie! Nadine, we willen gerust een dagje vrij nemen om in Frankrijk te komen barbecueën :-)

Iets dichterbij mij en dus werkgerelateerd iets belangrijker, zijn mijn eigen

bureaugenootjes. Pieter, het is tof dat ik een werk-partnerke gekregen heb! Benoit, succes in jullie nieuwe huisje en met de 2 kindjes! Bedankt voor de immere bereidwilligheid om te helpen. Jodie, zeker niet aarzelen om cakes te blijven maken en ze ons te laten proeven weliswaar. Stefaan, je zang- en fluitconcerten zorgden voor een zekere sfeer, na het doctoraat een muziek- of leerkracht carrière? Vincent, merci voor alle UNIX-hulp. Dominique, vanaf nu de kruimeltjes opkuisen hé :-)
Ook aan de andere collega’s die steeds klaar staan: Herbert, Dieter, ...: MERCI! Eveneens Wim Meeus en Jan Van Campenhout waren een schakeltje in dit werk door hun VHDL kennis te delen.

Aangezien het leven verder gaat buiten de werkuren, is ook dit paragraafje niet achterwege te laten. De eerste en belangrijkste personen in mijn leven die ertoe bijgedragen hebben dat ik sta waar ik nu ben: mijn ouders. Merci voor de financiële en andere steun. Doe zo voort! Ook nu het kotleven reeds lang achter de rug is, mogen jullie nog steeds pakjes eten meegeven. Bart, jij mag hen het eerste kleinkindje bezorgen. Ook alle andere familieleden en aanverwanten worden bedankt voor hun goede daden in mijn leven.

Een gezonde geest in een gezond lichaam... daarvoor zorgt niet alleen sport, maar ook de mensen met wie regelmatig een pintje gedronken wordt. Wandelvriendjes, studievriendjes, de mensen van Melle, de zwalmkoets, T&H, Sigrid, Domi, huppelkonijn-David, de broertjes en andere aanverwanten, ...: spring allemaal altijd maar eens binnen als jullie zin hebben.

Last but not least is er natuurlijk Alwin. Het meest gelukkig ben ik simpelweg om wie je bent! Dat je mijn doctoraat wil nalezen en al die andere dingen voor mij doet, maken het des te perfecter!

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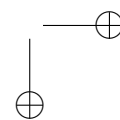
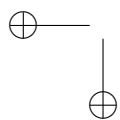
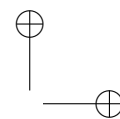
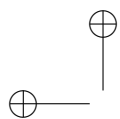
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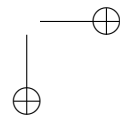
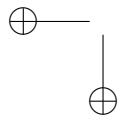
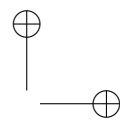
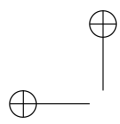
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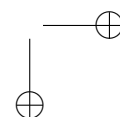
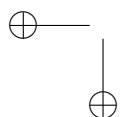
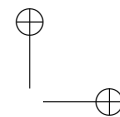
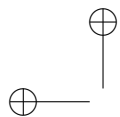
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Samenvatting

Een groot probleem in batterijgevoede draagbare toepassingen (zoals een e-book of een Palm) is de beperkte levensduur van de batterij. De levensduur kan vergroot worden door het vermogenverbruik van het toestel naar beneden te halen. Dit vermogenverbruik wordt bepaald door de functies die moeten uitgeoefend worden (bij een gsm is dit bv. het zenden en ontvangen van signalen) alsook door de aanstuurlogica van het scherm. Een goede keuze van het type beeldscherm en een optimalisatie van de aanstuurlogica kan leiden tot een vermindering van het vermogenverbruik.

Gedurende dit doctoraat is een aansturbord voor een beeldscherm ontworpen met als groot voordeel dat het tot 50% minder vermogen verbruikt in vergelijking met traditionele aanstuurcircuits. Het type beeldscherm waarop dit onderzoek gericht is, is een Cholesterisch Texture Liquid Crystal beeldscherm. Dit wordt vaak aangeduid d.m.v. de Engelse afkorting ChTLCD (of simpelweg ChLCD). LCD staat voor Liquid Crystal Display. Het is een bistabiel beeldscherm wat betekent dat het vloeibare kristal twee stabiele toestanden kan aannemen wanneer er geen spanning aangelegd wordt. In één van die toestanden is het vloeibaar kristal zodanig geordend dat het invallende licht erdoor gaat en geabsorbeerd wordt door het materiaal dat zich achter de kristallen bevindt. In deze toestand kan de toeschouwer geen kleur waarnemen en is de corresponderende pixel zwart. In de andere toestand wordt het licht gereflecteerd en krijgen we een witte pixel. Dankzij deze eigenschap is een bistabiel beeldscherm in staat een beeld op het scherm te behouden indien de spanningsbron afgeschakeld wordt. Voor toepassingen waar geen bewegende beelden vereist zijn, is dit heel interessant. Een groot nadeel echter voor het vermogenverbruik zijn de hoge spanningen vereist om de vloeibare kristallen van toestand te doen veranderen. Daarenboven moeten de aanstuurgolven

vormen heel precies ontworpen worden.

In dit boek wordt een grondige analyse gemaakt van de aanstuurgolfformen en hoe deze kunnen geoptimaliseerd worden met als doel het vermogenverbruik in de aanstuurlektronica te verminderen.

Er bestaan zowel conventionele als dynamische aanstuurmethodes. De dynamische aanstuurmethodes zijn sneller dan de conventionele, maar kunnen geen grijswaarden produceren. Daarom richten we ons in dit werk op de conventionele aansturing. Een grondige theoretische analyse van de mogelijke aanstuurgolfformen heeft tot het ontwerp van een nieuw aanstuurschema geleid. Met behulp van een microcontroller en een bestaande aanstuurchip was het mogelijk een beeldscherm aan te sturen met dit nieuwe aanstuurschema. Dit is gedaan voor verschillende beelden waarbij telkens het vermogenverbruik gemeten werd. De metingen waren veelbelovend en dus was de volgende stap het ontwerp van een volledige driver waarin de uitgedokterde logica geïmplementeerd is. Om nog een extra vermogenbesparing te realiseren worden speciale multiplexers gebruikt in de aanstuurchip die in staat zijn hun uitgangsspanning te behouden indien de laagspanningsvoeding afgeschakeld wordt.

In hoofdstuk 2 wordt begonnen met een overzicht van de verschillende beeldschermtechnologieën. Zowel de klassieke CRT (Cathode Ray Tube), het plasma beeldscherm, het elektronisch papier als de minder ingeburgerde technologieën komen aan bod.

Aangezien dit doctoraat voornamelijk gericht is op het aansturen van een ChLCD is het belangrijk een goed begrip te hebben van de fysische en optische eigenschappen van vloeibare kristallen en de verschillende manieren waarop een LCD (Liquid Crystal Display) kan aangestuurd worden. Dit wordt besproken in hoofdstuk 3. Een LCD kan zowel actief als passief aangestuurd worden. Afhankelijk van de lichtbron en waar deze zich bevindt ten opzichte van het beeldscherm kan een onderscheid gemaakt worden tussen emissieve, transmissieve en reflectieve beeldschermen. Wat dit allemaal betekent wordt tevens uitgelegd in dit 3^{de} hoofdstuk. Verder worden de verschillende beeldschermtechnologieën onderling vergeleken.

Hoofdstuk 4 richt zich nog specifiek op de fysische en de optische eigenschappen van het cholesterisch texture vloeibaar kristal. De kennis van de optische eigenschappen maakt het mogelijk om de aanstuurgolfformen voor een ChLCD op te stellen. Zowel het conventionele als het dynamische aanstuurschema wordt besproken in dit hoofdstuk. Er worden

ook enkele toepassingen van een ChLCD geïllustreerd.

Eens gekend aan welke voorwaarden de aanstuurgolfformen moeten voldoen, kan nagegaan worden of enige optimalisatie op het vlak van energieverbruik mogelijk is. Daartoe wordt begonnen met het opstellen van een formule voor het energieverbruik. Dit wordt gedaan in hoofdstuk 5. Uit deze formule blijkt dat niet de absolute waarden van de rij- en kolomspanningen de bepalende factor zijn, maar enkel hun verschil, m.a.w. de pixelspanning. Daarnaast zijn ook het aantal rijen en kolommen en de capaciteit van het beeldscherm bepalende factoren.

Nu we ook weten welke parameters bijdragen tot het energieverbruik, is het mogelijk enkele methodes voorop te stellen die tot een vermindering van het energieverbruik kunnen leiden. Deze zijn het aanbrengen van tussenniveaus, de aanpassing van de aanstuurgolfformen aan het beeld en eventueel het slechts gedeeltelijk vernieuwen van het beeld. Extra tussenniveaus kunnen aangebracht worden met behulp van een externe spanningsbron ofwel door een weldoordachte ladingsverdeling in het beeldscherm. Deze principes en hoe hiermee een nieuw aanstuurschema kan opgesteld worden, worden uitgelegd in hoofdstuk 6. Het gebruik van het ontworpen aanstuurschema leidt theoretisch tot een vermogenverbruik dat minder dan de helft is vergeleken met het eenvoudigst mogelijke aanstuurschema.

Gezien dit positieve resultaat is een voor de hand liggende volgende stap nagaan of dit nog steeds blijkt in de praktijk. Daartoe werd een reeds bestaand aanstuurbord aangepast. De generatie van tussenniveaus door het kortsluiten van rijen of kolommen kan hiermee echter niet getest worden omdat er geen schakelaars aanwezig zijn tussen de rijen en kolommen. De golfformen die het scherm aansturen worden berekend in een microcontroller. Er gebeurt een optimalisatie van de aanstuursignalen op basis van het af te beelden patroon. Het aantal spanningsniveaus dat kan gebruikt worden, wordt bepaald door het aantal aanwezige spanningsbronnen. De hardware van het testbord en de benodigde software worden besproken respectievelijk in hoofdstuk 7 en 8. De metingen die gedaan zijn voor verschillende beeldpatronen bevestigen het voordelige aspect van het toepassen van de voorgestelde energiebesparende principes.

Aangezien de testmetingen veelbelovend waren, werd er overgegaan tot het zelf ontwerpen van een aanstuurbord dat een compleet andere architectuur heeft dan het reeds bestaande. Het ontworpen aanstuurbord bestaat uit een digitaal en een analoog gedeelte. Het digitale deel bevat

een microcontroller die instaat voor de communicatie met een externe computer en voor de communicatie tussen het geheugen dat zich op het bord bevindt en de FPGA (Field Programmable Gate Array). De FPGA bevat de nodige logica om de meest efficiënte aanstuurgolfvormen te berekenen en genereert de controle signalen voor het analoge deel. Het analoge deel bestaat voornamelijk uit schakelaars die geoptimaliseerd zijn in functie van de beoogde toepassing. Belangrijk zijn bijvoorbeeld het stroomniveau en de schakelduur. De signalen verstuurd door de FPGA zorgen ervoor dat de schakelaars zich openen en sluiten op de juiste momenten. Door de gate capaciteit van de uitgangstransistoren in de schakelaars te controleren is het mogelijk de gewenste uitgangsspanning te behouden op de rijen en kolommen wanneer de laagspanningsvoeding afgeschakeld wordt en er dus geen stroom meer vloeit. De hardware van het ontworpen aanstuurbord en enkele simulatie resultaten zijn weergegeven in hoofdstuk 9.

De meetresultaten gedaan met het nieuwe aanstuurbord worden besproken in hoofdstuk 10.

Summary

A big problem in portable applications like e-books and PDAs (personal digital assistant) is the lifetime of the batteries. The power consumption of the battery is determined by the operations the instrument has to fulfill on the one hand and by the display driver on the other hand. A reduction of the power consumption can be achieved by a good choice of display type and by optimizing the display driver.

During this Ph.D. an intelligent display driver is designed in which the consumed energy is reduced up to 50% compared to traditional drivers. More specifically, this research is focused on Cholesteric texture Liquid Crystal Displays. These displays are bistable, meaning there are two stable states the liquid crystal can take on when no power is applied. In one of these states, no light is reflected and therefore the corresponding pixel appears black. In the other state where all light is reflected, the pixel appears white. Due to these properties it is possible to maintain an image unchanged on the screen when the power supply is removed. This is a very interesting quality useful for displays without a high refresh rate. Nevertheless, there are some drawbacks. In the cholesteric texture liquid crystal displays, high voltage drive waveforms (up to 100 V) are required. This in combination with the demand of very low internal power consumption can pose difficulties. Moreover, the timing parameter demands are very strong.

In this book, a profound analysis of the drive waveforms is given together with the methods that can be used to improve them. The choice is made to focus on conventional instead of dynamic drive schemes. Dynamic drive schemes are faster, but can not produce gray pixels. After a theoretical analysis of the drive waveforms and the development of a new power-efficient drive scheme, a first test of this drive scheme was done with the help of a microcontroller. The power consumption was measured for dif-

ferent images. Since the measurement results were promising, a complete driver board was developed implementing the developed logic. The hardware of the driver board was also optimized. Special dynamically controlled High-Voltage switches are used to restrict the power consumption. Chapter 2 starts off with a global overview of different display technologies. First, the old Cathode Ray Tube (CRT) display that used to be present in every home is explained followed by a discussion of the Plasma Display Panel offering an alternative for the CRT. Furthermore, a concise description of some other established display technologies is given.

The other well-known display technology that has replaced the CRT is the Liquid Crystal Display (LCD), which is discussed in detail in chapter 3. The LCDs can differ in a lot of ways. A first distinction can be made between Active Matrix LCDs and Passive Matrix LCDs. According to the type of liquid crystal used in the display, an extra categorization can be made. Another basis for a division is the type of light source. The display can be emissive, reflective or transmissive. The physical characteristics of these different kinds of LCDs are discussed in this chapter. In the end, different display technologies are compared.

Since this Ph.D. is primarily aimed at Cholesteric texture LCDs (ChTLCDs or ChLCDs), a detailed analysis of the physical and optical properties, and the drive scheme that can be deduced from these properties, is given in chapter 4. A number of implementation possibilities for a conventional drive scheme as well as the dynamical drive scheme are mentioned. Afterwards, some applications of the ChLCD are depicted.

With the knowledge of the optical properties of the cholesteric texture liquid crystal, it is possible to compose drive waveforms for the ChLCD. However, the purpose of this Ph.D. is more than just driving the display. The display needs to be driven in a power-efficient way. To be able to compose the drive waveforms in a power-efficient way, it is useful to have some kind of formula that provides an insight into the important parameters that contribute to the power consumption. In chapter 5 such a formula is derived. An important conclusion is that not the absolute values of the row and column voltages determine the resulting power consumption, but the voltage over the pixels. Furthermore, the number of rows and columns and the display capacitance contribute to the power consumption in the driver.

The composition of a power-efficient drive scheme is described in chapter 6. It is important to view the expression 'power-efficient' in the context

of this work. The theoretical methods that can be used to reduce the power consumption are implemented while keeping in mind the practical aspects of developing a driver. In the beginning of the chapter, the principles used in this work are explained. These are the addition of intermediate levels with the help of an external voltage source or by short-circuiting the appropriate rows or columns, the generation of image-dependent waveforms and selective update of the display. Afterwards, these principles are applied to the row and column waveforms. With the drive scheme developed in this Ph.D. the energy consumption in the driver is reduced by more than half theoretically compared to the most simple drive scheme.

These positive theoretical results are begging for a practical implementation. To that end, an existing driver for a ChLCD is used in combination with a microcontroller. The derived logic is implemented into the microcontroller. The latter generates the control signals so the correct voltage levels are applied to the rows and columns. The hardware and the software of the test board are described in chapter 7 and 8 respectively. In the existing driver it is not possible to short-circuit adjacent rows. Therefore it is not possible to test the usefulness of charge recycling by short-circuiting rows or columns. The benefit of the other energy-saving principles is researched by measuring the power consumption in the driver when displaying an image. The measurement is done for different images. The results confirm the gain predicted in the theoretical research.

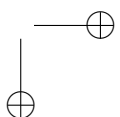
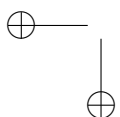
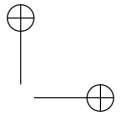
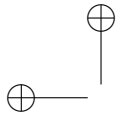
After the promising measurement results with the test board, a new driver is developed. The driver has a different operating principle than the one used on the test board. There is a digital and an analogue part. The digital part consists of a microcontroller responsible for both the communication with an external computer and the communication between the on-board memory and the FPGA (Field Programmable Gate Array). The FPGA is the logic cell that calculates the most efficient drive waveforms and generates the control signals for the analogue part. The analogue part mainly consists of switches. The switches are adapted to the requirements of driver. The signals received from the FPGA are converted so they close the correct switches. By controlling the gate capacitance of the output transistors in the switches it is possible to maintain correct output voltages in the driver without the need for a continuous current flow. The hardware of the developed driver and some simulation results can be found in chapter 9.

The results of the measurements done with the new driver are discussed

in chapter 10.

Notations

Notation	Meaning
AM-LCD	Active Matrix LCD
BCT	Bistable Cholesteric Texture
ChLCD	Cholesteric Liquid Crystal Display
ChTLCD	Cholesteric Texture Liquid Crystal Display
CMOS	Complementary Metal Oxide Semiconductor
CRT	Cathode Ray Tube
E-paper	Electronic Paper
EPD	Electrophoretic Display
FED	Field Emission Display
FPGA	Field-Programmable Gate Array
Gnd	Electrical Ground
HV	High-Voltage
IPS	In-plane Switching
LC	Liquid Crystal
LCD	Liquid Crystal Display
LCOS	Liquid Crystal on Silicon
OLED	Organic Light-emitting Diode
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDP	Plasma Display Panel
PM-LCD	Passive Matrix LCD
SED	Surface-conduction Electron-emitter Display
STN	Super Twisted Nematic
TFT	Thin Film Transistor
TN	Twisted Nematic
VAN	Vertically-Aligned Nematic



Chapter 1

Introduction

1.1 The need for power-efficient portable display systems

An application that has become more and more widespread these last years is the portable electronic tool with an embedded display. Examples are the PDA (Personal Digital Assistant), e-book, mobile phone and smartcard. The most annoying problem faced while using these tools is the battery-capacity. Without a night time charge of the batteries one is not able to use the electronic tool. Therefore, it is important to develop these devices in a way so they consume as little power as possible. In some of these applications, a big amount of the power consumption is used by the display driver. A really important challenge is the reduction of power consumption in the display drivers. Unlike Game Boys for example, the display content of the applications mentioned before does not change continuously. Therefore, it is interesting to equip these devices with a bistable display. A bistable display contains a kind of inherent memory function by nature. This ensures that the image on the screen does not disappear when the power source is switched off. Of course, this is an enormous advantage in battery-powered applications as these displays do not need a continuous refresh.

Figure 1.1 shows an example of a bistable display, an electronic price tag made by BridgeStone. Since price indications in a shopping mall have a very low refresh rate, it would be an enormous waste to use a traditional



Figure 1.1: Electronic price tag, BridgeStone

non-bistable display for this application. On the other hand, a piece of paper has the drawback that the content can not be changed and therefore every piece needs to be replaced when there is a price change. In Belgium, the department store Carrefour uses bistable displays to indicate the price of a product.

The electronic display proposed in Figure 1.1 is an example of an e-paper based on the EPD technology (explained in next chapter). In this Ph.D. we will focus on a different kind of bistable display, namely the Cholesteric Texture Liquid Crystal Displays (ChLCDs). The different display technologies are explained in chapters 2, 3 and 4.

To have an idea about the energy consumption in a bistable display (for example ChLCD) compared to that in a non-bistable display, we make a rough estimation for the electronic newspaper. Suppose the image content changes about every 10 seconds, in a non-bistable environment this means that the image is refreshed every 20ms, adding up to 500 times during the 10 seconds. With the drive voltage being 5V in the non-bistable technology and 40V for the ChLCD, for this application the ChLCD uses $500/8=125$ times less energy than the non-bistable technology.

Most bistable displays offer even more important features like the unlimited multiplex ratio, high resolution, the possibility to produce bright reflective color displays and the adaptability of gray levels. Unfortunately, bistable displays need high-voltage transitions to switch the pixels from one stable state to the other. The high-voltage drive waveforms can reach voltages up to 100 V. Hence, special high-voltage drivers with low internal power consumption are needed. Another drawback is the complexity of the waveforms needed to drive the displays and strong demands are to be

1.2 Solution: design of a power-efficient bistable display driver 3

met involving the accuracy of voltage levels and timing parameters.

1.2 Solution: design of a power-efficient bistable display driver

Special high-voltage driver circuits, reducing the power consumption, have already been designed [1]. The focus on these drivers was particularly hardware-oriented. Some new CMOS-circuits were developed, including power-efficient level-shifters, high-voltage (HV) multiplexers and HV generators. An extra decrease in power consumption can be realized by adding an additional block of programmable logic to the display drivers, calculating the most efficient waveforms to be applied to the rows and columns for each image on the screen. It appears that for different images, a difference in power consumption exists. A profound knowledge of the image pattern dependency of the power consumption can help in composing an energy-efficient drive scheme. This provides the possibility to create row and column waveforms that generate the correct image on the display in an energy-efficient way.

The development of a driver for a cholesteric texture LCD with 16 different gray levels was the main task of this Ph.D. For that purpose, I first calculated the power consumption of existing drive schemes and investigated the influence of the important parameters. With this knowledge, it was possible to compose a more energy efficient drive scheme. The logic to calculate the drive waveforms was then programmed in an FPGA (Field Programmable Gate Array). To be usable, a complete driver board was developed having the FPGA as a component.

This book gives a profound analysis of the developed drive schemes, the developed driver board and a discussion of the measurement results. The power consumption is measured for three different image patterns. Compared to the traditional drive schemes, a power saving of up to 50% can be achieved.

1.3 Publications

The following journal papers have been published

- A. Monté, J. Doutreloigne and A. Van Calster, "A new Power-Efficient High-Voltage Driver for Bistable Displays", Chinese Journal of Electronic Devices, Vol. 31, number 1, Feb 2008.

The following papers have been submitted for publication in a SCI-journal

- A. Monté, J. Doutreloigne and A. Van Calster, "Driving Scheme Algorithms for Intelligent Energy-Efficient High-Voltage Display Drivers", submitted to IEEE Transactions on Circuits and Systems I.
- A. Monté, P. Bauwens and J. Doutreloigne, "A Low-Power High-Voltage Driver for Bistable Displays", submitted to Elsevier.
- P. Bauwens, A. Monté and J. Doutreloigne, "Improved Passive-Matrix Multiplexability with Modular Display", submitted to Elsevier.
- A. Monté, P. Bauwens, S. Maeyaert and J. Doutreloigne, "Driving Scheme Algorithms for Intelligent Power-Efficient High-Voltage Display Drivers", submitted to JSID.

The following papers have been presented at international conferences

- A. Monté, J. Doutreloigne and A. Van Calster, "An Intelligent Driving Scheme for High-Voltage Display Drivers", Proceedings of the 11th International Display Workshops IDW'04, Niigata, Japan, December 2004, pp. 1737 - 1740.
- A. Monté, J. Doutreloigne and A. Van Calster, "Principles to Reduce the Power Consumption in High-Voltage Bistable Display Drivers", Proceeding of the Twenty-Fifth International Display Research Conference, Eurodisplay 2005, Edinburgh, Scotland, pp. 148-151.
- A. Monté, J. Doutreloigne and A. Van Calster, "A Power-Efficient Way to Operate High-Voltage Bistable Display Drivers", Proceedings of the 12th International Display Workshops IDW 5, Takamatsu, Japan, December 2005, pp. 887-890.

1.3 Publications

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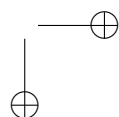
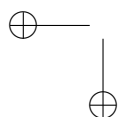
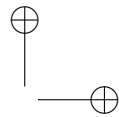
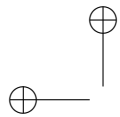
- A. Monté, J. Doutrelaigne and A. Van Calster, "A new Power-Efficient High-Voltage Driver for Bistable Displays", Proceedings of Asia Display 2007, Shanghai, China, Volume 1, March 2007, pp. 198-202.
- A. Monté, J. Doutrelaigne and P. Bauwens, "A Completely Integrated Power-Efficient High-Voltage Driver for Bistable Displays", Proceeding of the 27th International Display Research Conference, Eurodisplay 2007, Moscow, Russia, pp. 428-431.
- P. Bauwens, J. Doutrelaigne and A. Monté, "A New Driving Technology for Passive-Matrix Displays", Proceeding of the 27th International Display Research Conference, Eurodisplay 2007, Moscow, Russia, pp. 158-160.
- P. Bauwens, J. Doutrelaigne and A. Monté, "A Driver for Modular Passive-Matrix Displays", Proceedings of the 14th International Display Workshops, Sapporo, Japan, December 2007, pp. 1317-1320.

The following posters have been presented at international conferences, without proceedings

- A. Monté and P. Bauwens, "Design of a new power-efficient high-voltage bistable display driver", SID-ME Chapter Spring Meeting 2008, Jena, Germany, March 2008.
- P. Bauwens and A. Monté, "Driving a modular passive-matrix display", SID-ME Chapter Spring Meeting 2008, Jena, Germany, March 2008.

The following papers have been presented at national conferences

- A. Monté, J. Doutrelaigne and A. Van Calster, Principles to Reduce the Power Consumption in High-Voltage Bistable Display Drivers, Sixth FirW PhD Symposium, Faculty of Engineering, Ghent University, November 2005.
- A. Monté and J. Doutrelaigne, An Intelligent Power-Efficient High-Voltage Driver for Bistable Displays, Eighth FirW PhD Symposium, Faculty of Engineering, Ghent University, December 2007.



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Chapter 2

Display technologies

As more and more devices and products are equipped with a visual interface, display technologies become more important. This section gives an overview of the different display technologies starting from the old fashioned CRT.

2.1 Cathode Ray Tube

The cathode ray tube (CRT) was invented in 1897 by the German physicist Karl Ferdinand Braun and is therefore also called the "Braun tube". A CRT is a specialized vacuum tube in which images are produced when an electron beam strikes a phosphorescent surface. The phosphor material is arranged into an array of millions of tiny cells, called dots. The electron beam source is the electron gun at the back of the monitor. [1] refers to a more than 60 years old article about the CRT and its applications. A cross-section of a CRT is shown in Figure 2.1.

The cathode rays exist in the form of streams of high speed electrons emitted from the heating of a cathode inside a vacuum tube at its rear end. The released electrons form a beam within the tube due to the voltage difference applied across the cathode and the anode. The direction of this beam is then altered either by a magnetic or electric field to trace over the inside surface of the phosphorescent screen, covered by phosphorescent material.

The electron guns produce a controlled stream of electrons by thermionic

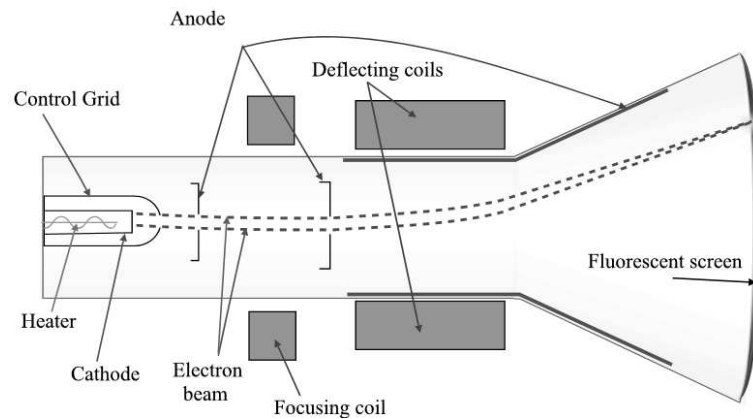


Figure 2.1: Cathode Ray Tube

emission and then focus it into a thin beam. The thermionic energy comes from a narrow filament. The gun is located in the narrow, cylindrical neck at the extreme rear of a CRT and has electrical connecting pins, usually arranged in a circular configuration, extending from its end. These pins provide external connections to the cathode and to various grid elements in the gun used to focus and modulate the beam. To produce a picture on the screen, these guns start at the top of the screen and scan very rapidly from left to right. Then, they return to the left-most position one line down and scan again, and repeat this to cover the entire screen. In performing this scanning or sweeping type motion, the electron guns are controlled by the video data stream coming into the monitor from the video card, which varies the intensity of the electron beam at each position on the screen. This control of the intensity of the electron beam at each dot is what controls the colour and brightness of each pixel on the screen. This all happens extremely quickly, and in fact the entire screen is drawn in a small fraction of a second.

There are three electron guns (on a colour monitor) that control the display of red, green and blue light respectively. The surface of the CRT is arranged to have these dots placed adjacently in a specific pattern. There are separate video streams for each colour coming from the video card, which allows the different colours to have different intensities at each point on the screen. One of two major technologies used to manufacture CRT dis-

2.2 Plasma Display Panel

11

plays that produce color images is the shadow mask (the other is aperture grille). Tiny holes in a metal plate separate the coloured phosphors in the layer behind the front glass of the screen. The holes are placed in a manner ensuring that electrons from each of the tube's three cathode guns reach only the appropriately-coloured phosphors on the display.

A CRT is a non-bistable display.

2.2 Plasma Display Panel

Another display technology in which the image is created by phosphors is PDP which stands for Plasma Display Panel. Plasma is an ionized gas and is therefore electrically conductive. Figure 2.2 shows the intersection of a PDP. A plasma display consists of several tiny cells positioned between two plates of glass, the front and the rear glass plate. Up against the glass plates there are electrodes. The address electrodes are placed behind the cells, along the rear glass plate. The transparent display electrodes being surrounded by an insulating dielectric material and covered by a magnesium oxide protective layer are mounted above the cell, along the front glass plate. The display electrodes are arranged so that they form a basic grid. In the different cells, there is an inert mixture of noble gases (neon and xenon). To ionize the gas and form a plasma in a particular cell, the electrodes that intersect with that cell are charged. When the intersecting electrodes are charged, an electric current flows through the gas in the cell. This current creates a rapid flow of charged particles, which stimulates the gas atoms to release ultraviolet photons. The released ultraviolet photons interact with phosphor material coated on the inside wall of the cell. Phosphors are substances that give off light when they are exposed to other light. When an ultraviolet photon hits a phosphor atom in the cell, one of the phosphor's electrons jumps to a higher energy level and the atom heats up. When the electron falls back to its normal level, it releases energy in the form of a visible light photon [2]. As in the CRT-displays, a pixel consists of 3 subpixels: one with a green light phosphor, one with a red light phosphor and one with a blue light phosphor.

The largest plasma video display in the world, which was shown at the 2008 Consumer Electronics Show in Las Vegas, Nevada, USA, North America, is currently a 150-inch (381 cm) unit manufactured by Matsushita Electrical Industries (Panasonic) standing 6 ft (180 cm) tall by 11 ft

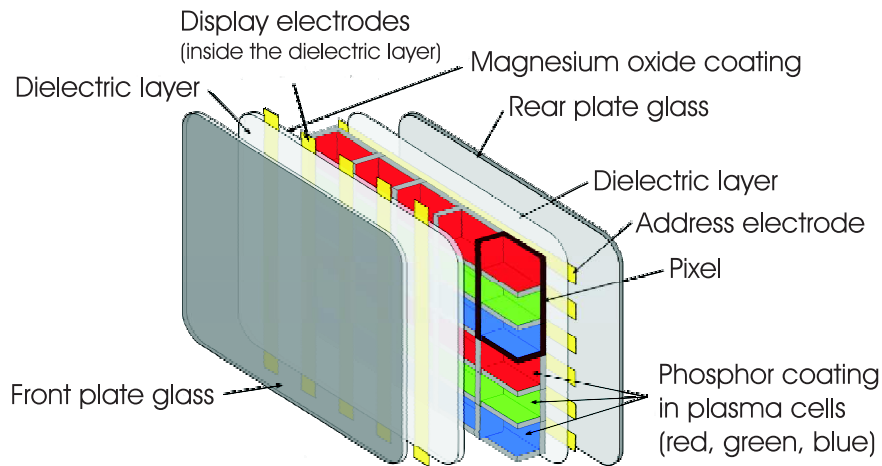


Figure 2.2: Plasma Display Panel

(330 cm) wide.

2.3 Field Emission Display

A third type of display using a phosphor coating is the Field Emission Display (FED) which is, just as the PDP, a flat panel display. It can be seen as the flat version of a CRT: instead of one electron gun to emit the electrons, a large array of fine metal tips or carbon nanotubes (CNT) [3], with multiple redundant emitters per area of display, is used in the FED. This is illustrated in Figure 2.3.

FED CNT use substantially less power than plasma displays. FED CNT allow for the elimination of the energy-hungry ionization step in PDP by stimulating the phosphors directly with electrons emitted by carbon nanotubes instead of by ultraviolet light.

As in a regular CRT, a cathode is induced to emit electrons, but unlike a regular CRT, field emission does not rely on heating the cathode to boil off electrons. FEDs rely on electric field or voltage induced emissions to excite the phosphors by electron bombardment. To produce these emis-

2.3 Field Emission Display

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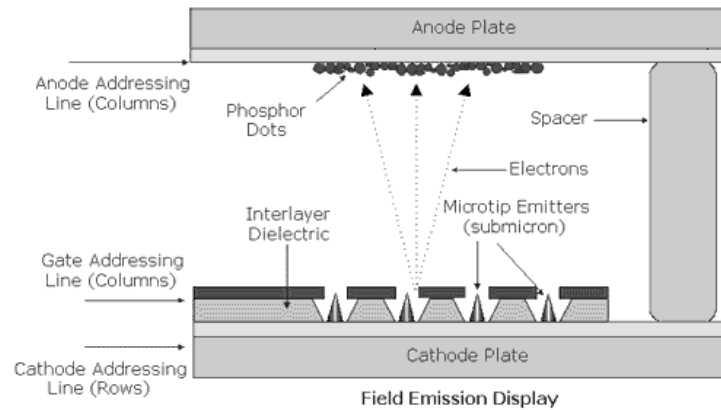


Figure 2.3: Field Emission Display

sions, FEDs use a multiplicity of x-y addressable cold cathode emitters. A large voltage sweeps the emitted electrons through a vacuum towards a positively charged anode just behind the glass face of the display, the rear of which is coated with phosphors that light up when struck, forming a visible image. Due to the fine tip of the emitters, a higher field can be generated for a certain voltage (of the order of kV). The quality of the field emission display depends on characteristics of the electron emission source, such as the material and the structure of the electron emission source.

Due to the cold cathodes, the emitters can be packed close together with their supporting electronics without causing the entire display to over-heat. The assembly of cathodes can then be placed close enough to the glass face of the display. As a result the bulky electromagnetic beam-steering setup used in a CRT can be eliminated.

A FED has advantages of light weight and thin profile and advantages of high brightness and self luminescence, like a CRT. They have a short response time resulting in high quality motion picture without any smearing of the image.

Although physically simple, actual operation of field emitters in a production device are anything but simple. Field emitters depend on high electric field strength to tear electrons from the surface. Instead of very high volt-

ages, FEDs use very small radii atomic lattice size and element spacing for cathodes. This small size renders the cathodes susceptible to damage by ion impact. The ions are produced by the high voltages interacting with residual gas molecules inside the device. FEDs require high vacuum levels which are difficult to attain: the vacuum suitable for conventional CRTs and vacuum tubes is not sufficient for long term FED operation. Intense electron bombardment of the phosphor layer will also release gas during use.

2.4 Surface-conduction Electron-emitter Display

The Surface-conduction Electron-emitter Display (SED) uses a similar flat-panel technology as the FED. It is seen as the simplified variant of a FED. In the SED, the electrons are emitted by a single surface conduction electron emitter behind every pixel. The surface conduction electron emitter apparatus consists of a thin slit across which electrons tunnel when excited by moderate voltages (tens of volts). When the electrons cross the electric poles across the thin slit, some are scattered at the receiving pole and are accelerated toward the display surface by a large voltage gradient (tens of kV) between the display panel and the surface conduction electron emitter apparatus. An illustration is given in Figure 2.4 [4].

2.5 OLED

OLED is the abbreviation of Organic Light-Emitting Diode. It was invented by Eastman Kodak in the early 1980s.

As simply derived from the name itself, an OLED is a specific kind of LED. Light is generated when an electric current passes through. Figure 2.5 shows the structure of an OLED. Between the metal cathode and the anode (Indium Tin Oxide), there is an electron transport layer, a hole injection layer and an emissive layer that consists of an organic material. Upon the anode there is a glass substrate. Manufacturers focusing on flexible OLEDs use another kind of substrate instead [6][7]. The organic material used in the emissive layer is typically a phosphorescent or a fluorescent material. An inherent property of these materials is that they absorb energy of a specific wavelength and re-emit energy at a different wavelength.

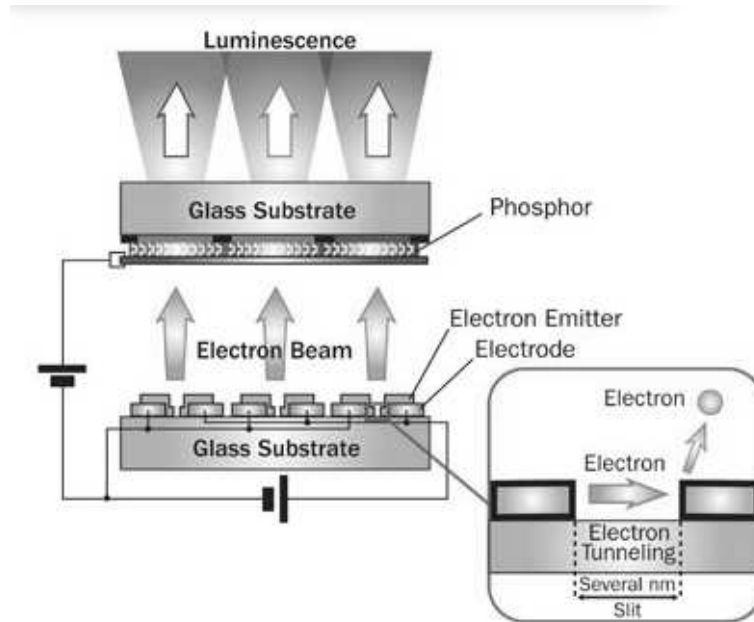


Figure 2.4: Surface-conduction Electron-emitter Display

This property is the key to the operation of an OLED: the emission of a photon when an electron and a hole combine in the emissive layer. To create excitons, electrons are injected via the cathode while holes are injected via the anode. After the injection, they move to the emissive layer where they can combine. To create a full-colour display, a pixel is composed of the basic-colour OLEDs, being red, green and blue. However, not all these colours are equally good. Making blue light is more difficult and less efficient than red or green light. For example, the efficacy (cd/A) of a fluorescent bottom emitting red, green and blue OLED are respectively 5.1, 13 and 4.7 [8]. Another drawback of the organic materials is the limited lifetime.

Also, the intrusion of water into displays can damage or destroy the organic materials. Therefore, improved sealing processes are important for practical manufacturing.

There exist passive matrix monochrome OLED displays (commercialized in 1997) and active matrix OLED displays [9].

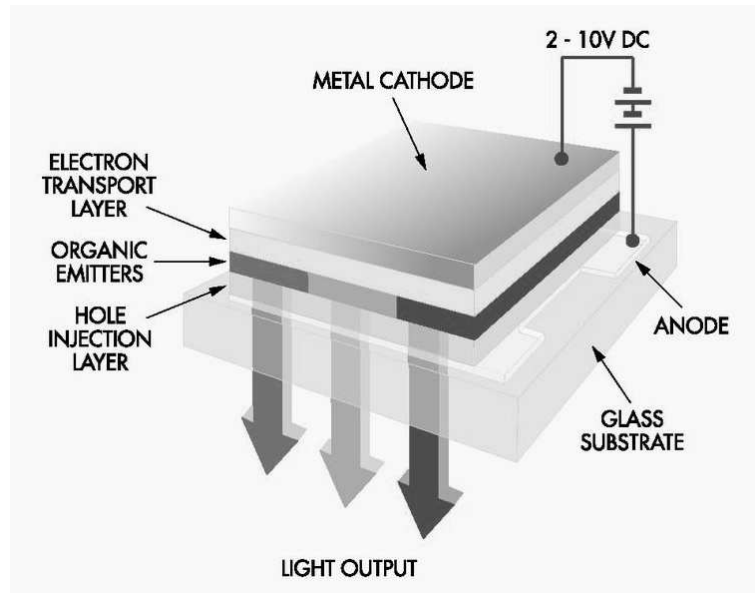


Figure 2.5: Organic Light-Emitting Diode [5]

2.6 Electrophoretic Display

An electrophoretic display is based on the principle of electronic ink [10]. In contrast to the emissive technologies discussed above, electronic ink is a reflective display technology.

Figure 2.6 shows the principle of electronic ink. The display consists of fluid in which little particles are dissolved. There are two kinds of particles: the white particles with a positive or negative charge and the black particles with the opposite charge. The charged pigment particles rearrange when an electric field is applied. Driving the various particles with the right electric field results in the appropriate image pattern.

Another way of building a display with electronic ink is the use of spheres with a white and black side with opposite charges. Due to the electric field the sphere rotates. Because of the large viscosity of the fluid, rather large voltages are needed to separate the black and white particles. The advantage though is that due to the large viscosity, the particles remain in the same place when the voltage is removed. A display with such a feature is called a bistable display. Bistable means that there are two stable

2.7 Electrowetting Display

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How it works

Cross Section of Electronic Ink Microcapsules

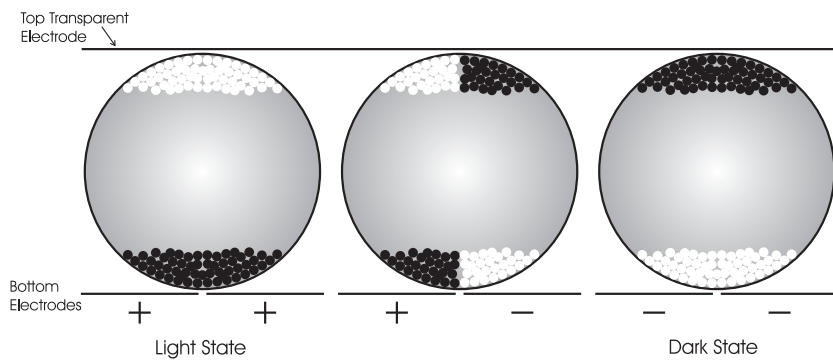


Figure 2.6: Principle of electronic ink

states in which the liquid can be when no voltage is applied.

A colour e-paper is created by adding coloured optical filters. Each pixel consists of three monochrome cells whereby a red, green or blue colour filter is added.

2.7 Electrowetting Display

The working principle of an electrowetting display is similar to that of an electrophoretic display, but instead of using little particles, water and oil are the main actors [11]. Figure 2.7 shows the principle of electrowetting.

In the basic state (without any voltage applied) the hydrophobic coating upon the electrode causes the water to be repelled from the surface, the oil film acting as an intermediate. Yet, when an electrical voltage is applied, the hydrophobic surface becomes hydrophilic and the oil is pushed aside. The creation of a display is achieved by colouring the oil with a dye and so different pixels are independently activated to make an image. Any

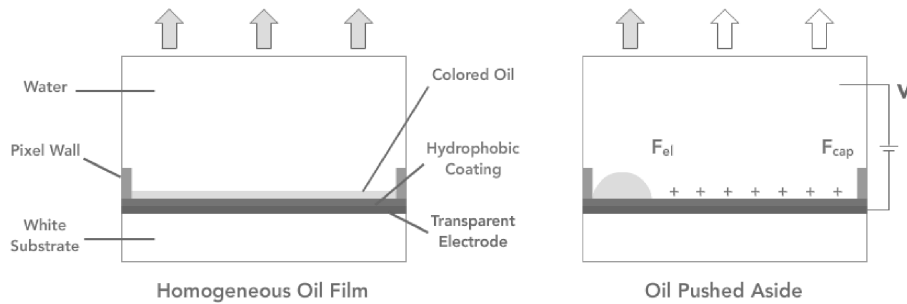


Figure 2.7: Principle of electrowetting

desired colour can be given to the pixels, and therefore every image can be generated on the display.

Research on making this technology bistable is done by the Swiss/German adt group [12].

2.8 Electrochromic Display

Electrochromism is the phenomenon displayed by some chemical species of reversibly changing color when a burst of charge is applied. An Electrochromic Display (ED) usually consists of an active electrochromic (EC) layer that colours and bleaches by the injection or ejection of ions and electrons respectively. There is also a counter electrode (CE) layer storing the ions and an electron-blocking ion conducting layer placed between EC and CE electrodes. At the top and the bottom two ion-blocking electronically conducting layers being connected with electrodes sandwich the above three layers. Figure 2.8 gives an illustration of an electrochromic device. The addition of an extra layer able to hold the charge makes this technology bistable.

Electrochromic Displays are especially suitable for static large-area information displays such as commercial advertising boards where high switching speed is not required [13].

2.9 Liquid Crystal Displays

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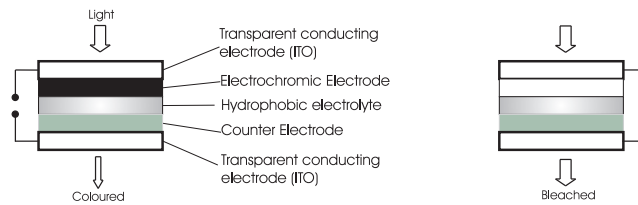
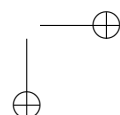
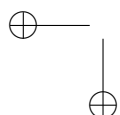
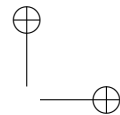
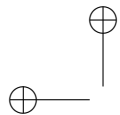


Figure 2.8: Electrochromic device

2.9 Liquid Crystal Displays

Together with plasma displays, Liquid Crystal Displays (LCDs) are the most popular flat panel displays. Each pixel in an LCD consists of 2 electrodes with a kind of liquid crystal between them.

A more profound analysis of LCDs is given in chapter 3.



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Chapter 3

Liquid Crystal Displays

A Liquid Crystal Display (LCD) is a display where each pixel consists of a layer of liquid crystal (LC) molecules aligned between two transparent electrodes. There are different kinds of LC and hence many different types of LCDs. In the past LCDs were used for displays with a limited resolution, but now they overrun the display market. In general, an LCD is a flat panel display with low energy consumption. Therefore they are very useful in portable applications with a limited battery capacity.

The first section of this chapter gives a short explanation of LC. An overview of different kinds of liquid crystal displays along with an explanation of its structure and working principle is given in the second section. The third section compares some different display technologies.

3.1 Liquid Crystals

Liquid crystals are substances that can be in a mesogene phase between liquid and solid. At that point they lose their crystal structure, but neither can move freely. Liquid crystal molecules are often shaped like rods or plates or some other forms that encourage them to align collectively along a certain direction. The complete texture consists of several domains where the LC molecules are oriented in a different direction. The vertical structure is a helical structure in which every molecule is turned a little bit compared to the one below. This is illustrated in Figure 3.1.

Within a domain, however, the molecules are well ordered. Based on the

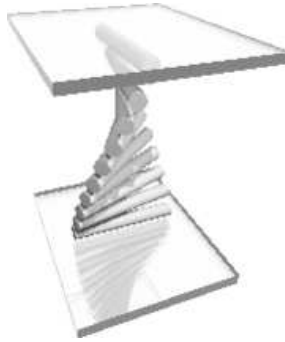
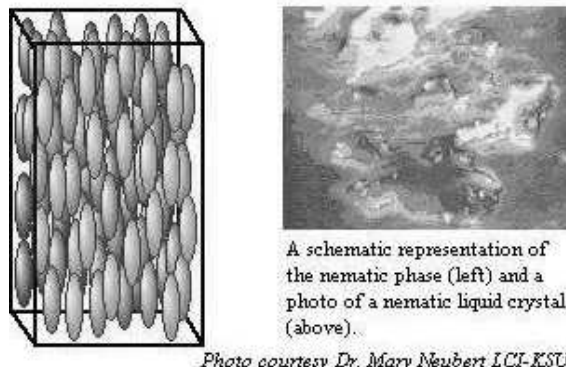


Figure 3.1: Liquid Crystal molecules in a helical structure

molecule structure, the liquid crystals can be divided into three phases: the smectic, the nematic and the cholesteric phase. They are characterized by the type of ordering. In the nematic phase, there is orientational order, but no positional order. This means that the molecules all point in the same direction, but their center of mass positions are randomly distributed. Figure 3.2 gives an illustration of Liquid Crystal in the nematic state.



A schematic representation of the nematic phase (left) and a photo of a nematic liquid crystal (above).

Photo courtesy Dr. Mary Neubert LCI-KSU

Figure 3.2: LC in the nematic state

Orientalional order and positional order in one direction is found in the smectic phase. The molecules are ordered in the same direction and are positioned in several layers. Figure 3.3 shows two different kinds of smectic Liquid Crystal phases.

3.2 Liquid Crystal Displays

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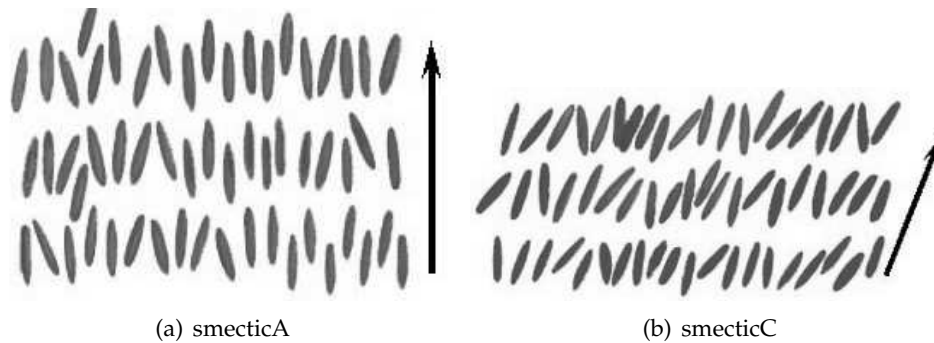


Figure 3.3: LC in the smectic state

In the smectic-A mesophase, the director (the average local orientation of the LC molecules) is perpendicular to the smectic plane, and there is no particular positional order in the layer. In the smectic-C mesophase, molecules are arranged as in the smectic-A mesophase, but the director is at a constant tilt angle measured in relation to the normal of the smectic plane.

The third phase is the cholesteric or chiral phase, where there is orientational order in one layer. Between the different layers, the molecules are twisted along the director, with the molecular axis perpendicular to the director. Cholesteric liquid crystal is explained on page 41.

3.2 Liquid Crystal Displays

There are two common ways to divide the group of Liquid Crystal Displays (LCDs). One is to divide them according to their light source. More specific, whether the display is emissive, reflective or transmissive. Another way is to separate them into active matrix or passive matrix displays. All this will be explained below.

LC is an interesting material to use in displays because the molecular orientation, and hence the material's optical properties, is affected by electric charge. The liquid crystals in the display are able to change the polarization of the incoming light. This means that the amount of light that goes through or is reflected by the LC molecules, determining the pixel gray

value, depends on the voltage over the liquid crystal.

The incoming light can be generated by an artificial light source behind the display. This is called a transmissive display and is used in most flat computer displays for example. When a mirror is used in the LCD-cell to reflect the light coming from the outside environment, the display is reflective. Figure 3.4 shows a schematic cross-section of an LCD where the difference between transmissive and reflective is clearly shown.

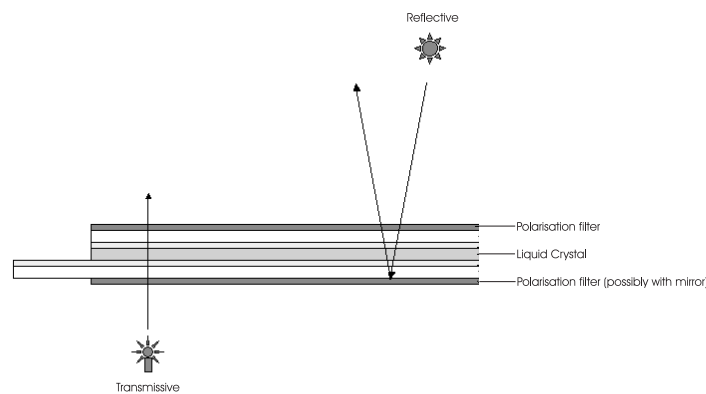


Figure 3.4: Difference between transmission and reflection of light

An example of a reflective display is the display in calculators. A combination of both methods is the transfective display that can use a semi permeable mirror. This is used in cell phones.

A colour display can be made by composing every pixel out of three subpixels that are equipped with a colour filter. The three colour filters are red, green and blue. An other way is to vary the pitch of the subpixels so that only the light with a wavelength corresponding to the pitch length is let through.

The second distinction, being the division between active matrix and passive matrix displays, is the in- or exclusion of an own dedicated transistor and memory cell in every pixel. Figure 3.5 and Figure 3.6 show a schematic

3.2 Liquid Crystal Displays

reproduction of respectively an active matrix (AM) and a passive matrix (PM) display.

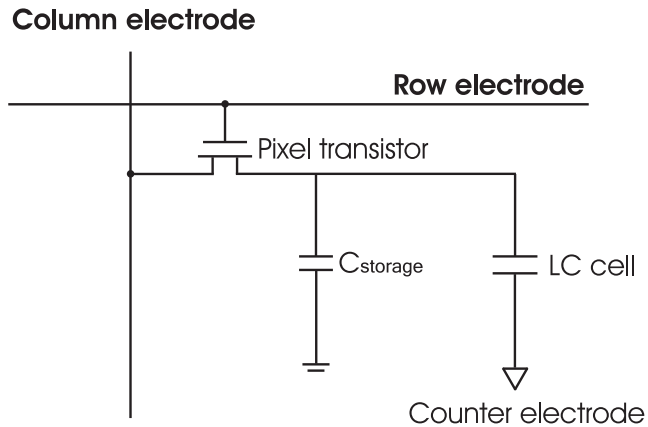


Figure 3.5: Active Matrix

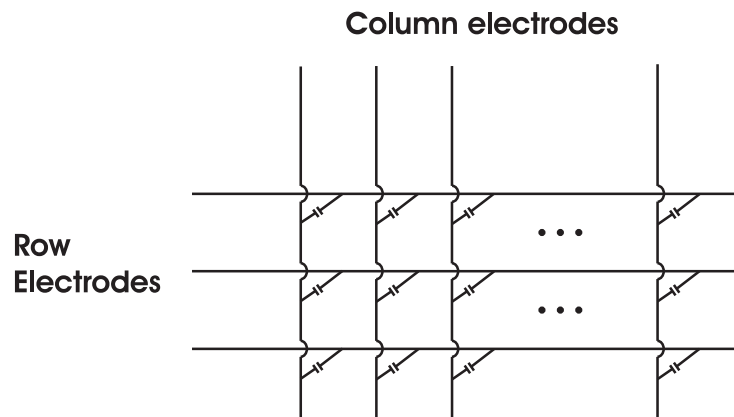


Figure 3.6: Passive Matrix

An active matrix LCD contains a matrix of transistors on the glass (TFT for example) or silicon (LCOS) substrate (TFT and LCOS are explained further on). The source of each transistor is connected to one electrode of a pixel. The other electrode of the pixels is shared by every pixel. The

gate of the transistors is connected to the row of the pixel and the drain is connected to the corresponding column (Figure 3.5). To address a particular pixel, the proper row is switched on, and then a charge is sent down the correct column. Since all of the other rows that the column intersects are turned off, only the capacitor at the designated pixel receives a charge. The capacitor is able to hold the charge until the next refresh.

Due to the lack of these transistors in the PM displays, the liquid crystal pixels are immediately connected with the corresponding row and column electrodes. The voltage across a pixel is determined by the difference between the row and column voltage. The rows and columns are connected to the circuit that controls the driving of the display. To display an image, every row is selected one after another. During the selection of a row, the data signals of the pixels on that row are applied simultaneously to the columns. In contrast to the active matrix driven pixels there is no extra capacitor that can hold the applied voltage during the time the other rows are selected. If the number of rows increases, this type of display becomes less feasible because the contrast between black and white reduces. The gray value of a pixel is determined by the root mean square value of the voltage over the pixel. Very slow response times and poor contrast are typical for passive-matrix LCDs. Yet, they are less expensive to manufacture than TFT LCDs.

The next subsections describe the different types of active and passive matrix LCDs. All LCs that are mentioned below can be used in an active matrix LCD, but not all of them are suitable in a passive matrix LCD. This depends on the electro-optical response characteristic of the LC.

3.2.1 Active Matrix LCD

An inextricable advantage achieved with this kind of driving circuit is the low cross-talk. The addressing electronics can be implemented with thin film transistors (TFT) or with standard CMOS technology. An example of a display in which the liquid crystal pixels are driven by an underlying active matrix fabricated in CMOS, is the LCOS (Liquid Crystal on Silicon) LCD technology. In this case monocrystalline silicon is used. TFT LCDs are engineered using polycrystalline silicon or amorphous silicon technol-

3.2 Liquid Crystal Displays

ogy.

Figure 3.7 illustrates the behavior of the liquid crystals in a Polymer Dispersed Liquid Crystal (PDLC) On Silicon (LCOS) display in case whether or not a voltage is applied over the cell.

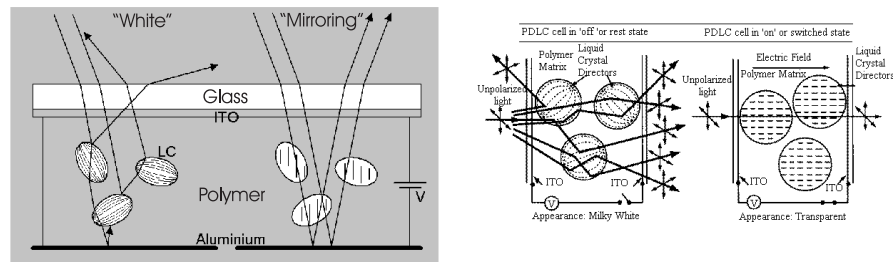


Figure 3.7: PDLC LCOS

Most displays today offer 256 levels of brightness per pixel. A traditional LC used was the Twisted Nematic (TN) LC. To improve on the poor viewing angle and colour reproduction of TN panels, In-Plane Switching (IPS) and Vertically-Aligned Nematic (VAN) LCDs were developed. IPS and VAN are the most commonly used technologies in TFT LCDs this moment. Beside those, there are several derivatives as MVA (Multi-domain Vertical Alignment), MTN (mixed-mode twisted-nematic),... Below, TN, IPS and VAN will be explained.

Twisted Nematic (TN)

The TN LC is naturally twisted and can be untwisted to varying degrees by applying an electric voltage. The rotation of the LC controls the light passage. Figure 3.8 shows the structure of a Reflective TN LCD.

The two ITO electrodes among which the LC molecules are enclosed, are transparent electrodes. The electrodes possess the main feature that they are electrically conductive and optically transparent. On the electrodes, there are microscopic grooves that are in the same direction as the polarizing film. The axes of the two polarizers must be perpendicular to each other. At the rear end of the LC cell, there is also a reflector. In the normal state, the twist of the LCs is aligned with the microscopic grooves on the

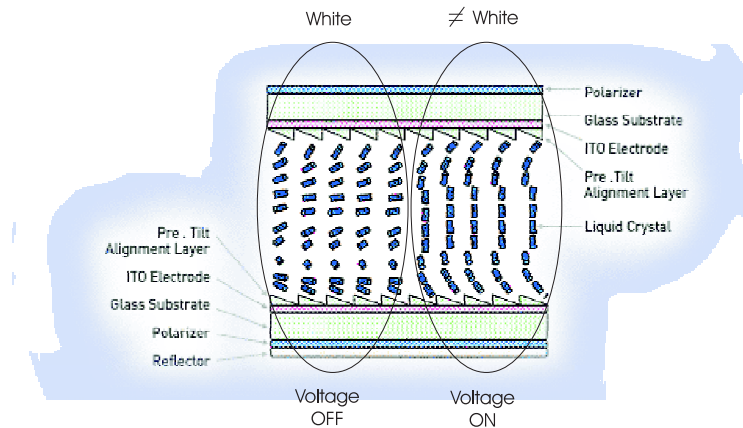


Figure 3.8: Structure of a Reflective twisted nematic liquid crystal display

electrodes. As light strikes the first polarizing filter, it is polarized. Passing through the LC, it is rotated in such a way that it can pass through the second polarizer (polarization angle perpendicular to the polarization angle of the first one) in case no voltage were applied. The second polarizer is also called the analyzer. At the reflective surface at the end the light is sent back to the viewer. This is the basic theory to achieve a white pixel and is illustrated in the left part of Figure 3.8. The right part of Figure 3.8 shows the behaviour of the LC when a voltage is applied over the cell. Depending on the voltage value the LCs will orient more or less parallel to the field. Because of this, not all the light that passed the first polarizer will be rotated over 90 degrees and therefore only part of that light will pass the second polarizer. As a consequence, only part of the light is reflected and the pixel appears gray or black.

The extreme cases black and white are illustrated once again in Figure 3.9 for a transmissive TN LCD.

The second situation in Figure 3.9 shows the molecular structure of the LC when an (sufficiently high) electric voltage is applied to the electrodes. The LC untwists and lines up parallel to the electric field. The polarized light that passes through the LC does not rotate as in the case no voltage is applied and therefore the light is blocked by the second polarizer. As a

3.2 Liquid Crystal Displays

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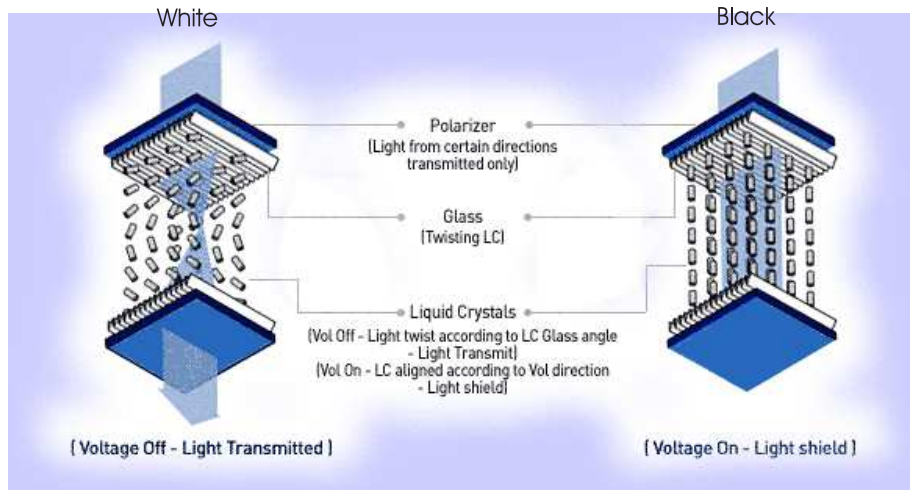


Figure 3.9: TN transmissive LCD: molecular structure in the on and the off state

result, no light is transmitted and the pixel appears black.

By controlling the twist of the liquid crystals in each pixel, the transmission of the exact amount of light that passes through can be varied. Gray-scale modulation is achieved by varying the voltage between the threshold for helix deformation and the saturation voltage.

The response of a typical TN cell to an applied voltage is given in Figure 3.10. Figure 3.10(a) shows the electro-distortional curve that represents the angle of the molecules in relation to the glass plates as a function of the applied voltage. Figure 3.10(b) shows the electro-optical response. This curve shows the percent of light transmitted through the liquid crystal.

To make colour pixels, colour filters are used as shown in Figure 3.11. Each pixel then consists of three subpixels that are created by use of a red, green and blue colour filter.

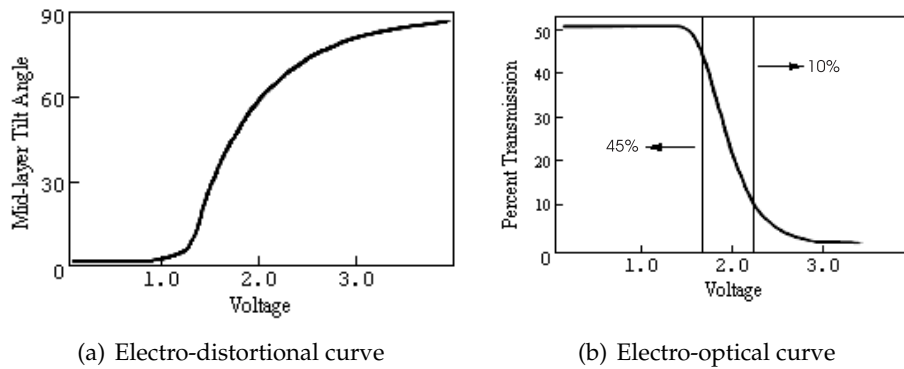


Figure 3.10: Distortional and optical behaviour as function of the voltage over the cell

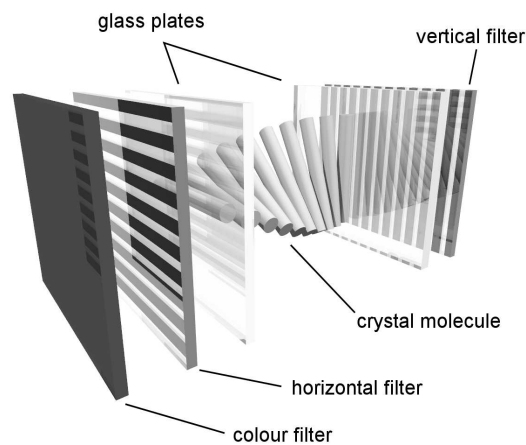


Figure 3.11: Colour filters are used to create a colour pixel

In-plane switching (IPS)

The key difference between TN and IPS is that the applied electric field is horizontal in case of IPS instead of vertical in case of TN. This way the LC molecules are always oriented parallel with the substrate. Usually, the electrodes have a finger structure as shown in Figure 3.12.

The right schematic represents the situation if no voltage were applied.

3.2 Liquid Crystal Displays

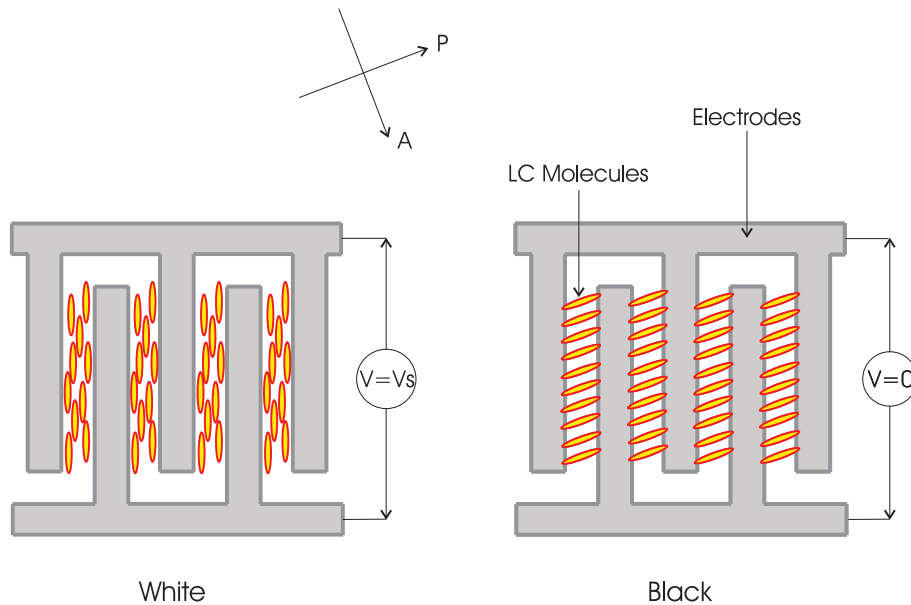


Figure 3.12: IPS LCD, top view.

In case the polarization of the incident light is directed parallel to the LC molecules, only one refractive index is encountered and the light will go through the LC. If the axis of the analyzer were perpendicular to the axis of the polarizer, no light can pass the analyzer and the cell appears black. When a voltage is applied over the cell, the LC molecules will attempt to orient perpendicular to the electric field (if $\Delta\epsilon_{LC} < 0$). This situation is illustrated in the first figure. The incident light now passes a birefringent layer and undergoes a polarization change. Because of this part of or all the light passes the analyzer and the pixel appears gray or white.

The big advantage of IPS compared to TN is the increased viewing angle as shown in Figure 3.13.

A disadvantage of this technology is the reduced aperture ratio due to the electrodes. To achieve the same brightness, the backlight has to send more light making IPS useless in battery-powered applications. Newer technologies use transparent electrodes to resolve this problem.

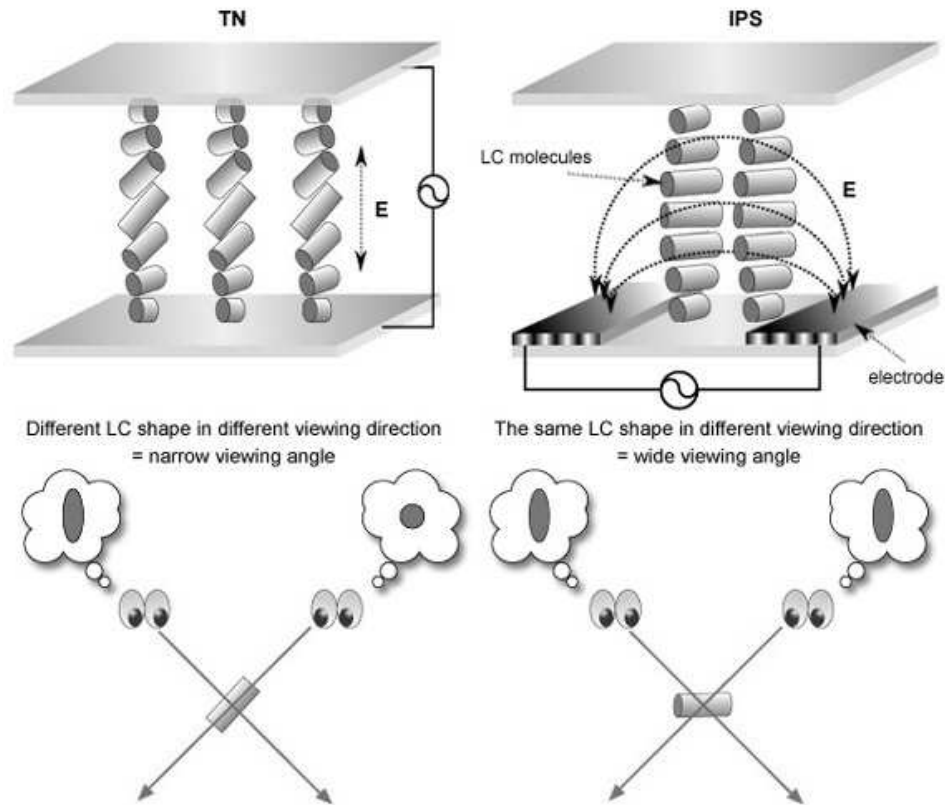


Figure 3.13: Difference in viewing angle between IPS and TN

Vertically-Aligned Nematic (VAN)

In a VAN LCD, a nematic LC is used with the characteristic that it aligns perpendicular to the electric field ($\Delta\epsilon_{LC} < 0$). Consequently it needs to be aligned vertically to the substrate if no voltage were applied. In this case of no voltage, the incident light is blocked by the crossed polarizers and the pixel appears black. When a voltage is applied to the cell, the LCs align themselves with the surface. As can be seen in Figure 3.14 this surface is not smooth, but protrusions are added. This facilitates the tilt and results in the creation of various domains in the cell. The polarization direction of the incident light will now change and depending on the cell thickness and the refractive index, a certain amount of light will pass the cell.

3.2 Liquid Crystal Displays

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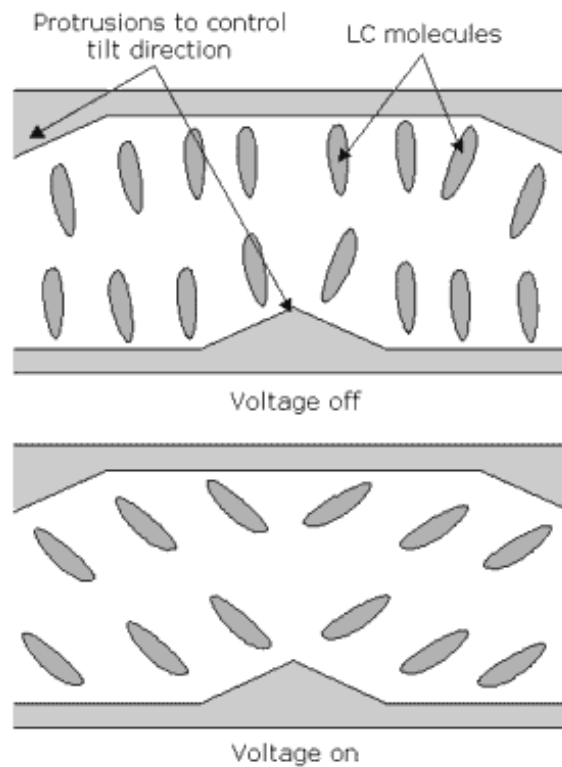


Figure 3.14: Transmissive Vertically-Aligned Nematic LCD cells

The contrast and the viewing angle are as good as the IPS technology (140 degrees in all directions). Even better are the brightness, the power consumption and the response time.

3.2.2 Passive Matrix LCD

Small displays such as those found in PDAs or older laptop screens have a Passive Matrix (PM) structure employing supertwist nematic (STN) or double-layer STN (DSTN) technology (DSTN corrects a colour-shifting problem with STN). Also TN can be used, but is less popular.

Twisted Nematic LCD

The twisted nematic LC, which is used in AM displays, is only limited usable in PM displays when they are set up in a matrix structure. This is so because the difference between the voltage needed to create a white pixel (V_{ON}) and the voltage needed to create a black pixel (V_{OFF}) is too big in case of a TN LC. Because the LC cells have a time-integrated response, the root mean-square (RMS) value of the voltage over the cells determines the condition of the LC cell (all voltages mentioned in this paragraph are RMS values). Consequently, when the number of rows increases, the difference between the RMS value of the voltage over a white and a black pixel cell decreases. Therefore it is necessary to have a liquid crystal that only needs a small voltage difference to switch between the two extreme states. The smaller that voltage difference the more rows that can be added. The relationship between V_{ON} , V_{OFF} and the number of rows N is calculated by Alt and Pleshko [1] and is given by $\frac{V_{ON}}{V_{OFF}} = \left[\frac{\sqrt{N+1}}{\sqrt{N-1}} \right]^{1/2}$. The more common expression is $N_{max} = \left(\frac{V_{th}}{\Delta} \right)^2$. Hereby is $\Delta = V_{ON} - V_{OFF}$ and V_{th} the threshold voltage ($V_{OFF} \leq V_{th}$).

Yet, for low information content numerical and alpha-numerical TN-LCDs as they are required for digital watches, pocket calculators or other simple machine-man interfaces, a matrix structure is not needed. Segmented electrodes are sufficient. All segments are placed on one substrate of the display with a common counter electrode at the opposite substrate and are addressed individually. Obviously, addressing of matrix displays, such as in LCD-screens for computer-monitors or flat television screens, is more complex than with segmented electrodes.

Figure 3.15 shows the general structure of a segment-driven Twisted Nematic LCD.

The first layer of a TN LC cell is the polarizer to polarize the incident light. The second layer is a glass substrate with ITO (Indium Tin Oxide) electrodes. The shapes of these electrodes will determine the dark shapes that will appear when the LCD is turned on or off.

The fourth layer is also a glass substrate with an ITO electrode film. This electrode is common for all the LC cells and has horizontal ridges to line up with the second polarizer (also called analyzer), which is the fifth layer.

3.2 Liquid Crystal Displays

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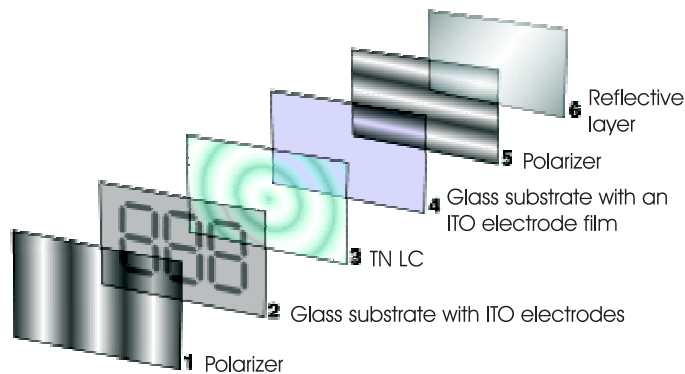


Figure 3.15: General structure of a segment-addressable Reflective TN LCD

Between the two electrodes, the TN LC molecules are comprised. The last layer is a reflective layer that reflects the light that has passed the previous layers.

Super Twisted Nematic LCD

The problem of the too big voltage difference to switch between the two extreme states in TN LCD was solved with the invention of the super-twisted nematic (STN) display. STN displays provide more contrast than TN by twisting the molecules to 180° or 270° instead of to 90° in the TN cell. The electro-distortional and electro-optical curve are shown in Figure 3.16 and Figure 3.17 respectively.

Note that the change in the tilt angle becomes very abrupt as the twist angle is increased. The consequence of this response curve is that the off and on voltages are much closer together.

Although it is desirable to obtain a sharp electro-optic transition, grayscale images require intermediate points along the curve. For this reason, many commercial STN displays use a twist angle of 210° . This broadens the

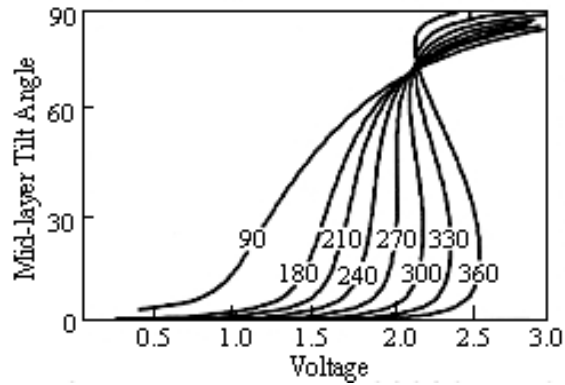


Figure 3.16: Electro-distortional curve STN

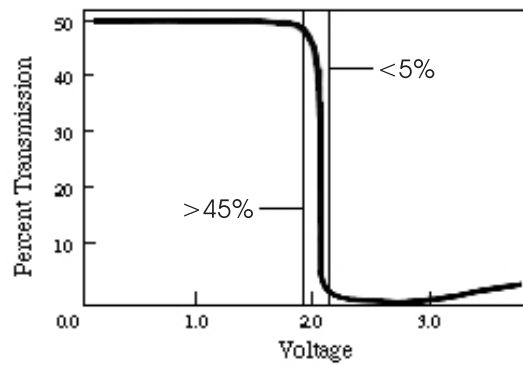


Figure 3.17: Electro-optical curve STN

transition region enough for grayscale while allowing conventional PM addressing.

Double Super Twisted Nematic LCD

Early displays operating in the 210° mode suffered from undesirable colouration resulting from a shifted transmission spectrum of the device. In the ON state, the pixels tended to be yellow, while the OFF state had a bluish-purple tint. In addition to not being popular with the consumer,

3.2 Liquid Crystal Displays

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full colour displays using filters can only be made with black and white operation. This problem was solved by adding a second STN layer with the opposite twist sense to the cell. This type of device is known as the double super-twisted nematic display (D-STN).

In the OFF state, the colour shift resulting from the first layer is compensated by the second layer. This pixel appears black. The ON state is not affected by the second STN layer and white light emerges. Since the two layers consist of the same liquid crystal material, the behavior is constant over the entire temperature range.

Film Compensated Super Twisted Nematic LCD

Film Compensated STN (FSTN) is a passive matrix LCD technology that adds a retardation film to the STN display that compensates for the colour added by the birefringence effect. Hence, it improves the sharpness of the image and provides a higher contrast and wider viewing angle. The film compensating layer is added between the STN display and the rear polarizer. The FSTN technology comes in a single colouration, black characters on a white / gray background. It is more expensive than STN and DSTN, but it has a better viewing angle and contrast than the STN technology. It was used in monochrome laptops before the DSTN method became popular.

Colour Super Twisted Nematic LCD

Colour STN (CSTN) Technology is actually STN technology that uses a white backlight and colour filters to produce the hues required for a colour display.

The original CSTN displays developed in the early 90's suffered from slow response times and ghosting (where lit pixels in a row can affect the unlit pixels). Recent advances in the technology, however, have made CSTN a viable alternative to active matrix displays.

Dual-scan Super Twisted Nematic LCD

In a Dual-scan STN, the screen is divided into halves, and each half is scanned simultaneously, thereby doubling the number of lines refreshed

per second and providing a sharper appearance. DSTN was widely used on earlier laptops.

Bistable Nematic LCD

The problem of the limited possible number of rows is eliminated in bistable passive matrix displays. Bistable means that there are two possible states in which the LC can be when no electric field is applied. Hence, the display content can be held without consuming energy. Examples of bistable passive matrix displays are the Bistable Nematic (BiNem) LCD and the cholesteric texture LCD. The latter is explained in the next subsection.

BiNem^R is a breakthrough technology that enhances existing LCD technologies by providing a memory effect and superior image quality. As mentioned before, bistable means that the image on the display does not change when no power is applied due to its internal memory effect. Nematic refers to the use of nematic liquid crystals which are discussed above.

The BiNem technology is a technology that is fully patented by the French company Nemoptic.

The technology is based on a unique principle called 'surface anchoring breaking'. The meaning of this will be clear later on.

The bistable nematic LC can assume two stable textures [2] [3] which are shown in Figure 3.18.

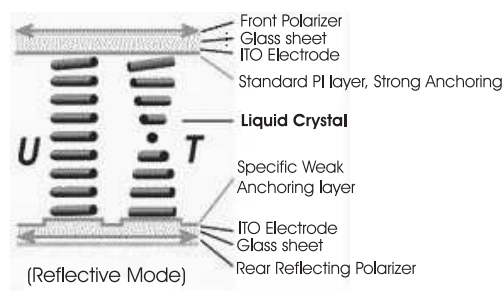


Figure 3.18: Internal structure of a reflective BiNem cell

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These stable states are the Uniform (U) state in which the molecules are parallel along the height of the cell gap and the Twisted (T) state in which the LC is twisted over 180° . Similar as in non-bistable LC, the structure of the LC is induced by the applied voltage over the pixel. However, it is not only the present voltage that determines the optical response, but the total shape and amplitude of the voltage pulse and the state of the LC before the pulse was applied.

When an electrical pulse is applied, the added energy will break the weak anchoring of the molecules on the bottom surface. Next, the LC molecules will arrange themselves perpendicular to the surface and the complete anchoring is broken. Since the anchoring is stronger on the top surface, the molecules above stay anchored. Then, depending on the shape of the falling edge of the pulse, the molecules organize either in U or T state [4]. The transition to the T- and U-state is presented in Figure 3.19.

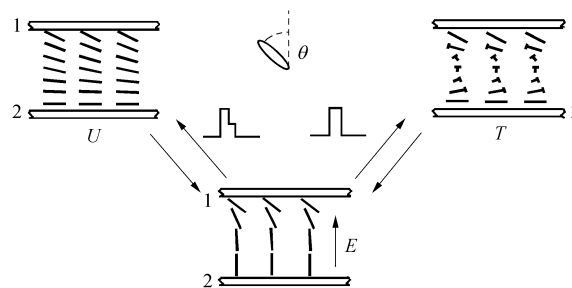


Figure 3.19: BiNem textures and transitions

Once either state is selected, it remains like this forever without consuming any additional power. By adjusting the twist of the liquid crystal molecules, not only black and white, but also grayscale images can be achieved [5].

Cholesteric Texture LCD

Cholesteric LC molecules are a subclass of the nematic LC molecules. Seen in a very thin layer, the cholesteric liquid crystal molecules look like nematic liquid crystal molecules. However, molecules in the different layers orient at a slight angle relative to each other. Figure 3.20 makes this more

clear.

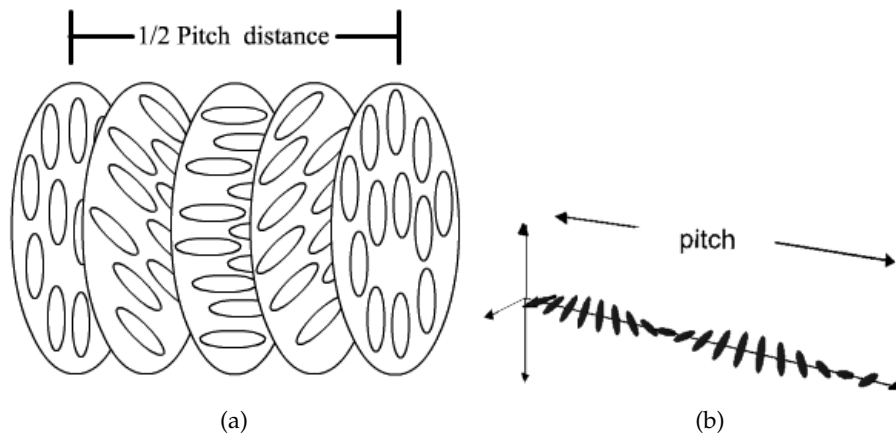


Figure 3.20: Behaviour of the cholesteric liquid crystal molecules

The left picture shows five cross-sections of the LC. The director of the different cross-sections describes a spiral as shown in the right picture of Figure 3.20. The length over which the director undergoes a full 360° twist is called the pitch. The pitch may be varied by adjusting temperature or adding other molecules to the LC fluid. For many types of liquid crystals, the pitch is of the same order as the wavelength of visible light. This causes these systems to exhibit unique optical properties, such as selective Bragg reflection of wavelengths equal to the pitch length, which is an interesting characteristic when it comes to creating displays. By varying the pitch through the visible spectrum, all different colours can be reflected. Increasing the temperature of the molecules gives them more thermal energy causing the angle at which the director changes to be made larger and thus tightening the pitch. Similarly, decreasing the temperature of the molecules increases the pitch length of the cholesteric nematic liquid crystal.

As mentioned before, the cholesteric liquid crystal (ChLC) is bistable. The two stable states that the LC can adopt are the planar state and the focal conic state. There is also a third instable state, the homeotropic state. Figure 3.21 shows the three predominant states of the ChLC molecules.

The first state is the Stable Planar (SP) state. The axis of the director helix is perpendicular to the electrodes. At the surface, the director is parallel to

3.2 Liquid Crystal Displays

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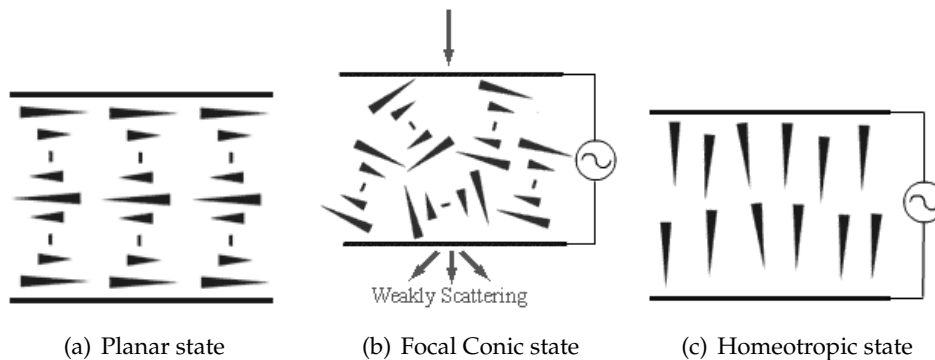


Figure 3.21: Behaviour of the cholesteric liquid crystal molecules as function of the applied electric field

the grooves. As described before, the colour with wavelength corresponding to the pitch will be reflected.

The second state is the Focal Conic (FC) state. In this state, the pitch of the LC molecules is smaller than in the planar state and the light is weakly scattered forward. This light is absorbed and the pixel appears black.

The third state represents the homeotropic (H) structure. This state, in which LC molecules are transparent, is reached when the applied electric field is increased above a certain threshold value. The homeotropic state is not stable and the LC molecules will switch to the SP-state after the electric field is withdrawn. By contrast, the SP and the FC state are stable.

When only a small electric field is applied, the LC cell remains in the same state. A moderate electric field results in the LC cell turning to the FC state.

The reaction of the LC on the applied field is shown in Figure 3.22.

Similar to the BiNem technology, grayscale images can be created. This is realized through the creation of domain structures.

A more profound analysis of Cholesteric Texture Liquid Crystal Displays (ChLCDs) can be found in chapter 4.

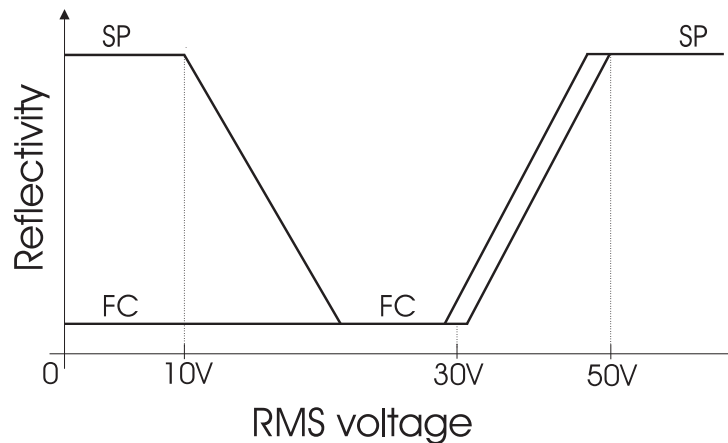


Figure 3.22: Reflectivity of the ChLC as a function of the rms voltage of the applied voltage pulse

3.3 Comparison of the different technologies.

When comparing different display technologies, several elements have to be considered. The most important ones are contrast ratio, brightness, resolution, power consumption, screen dimension, lifetime, price, colour saturation, response time and viewing angle.

First the main players on the market, CRT, LCD and PDP are discussed. Then, a comparison will be made with some other technologies.

3.3.1 CRT

At the end of the sixties, the CRT started to enter peoples living room. In the nineties practically every household had one. Nowadays, some friends or family members have traded this CRT for an LCD or plasma television. Not necessarily because the latter have a better image quality, but because they have the huge advantage of being slim and able to reach bigger display dimensions. Analysts predict that by the end of 2008, CRT televisions would still enjoy a 70% market share. Slimmer CRT televisions

3.3 Comparison of the different technologies.

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are being developed in order to challenge the flat-panel display technologies at their most appealing characteristic - being slim. CRT display tube manufacturer LG.Philips has developed a super slim CRT design that drastically reduces the average depth of the tube device. In addition, the tube is re-designed such that the tube-based set would look like a flat-panel TV from the front.

Looking at the price, a CRT costs half as much as an LCD or PDP. Moreover, CRT has one of the best pictures you can get from a video display device. Not even the latest top plasmas can rival conventional cathode ray tube displays for black depth and contrast.

While CRTs are capable of displaying multiple video resolutions without introducing defects, LCD display quality reduces when images are scaled to another resolution than the native resolution ratio.

On the other hand, the lifetime¹, which is about 20 000 hours and the brightness, is less than for LCDs. Moreover, they consume more power and are prone to screen flicker.

3.3.2 LCD-PDP

Until quite recently, the superior brightness, wider colour range and wider viewing angle of colour plasma displays, compared to LCD displays, made it one of the most popular ways of displaying HDTV. However since then improvements in LCD technology have closed the gap dramatically. The lower weight, price, and power consumption of LCDs have ensured them a place in the former plasma market.

Table 3.1 shows the significant differences between a 42 inch LCD and Plasma (PDP) TV nowadays. This information is partly from the website of CHIMEI, which is now one of the two largest TFT-LCD manufacturers in Taiwan and one of the four leading TFT-LCD manufacturers in the world, and partly from commercial LG-Philips products.

At the smaller end of the scale - 37 inch to 42 inch, plasma displays support a lower resolution than an equivalent LCD screen. Moreover, LCD has a power consumption advantage over PDP.

LCD displays generally have a lower contrast ratio in a dark environment

¹The lifetime is defined as the time taken for the brightness to drop to half the default value

Table 3.1: Comparison between LCD and PDP

	42" PDP	42" LCD
Resolution	1024x768	1366x768
Power consumption	385W	240W
Brightness	1200cd/m ²	500cd/m ²
Contrast		
Dark environment (< 1 lux)	3000:1 (peak)	1000:1
Bright environment (250 lux)	10:1 (peak)	250:1
Colour Saturation	95% NTSC	75% NTSC
Response Time	3ms ²	8ms
Viewing Angle	Up to 175°	Full viewing angle 85°
Burn-In	Serious	Immune
Life expectancy	30 000 hours	50 000 hours

than a plasma display or CRT. In a bright environment, the LCD performs better than the PDP. This according to CHIMEI.

The brightness of the image and the colour saturation, which is a measurement of the colour purity measured as a percentage of the NTSC standard of 100, is greater in plasma displays.

Older LCDs had longer response times than their plasma and CRT counterparts, creating ghosting when images rapidly changed. This drawback is continually improving as the technology progresses and is almost imperceptible in current LCD Computer Displays and TVs. Newer LCDs have response times of approximately 8ms, the exact response time varying according to the type of panel and manufacturer.

LCD display panels have a limited viewing angle, thus reducing the number of people who can conveniently view the same image. As the viewer moves closer to the limit of the viewing angle, the colours and contrast appear to deteriorate. PDPs as well as CRTs support a viewing angle of up to 175° with no colour shift. However, for some applications like bank terminals or using a laptop in a public place, the limited viewing angle of the LCD can be an advantage.

The problem of limited viewing angle in LCDs is eliminated by TFT-LCD manufacturers with the invention of several wide-angle technologies, such as TN+Film, MVA and IPS, which result in excellent images for wide

3.3 Comparison of the different technologies.

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viewing angles. CHIMEI, for example, uses an exclusive combined technology with the intention to achieve a viewing angle of up to 178° .

LCD screens occasionally suffer from image persistence, which is similar to screen burn on CRT monitors. This is becoming less of a problem as technology advances, with newer LCD panels using various methods to reduce the problem. Sometimes the panel can be restored to normal by displaying an all-white pattern for extended periods of time. For PDPs on the other hand, burn-in used to be a big problem. This is due to the physical properties of phosphor and how it reacts to light and electric impulse. Thanks to much research in the past years, some manufactures now claim that PDPs have the same burn-in resistance and susceptibility as CRTs. Though, it’s still smart to avoid static images on your screen. On the other hand, LCD displays may have dead pixel problems which are rare with PDP.

3.3.3 Comparison of other Flat Panel Displays with LCD/PDP

As mentioned in chapter 2, FED and SED are two technologies with CRT-like qualities. They exhibit fast response time and high efficiency, brightness and contrast ratio [6]. The power consumption of FEDs is less than for LCDs or PDPs. The total cost of a FED can also be lower because fewer components are needed. Another advantage is that FEDs do not display dead pixels like LCDs because of emitter redundancy. They are also more flexible than LCD when it comes to handling non-standard resolutions. However, FEDs are not yet commercial. There are still some technical issues.

SED is considered to be the variant of FED that is currently feasible to mass-production. Toshiba announced to mass-produce the SED TVs in cooperation with Canon by 2008. In a dark room, SED can reach a contrast ratio of 50000 : 1 (according to some sources, Toshiba’s final versions of SEDs will enter the market with a contrast ratio of 100000 : 1). The response time is $1ms$ and the brightness is about $450cd/m^2$. Similar to PDP, SED is also susceptible to burn-ins.

Another technology that is beginning to replace LCD technology in hand-

held devices such as PDAs and cellular phones is the OLED technology. One of the great benefits of an OLED display over the traditional LCD displays is that OLEDs do not require a backlight to function. This means that they require far less power and, when powered from a battery, can operate longer with the same charge. A second disadvantage of the LCD backlight is the incapability of showing true black, while an “off” OLED element produces no light (and hence consumes no power). In LCDs, energy is also wasted because the liquid crystal acts as a polarizer which filters out about half of the light emitted by the backlight. It is also known that OLED based display devices can be more efficiently manufactured and hence have a significantly lower cost than liquid-crystal and plasma displays [7].

The range of colours, brightness and viewing angles possible with OLEDs are greater than that of LCDs because OLED pixels directly emit light. Because of this, OLED pixel colours appear correct and unshifted, even as the viewing angle approaches 90° from the axis perpendicular to the display.

However, degradation of OLED materials has limited the use of them. Particularly, blue OLEDs have lifetimes of around 5000 hours when used for flat panel displays. However, it is possible to extend the lifetime to 20000 hours. The lifetime of an OLED largely depends on the luminance. Another drawback is that the intrusion of water into displays can damage or destroy the organic materials. Therefore, improved sealing processes are important for practical manufacturing and may limit the longevity of more flexible displays.

The fact that OLEDs can be printed onto flexible substrates opens the door to new applications such as roll-up displays or even displays embedded in clothing.

Not only OLED has a future in flexible electronics, another technology that received media attention recently, is E-Ink. The big advantage of Electronic Paper Displays (EPD) is their characteristic of paper-like high contrast, the ultra-low power consumption (EPD is a non-volatile reflective display) and their thin, light form. The first commercial product using an EPD is the SONY LIBRI. This product, launched in April 2004 in Japan, is an electronic reader utilizing an E Ink Imaging Film EPD.

3.3 Comparison of the different technologies.

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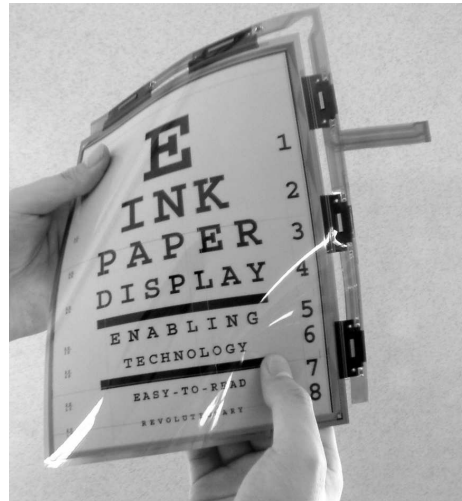


Figure 3.23: A prototype electronic paper display, using E Ink’s Electrophoretic Imaging Film

3.3.4 Comparison of the different LCD technologies

Depending on the application, there is the choice between a PM or AM LCD. PM displays have a much slower response time than AM displays. This causes ghosting and so PM displays can not be used in video applications. AM displays are also much brighter and sharper than passive-matrix displays of the same size, producing much better images. AM driving of displays also allows a bigger pallet of gray values. Especially with a growing number of rows, non-bistable PM displays become useless. On the other hand, they are much cheaper than AM displays. A well known application in which a PM display is used, is the Nokia 6800 gsm (Figure 3.24).

PM driving of displays with an increasing number of rows is possible when a bistable LCD is used. An application with a bistable nematic (BiNem) LCD is shown in Figure 3.25, a palm fabricated by Nemoptic. Furthermore the BiNem technology has a very high optical performance level: excellent contrast, very wide viewing angle, pure Black and White and a large number of colours.

When it comes to AM Displays, IPS and multi-domain VAN are commonly



Figure 3.24: The Nokia 6800 gsm has a PM diplay



Figure 3.25: BiNem LCD

used because of their improved viewing angle. Figure 3.26³ presents the S-IPS (Super In Plane Switching) based LCDs used by LG, Philips and compares them with VAN LCDs.

As can be seen in the figure, S-IPS exhibits little change in contrast ratio from almost any viewing angle and has virtually no colour shift. Multi-domain VAN LCD TVs are used by Samsung for example.

³http://www.lgphilips-lcd.com/homeContain/jsp/eng/tech/tech301_sips.j.e.jsp

3.3 Comparison of the different technologies.

01. Color Shift of Viewing Angle



02. Best Display Quality

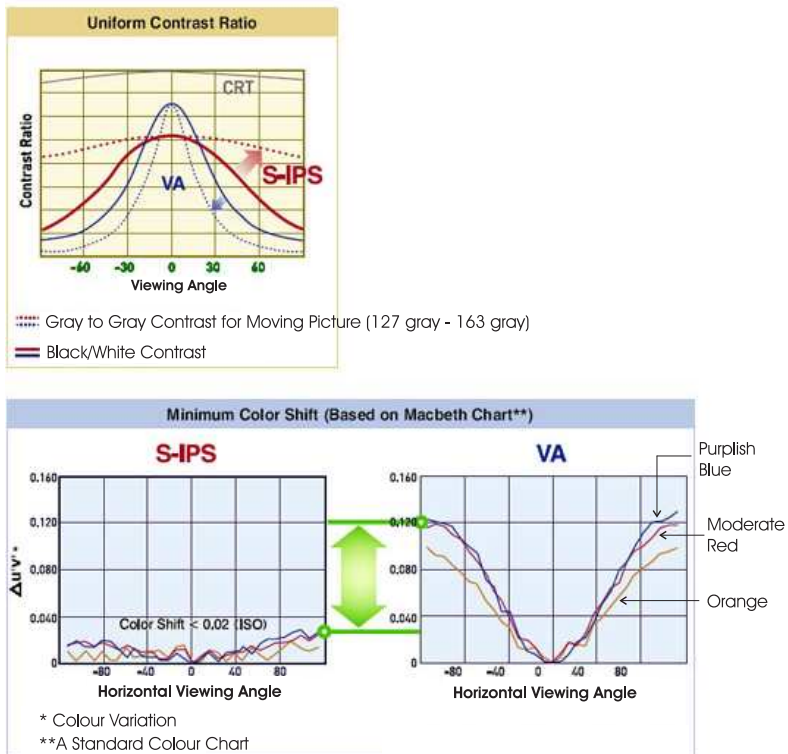
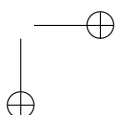
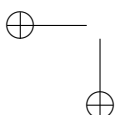
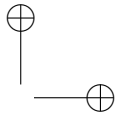
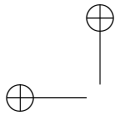
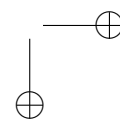
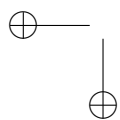
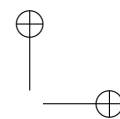
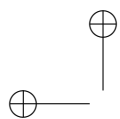


Figure 3.26: VA mode and IPS mode to improve the viewing angle of LCDs



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Chapter 4

Cholesteric Texture Liquid Crystal Displays

In section 3.2 a division of some different kinds of LCDs was made based on the way they are driven (AM or PM). Another distinction between different LCDs is their type of light source. Computer displays for example have a backlight that generates the light being sent through or blocked by the pixels. Back-lit displays however are inefficient because the backlight consumes a lot of energy which undoes the merits of LCDs, their low drive power requirements in particular.

This drawback in transmissive displays is eliminated in the reflective displays which will be a major display technology in the future. Reflective displays can use a front-light or, even better, the light from the environment. Bistable cholesteric texture (BCT) reflective displays are a prime candidate for such a technology that uses no artificial light source. Using Bragg reflection, no color filters or polarizers are needed. The BCT reflective display has a high contrast, excellent sunlight readability, unlimited multiplex ratio, plastic substrate compatibility, high resolution capability, gray scale and full color, has a wide viewing angle and is bistable. A bistable device can retain an image without the need of a power supply. The liquid crystals have two stable orientations (corresponding to "black" and "white") and power is only required to change the image. In this chapter, the Cholesteric Texture Liquid Crystal Displays are discussed in more detail. First, the physical aspects like how the LC reorganizes as a function of the applied voltage are analyzed after which some different

driving principles are discussed.

4.1 Physical aspects of the ChLCD

A brief explanation of how a ChLCD works, is already given in section 3.2.2. The Cholesteric LC, also called chiral nematic LC, is described as a subclass of the Nematic LC. The special characteristic of the ChLC molecules is that the director, to which the liquid crystals line up, rotates in space. Figure 3.20 shows the helical pattern that arises when the LC molecules undergo their 360° twist. The twisting of the molecules is known as chirality.

Some more information about the director of the LC molecules, the twisting of the molecules and how they react as a function of the applied voltage is explained in this section. Once the behavior of the LC molecules is known, we can start to create images by applying the correct voltage waveforms over the electrodes of the LC cells.

4.1.1 Relaxation to the Planar and Focal Conic state

When no voltage is applied to the electrodes of the cell, the LC molecules maintain their structure. There are two stable states which are the Focal Conic (FC) and the Stable Planar (SP) state. In the latter, the LC molecules line up vertically as shown in Figure 4.1.

This reflective state has an intrinsic twist with equilibrium pitch P_0 . The helical axes are (on average) perpendicular to the substrates. This periodicity causes a Bragg reflection with wavelength $L_0 = \langle n \rangle P_0$, where $\langle n \rangle$ is the average index of refraction [1].

By applying an electric voltage to the electrodes, the LC molecules change direction, allowing the display to switch between the reflecting state and the non reflecting state. Which of these two states will be the result, depends on the value of the applied voltage. A medium voltage will make the spiral shaped LC molecules turn horizontally. The horizontal state is maintained even after the voltage is turned off (Figure 4.2).

This state is the second stable state and is called the Focal Conic (FC) texture. The twist of the molecules is the same as in the Planar texture, P_0 . Since all the incoming light will pass through the LC cell, no light

4.1 Physical aspects of the ChLCD

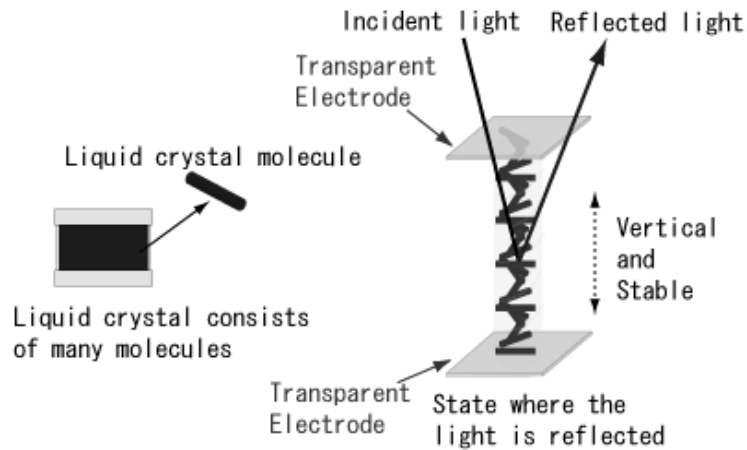


Figure 4.1: Spiral structure of the LC molecules, SP state

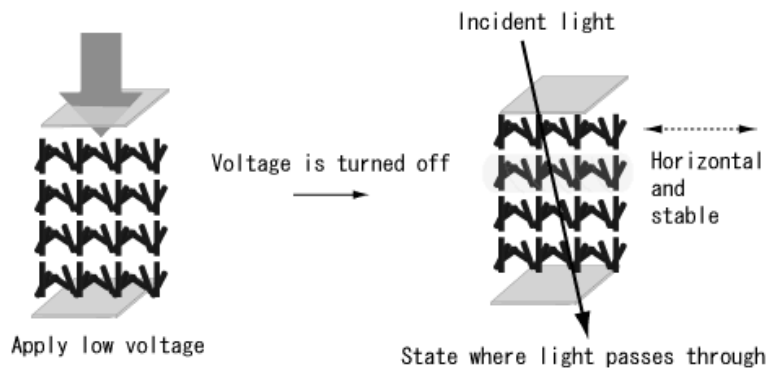


Figure 4.2: Structure of the ChLC cell when a low voltage is applied, FC state

is reflected when the rear substrate is painted black. Hence the LC cell appears dark.

In case a white pixel is wanted, the LCs have to line up vertically again. This transition to the SP state happens in four phases [2] [3] and is illustrated in Figure 4.3.

First, a sufficiently high voltage is applied over the pixel electrodes. The

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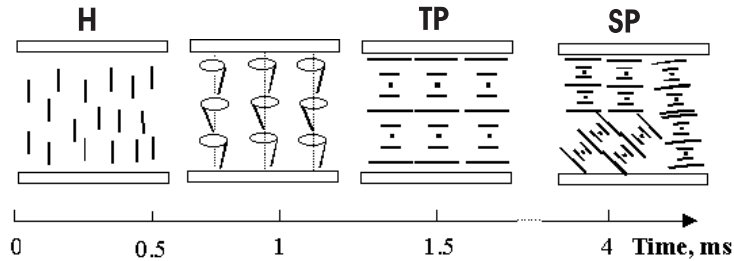


Figure 4.3: Transition from the Homeotropic to the Planar state

induced electric field will make all the LCs untwist and align the director perpendicular to the substrate. This state is known as the Homeotropic (H) state. Secondly, the voltage is withdrawn and the director relaxes in a one-dimensional (monodomain) conical fashion to a Transient Planar (TP) state. This transient planar state is very similar to the equilibrium (reflecting) planar state, except that it has a much longer pitch, and therefore reflects in the near infrared rather than in the visible region. The helical axis of the transient planar state is generally along the cell-normal direction.

Because it does not exhibit the equilibrium value of twist, the TP state has a high elastic free energy. It is energetically desirable for it to transform to a more highly twisted structure. This pitch change can be observed and reaches its equilibrium value in about 4 ms. As the pitch is changing, several other changes are observed to take place. First, the helical axes of the material take on a very wide angular distribution. More specifically, reflecting helices become oriented at angles away from the cell-normal direction. At the same time, the liquid crystal forms a domain-divided structure rather than its initial monodomain state. The more varied the angle of the helical axes, the wider the viewing angle. This is because the reflected light is distributed over a broad range of angles.

In a ChLCD, the stabilized domains of the Stable Planar (SP) texture coexist with domains of the FC texture. The relative percentage of the domains in the SP state determines the amount of light that is reflected and hence the gray-value of the corresponding pixel.

By composing every pixel of three subpixels with a pitch corresponding to the wavelengths of green, red and blue respectively, a color display with

4.1 Physical aspects of the ChLCD

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a certain range of gray-values can be made. Yet, a much higher reflection intensity is achieved by composing the display of three stacked cells with each cell corresponding to one of the basic colours [4].

4.1.2 Composition of the voltage waveforms to drive a display

A rough conclusion so far is that a low voltage over the pixel electrodes results in a dark pixel, a high voltage in a reflecting pixel. The exact value of the 'low' and 'high' voltage depends on the kind of cholesteric LC. The information needed to drive the display, is given by the electro-optical response curve of the LC showing the reflectivity of the LC as a function of the voltage applied over the cell. When removing the electric potential, the LC material relaxes to a certain state of which the reflectivity is determined by the electro-optical characteristic. As an example, the electro-optical response of Polymer Stabilized Cholesteric Texture LC used by Kent Displays is given in Figure 4.4 [5]. This kind of LC has the merit of a wide viewing angle due to the dispersed polymer in the LC that disturbs the orientation of the helical axes. The reflectivity of the cell was measured after a time delay of approximately 1 second following the pulse.

Because the relaxation of the LC also depends on the original state of the LC (SP or FC), the electro-optical characteristic consists of two curves. In Figure 4.4, this is represented by the two curves A and B.

An important characteristic of ChLC is that it does not withstand a DC-voltage. Due to the permanent polarisation the molecules will be pulled apart as it were. Hence, every applied voltage has to be succeeded by a voltage of the same absolute value and duration, but opposite sign. Figure 4.4 thus gives the response of the LC after a single AC pulse is applied over the cell electrodes. Curve A shows the reflectivity in case the cell is originally in the reflecting state, curve B in case the cell is in the FC state before the pulse is applied.

If the voltage of the applied pulse is below V_1 , the cell retains its original state. Starting from the SP state, a voltage higher than V_1 will result in a decreasing reflectivity approximately linear with increasing voltage of the pulse in the region between V_1 and V_2 . Between V_2 and V_3 , the voltage pulse drives the cell into the FC state. Above V_3 the reflectivity rises again until the maximum value, corresponding to V_4 , is reached. When

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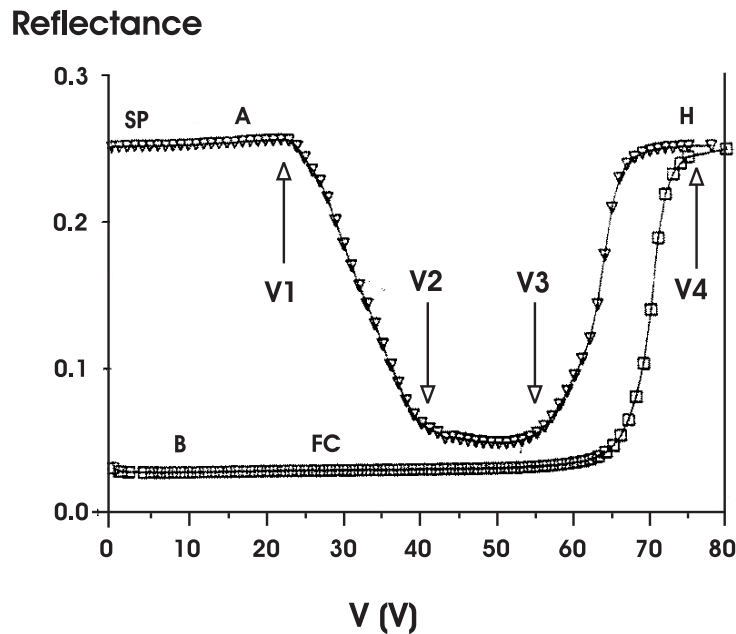


Figure 4.4: Electro-optical characteristic of the PSChT cell to a single ac voltage pulse

applying a voltage above V_4 , the LC molecules will return to the SP state when the voltage is withdrawn and the reflectivity of the cell remains at its maximum.

A cell originally in the FC state maintains its low reflectivity till a pulse with an amplitude of more than V_3 is applied. Above V_3 the reflectivity curve has approximately the same shape as the curve of the LC originally in the SP state.

Both the amplitude of the voltage pulse and the duration of the pulse determine the evolution of the LC.

Figure 4.5 illustrates the influence of the pulse width on the reflectivity of a LC cell for a cell originally in the SP state.

As the pulse width is decreasing below $10ms$, the contrast of the cell is getting smaller because the minimum reflectivity is increasing. Starting from the FC state, a smaller pulse width requires a higher voltage for transfer-

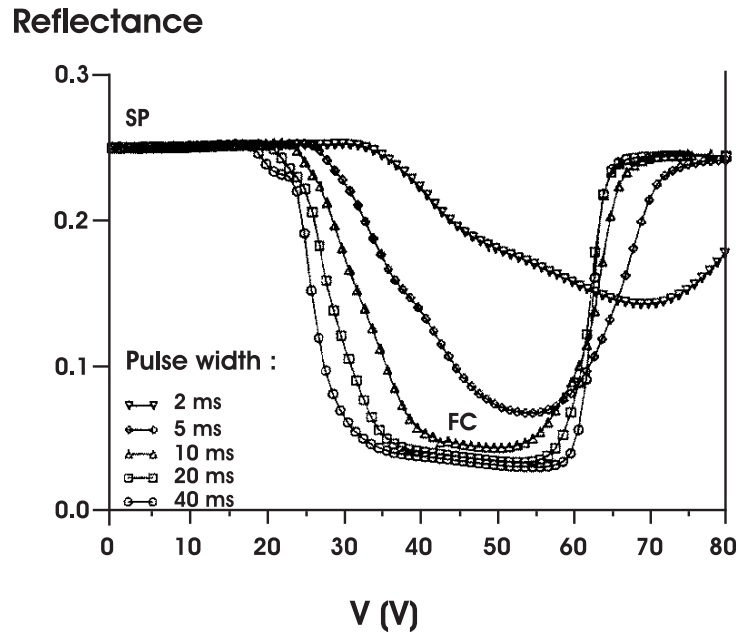


Figure 4.5: Influence of the pulse width on the reflectivity of a LC cell, cell originally in the SP state

ring to the SP state (see Figure 4.6). Pulses shorter than $2ms$ result in no change at all. The disadvantage of a pulse width that is too high is that the slope of the graphic becomes too steep and hence it is more difficult to obtain a big range of gray values.

Starting with this information, a drive scheme for the display can be developed.

4.2 Drive schemes for a ChLCD

A ChLCD is a PM display meaning that the resulting pixel voltage is the difference between the row voltage and the column voltage. Every row is selected one after another. When a row is selected, the column voltages for the corresponding pixels are applied simultaneously. To the other rows, the row non-select voltage is applied.

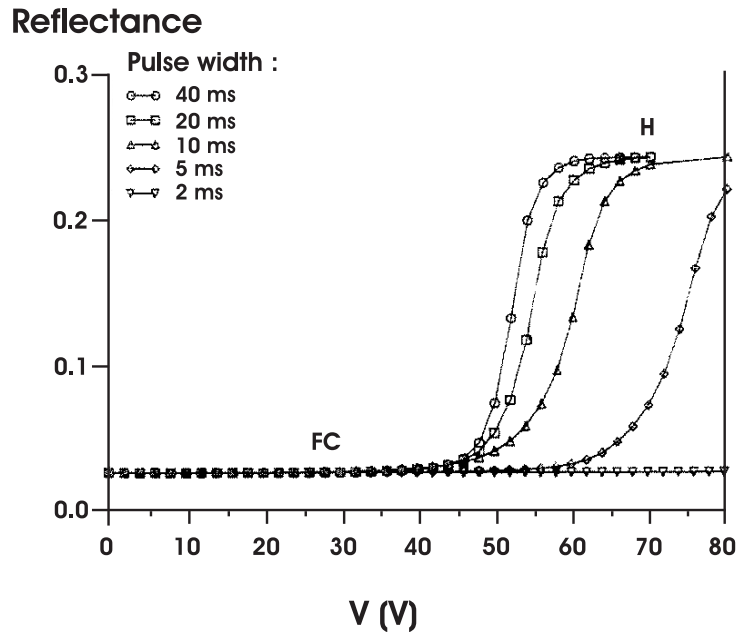


Figure 4.6: Influence of the pulse width on the reflectivity of a LC cell, cell originally in the FC state

Dependent on the application, there is the choice between a conventional and a dynamical drive scheme.

4.2.1 Conventional drive scheme

The term 'conventional' refers to the fact that the state of the LC depends on only one long-duration AC pulse. A conventional drive scheme is pretty straightforward. The AC-pulse corresponding to the wanted state of the pixel is applied over the pixel electrodes. The only condition is that the voltage over the pixels in the non-selected rows is less than V_1 (Figure 4.4) so the liquid crystal in those cells does not switch to another state. Different drive waveforms can be composed. Hereinafter, two examples are given. In the first one the gray values are obtained by using the falling slope of the electro-optical characteristic, the second example uses the rising slope.

4.2 Drive schemes for a ChLCD

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Drive scheme corresponding to the falling slope of the electro-optical response curve

An initial reset that puts the display in the reflecting state is needed to generate the different gray values unambiguously. First a pulse of amplitude V_4 is applied over the pixels. The other demands are

1. To obtain all the gray levels, the range of the pixel voltage must be between V_1 and V_2
2. The pixel voltage over the non-selected cells must be lower than V_1

If the voltage of a **non-selected row** is chosen to be $0V$, previous conditions can be written as follows (see Figure 4.4):

1. $V_R - V_{C1} = V_1$
2. $V_R - V_{C2} = V_2$
3. $|V_{C1}| < V_1$
4. $|V_{C2}| < V_1$

In this formulas, V_R corresponds to the row selection voltage, V_{C1} to the column voltage corresponding to white and V_{C2} to the column voltage corresponding to black.

In the first two equations, there are three unknown parameters. So one parameter can be chosen. Choosing $V_{C1} = 0V$ includes that $V_R = V_1$ and $V_{C2} = V_1 - V_2$. The presupposed demands are fulfilled if $|V_1 - V_2| < V_1$. Varying the column voltage between V_{C1} and V_{C2} generates the complete range of gray values.

Drive scheme corresponding to the rising slope of the electro-optical response curve

A similar principle is used to compose the drive waveforms based on the second slope. Let's take a row non-selection voltage of $0V$ once more. In this case, the demands are:

1. $V_R - V_{C1} = V_4$

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2. $V_R - V_{C2} = V3$
3. $|V_{C1}| < V1$
4. $|V_{C2}| < V1$

Another way of choosing the voltage values can be done by minimizing the amplitude of V_{C1} and V_{C2} . In that case, V_R corresponds to the voltage in the middle of the rising slope, so $V_R = \frac{V3+V4}{2}$. The corresponding column voltages are $V_{C1} = \frac{V3-V4}{2}$ and $V_{C2} = \frac{V4-V3}{2}$. These waveforms are presented in Figure 4.7. The first waveform is the row-select waveform. Every row is selected one after each other. During the selection of one row, the other rows are a constant 0V voltage. To ensure that the optical response of the pixels on the non-selected rows does not change, the condition $\frac{V4-V3}{2} < V1$ has to be fulfilled.

Both slopes have their merits and demerits. The advantage of the falling slope is the good uniformity and the big range of gray values. But, the drawback is the relatively slow response time. The rising slope is much faster and has a better contrast, but less uniformity and less gray levels. In this Ph.D. the rising slope is used to create images.

Figure 4.5 and Figure 4.6 indicate that a line time, the time during which one row needs to be selected, of at least 10ms is needed to obtain a good image quality.

4.2.2 Dynamic drive scheme

A faster response time can be achieved by using a dynamic drive scheme. By composing the line-select waveform of a sequence of several shorter pulses and addressing the lines with a kind of pipeline mechanism, the time to refresh a display can be significantly reduced. At the Kent State University, a dynamic drive scheme has been developed that is able to update a 1000 line bistable cholesteric display in approximately 0.05 seconds [6]. The waveform is shown schematically in Figure 4.8.

The drive scheme is composed of five phases: preparation, post-preparation, selection, post-selection and evolution. The selection phase that takes 50μs determines the behavior of the LC after the addressing.

4.2 Drive schemes for a ChLCD

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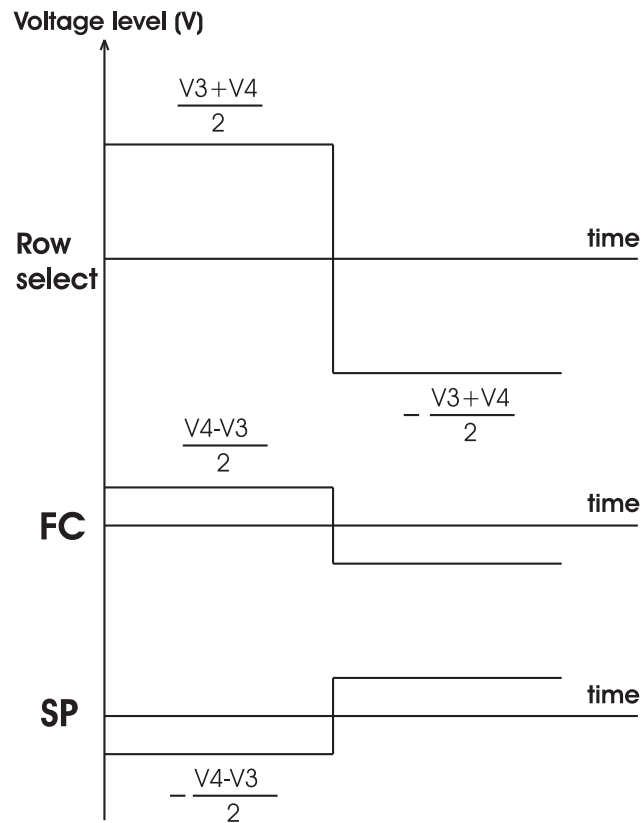


Figure 4.7: Example of a conventional drive scheme, the non-selected rows are at 0V.

In the preparation phase, the voltage is chosen so that the LC will switch to the homeotropic state. Diminishing the voltage sufficiently low, as done in the post-preparation phase, makes the LC relax to the transient planar state. The duration of this phase is such that the transition to the TP texture is only partial. If the voltage in the selection phase is also low, the LC remains in the conic helix structure. On the other hand, a high voltage in the selection phase stops the transition to the TP texture and the LC material switches back to the homeotropic texture. The influence on the following states is as follows:

- Low voltage in the selection phase: the low voltage in the post-

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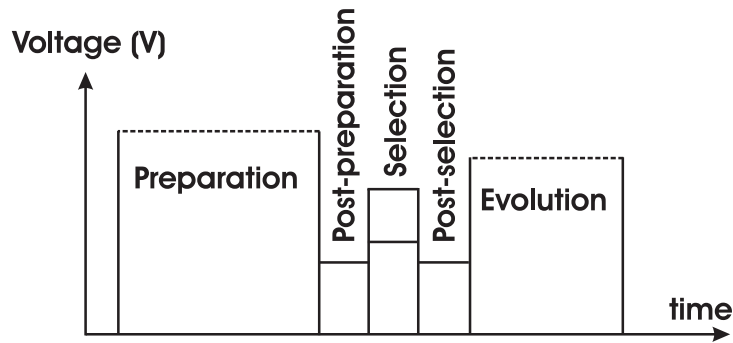


Figure 4.8: Example of a dynamic drive scheme

selection phase will finish the transition to the TP texture almost completely. In the evolution phase, an intermediate voltage is put over the LC cell. In this phase, the LC material is switched to the FC texture. After the evolution phase, the voltage is sufficiently low, so the LC remains in the FC texture.

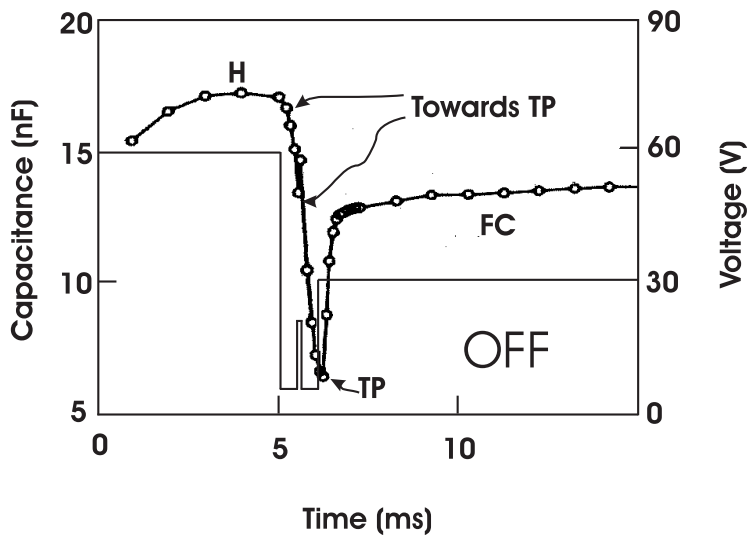


Figure 4.9: Dynamic drive scheme: evolution to the FC texture

4.2 Drive schemes for a ChLCD

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- High voltage in the selection phase: the LC that was switched to the homeotropic texture in the selection phase relaxes slightly back to the TP texture again due to the low voltage in the post-selection phase. Then it is switched back again to the homeotropic texture in the evolution phase. When the voltage is withdrawn or sufficiently low after the evolution phase the material relaxes to the TP texture and then to the SP texture.

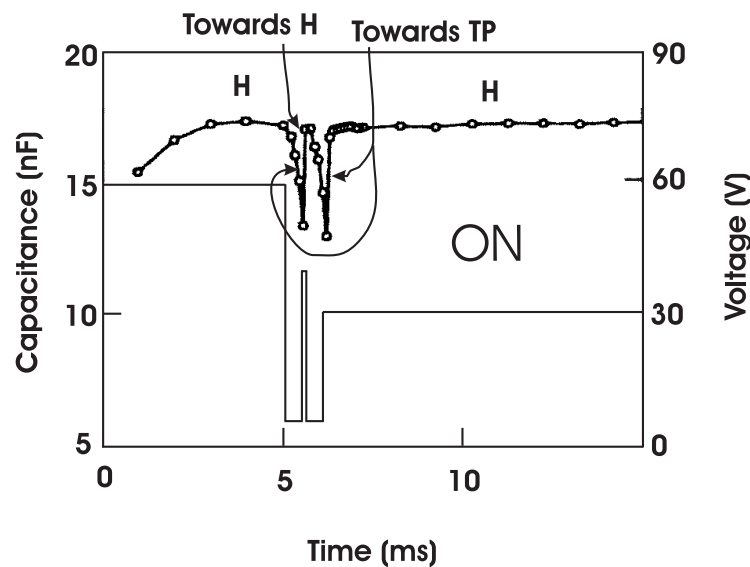


Figure 4.10: Dynamic drive scheme: evolution to the SP texture

Figure 4.9 and Figure 4.10 illustrate the behavior of a cholesteric LC material that reflects yellow light ($\lambda = 580nm$) in both cases. For this material, the $H \rightarrow TP$ transition takes $0.9ms$. These results are from the Kent State University [6]. On the left vertical axis, one can see that the state of the LC is measured by use of the cell capacitance. Because the orientation of the LCs determines the ϵ - value of the cell, the capacitance is a good measurement parameter to derive the state of the LC [6] [7].

In practice, the applied waveform is bipolar because the LC can not bear DC-voltages. The LC is insensitive to the polarity of the applied voltage. A schematic example of the bipolar implementation of the waveform is

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shown in Figure 4.11.

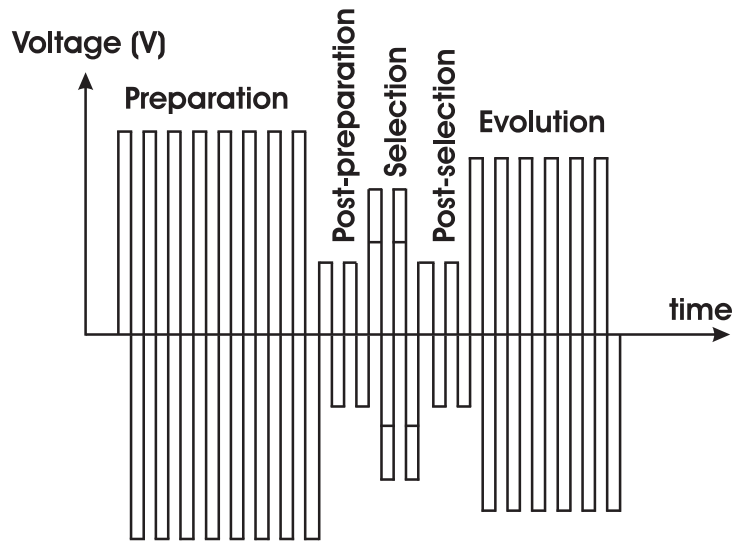


Figure 4.11: Dynamic drive scheme: bipolar implementation

Implementing the dynamic drive scheme in a pipeline-mechanism, results in the following total frame time for an n-line display:

$$T_{frame} = T_p + T_{pp} + T_{ps} + T_e + n * T_s \quad (4.1)$$

where T_p , T_{pp} , T_s , T_{ps} and T_e are respectively the preparation, post-preparation, selection, post-selection and evolution times. The pipeline-mechanism is shown in Figure 4.12.

The row and column waveforms are chosen in a way that the voltages on the columns only influence the row that is in the selection phase that time. The voltage over the pixels in the previous rows being in the post-selection or evolution phase or over the pixels in the succeeding rows being in the preparation or post-preparation phase are changed a bit, but not enough to result in another behavior of the LC.

Due to the pipeline-mechanism, dynamic driving is much faster. However, it does not allow the usage of gray values. During the selection phase, the optical response of the LC can only be pushed in a certain direction (towards black or white). It is very difficult to control the exact

4.2 Drive schemes for a ChLCD

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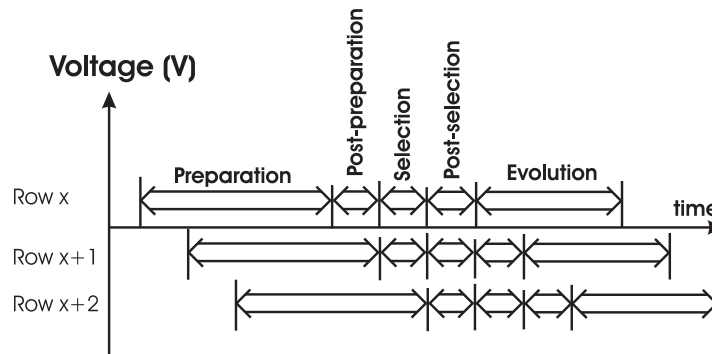


Figure 4.12: Dynamic drive scheme: pipeline-mechanism

optical response if the selection phase is only $50\mu s$ and therefore no gray levels can be made.

4.2.3 Alternative implementation of the drive schemes

Since the LC does not tolerate a long-lasting DC-voltage, the average voltage over the cell needs to be $0V$. A possible way to achieve this is by using a bipolar drive scheme as illustrated in Figure 4.7 and Figure 4.11. As an alternative, also **frame-inversion** can be used. Instead of voltage compensation during the same line addressing time, the voltages are compensated in a subsequent frame-selection. Figure 4.13 illustrates the difference between line-inversion and frame-inversion for a 3×3 display and a conventional drive scheme. Three different voltage levels are applied to the rows and columns. For the first row, these voltage levels are $25V$, $-15V$ and $-15V$. In case of line-inversion, these voltage levels are compensated immediately resulting in the sequence $25V \rightarrow -25V \rightarrow -15V \rightarrow 15V \rightarrow -15V \rightarrow 15V$. In case of frame-inversion, the opposite voltage levels are applied in a next frame time.

Furthermore, the drive schemes can be adapted to lower the voltage swing in the row drivers in order to reduce the voltage requirements of the system. Of course, this involves a higher voltage swing in the column drivers. The optimal situation of a **minimum voltage swing** in the whole driver system is obtained when the maximum voltage swing in the

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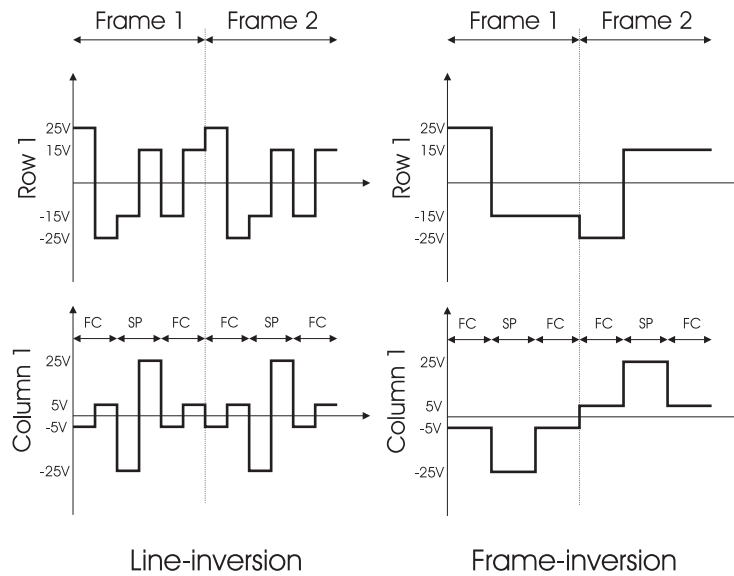


Figure 4.13: Line and frame inversion

row and column drivers is identical. To illustrate this, we go back to Figure 4.7. This figure gives an example of the row and column waveforms in case of a conventional drive system. The maximum voltage swing of a row waveform is $V_{swing,max,row} = V3 + V4$ and in a column waveform $V_{swing,max,column} = V4 - V3$. Hence, the average maximum voltage swing is $V4$. Subtracting the voltage value $V3/2$ from all the row and column voltages in the first half of the line time and adding $V3/2$ in the second half of the line time results in identical voltage requirements for the row and column drivers. The adaptation of Figure 4.7 by doing this, is shown in Figure 4.14. Since the non-select row voltage isn't $0V$ anymore, this waveform is added to the figure. Note that the resulting pixel voltages do not change.

To avoid negative voltages, the easiest way is to choose a lower reference voltage. In other words, just adding a constant value to every voltage.

Furthermore, the voltage waveforms can be adapted in order to reduce the

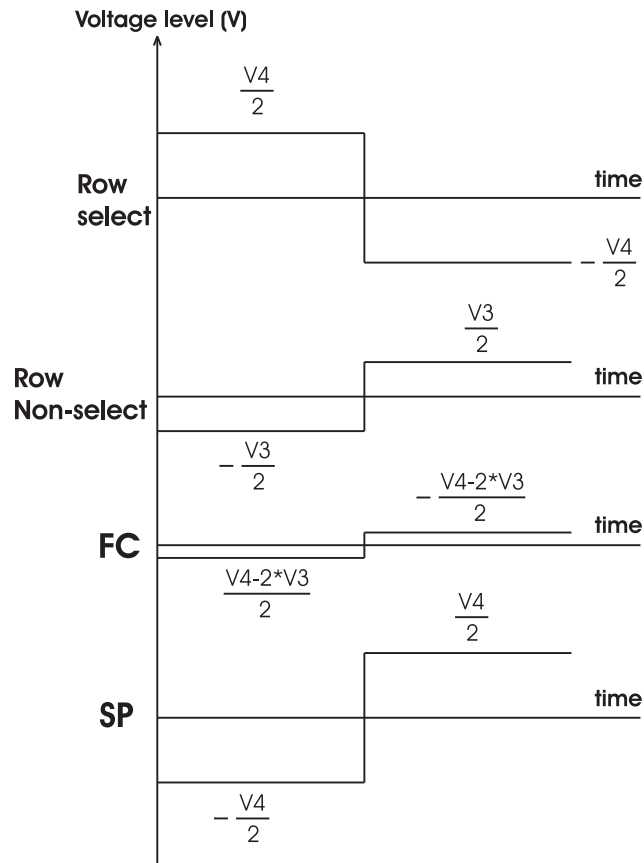


Figure 4.14: Example of a minimum swing conventional drive scheme

power consumption. This is the main goal of this Ph.D. and is discussed in the following chapters.

4.3 Applications

The bistable nature of the cholesteric liquid crystals makes them very useful in battery powered applications with an image refresh rate lower than the traditional $50Hz$. Examples are the PDA or the e-book.

The world leader in the research, development, and manufacture of

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Cholesteric Texture Liquid Crystal Display products is Kent Displays. This company was founded in 1993 to further develop and commercialize the Cholesteric Display technology.

Another company involved in the research of ChLCDs is the Swedish company LC-TEC. In 1994, the LC-TEC HOLDING consisted of LC-TEC AUTOMATION and LC-TEC DISPLAYS. LC-TEC AUTOMATION (formally *Hörnell* Automation AB) was formed in 1988 to develop and manufacture equipment for LCD-production. LC-TEC DISPLAYS (formally *Hörnell* Innovation AB) was formed in 1992 and carries out *R&D* work in the field of liquid crystal displays. In 2004, LC-TEC AUTOMATION was sold. LC-TEC DISPLAYS manufactures and supplies an 18.1 inch diagonal SVGA (800 * 600 pixels) monochrome cholesteric texture liquid crystal display (Ch-LCD) module.

At our research group, a cooperation with Asulab, a division of the Swatch Group Research and Development Ltd., has led to the development of a watch with an integrated digital camera being shown in Figure 4.15.



Figure 4.15: Iris watch developed in cooperation between TFCG-microsystems and Asulab

The watch with classical design has a digital 80x104 display and contains, despite of its small size, a complete digital camera. It also has an infrared link to a PC for further processing of the images.

The test driver for this watch that was developed at TFCG-microsystems,

is similar to the driver I use in my Ph.D. to test my design. Another possible application for ChLCDs is a bank card with an integrated display as shown in Figure 4.16.



Figure 4.16: Smartcard with a bistable display

This is useful in e-purse applications. For this application, no internal battery is needed. The energy is withdrawn from an external source like a card reader. The card reader includes a reading mechanism which makes a galvanic contact with the card when inserted correctly. This way, the card can be read and programmed. After withdrawal of the card, the display maintains its content due to its bistable character.

4.4 Conclusion

Several drive schemes are possible for a cholesteric texture LCD. Either a long-duration pulse or a sequence of short pulses can be used. A dynamic drive scheme is used for video-applications since they are faster than the conventional drive scheme. On the other hand, the conventional drive scheme has the advantage that gray values are possible in contrast to the dynamic drive scheme that does not allow gray values. Once the choice between conventional or dynamic driving is made, the drive waveforms can still be adapted according to the demands.

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Chapter 5

Theoretical calculation of the power consumption

To create a power-efficient display, it is important to know which part of the display driver consumes most of the energy or where energy is lost. A theoretical calculation of the power consumption in the driver provides you with a better insight into the energy behavior. In this chapter, the energy consumption of one switch is calculated followed by the energy consumed by a display driver.

Since the aim is to create a display consisting of gray pixels, dynamic driving is useless and so we only focus on conventional drive schemes. A second constraint is the use of line inversion opposed to frame inversion since not all of the cholesteric liquid crystals can withstand DC stressing during one frame time.

Finally, the benefit of minimum-swing driving in terms of power consumption is examined.

5.1 Power calculation in one switch

Figure 5.1 shows a voltage source that delivers a certain amount of energy to charge the capacitor C .

Suppose that at $t = 0$, the voltage over the capacitor is V_A . When the switch closes, a current starts to flow and the capacitor is charged. The amount of current is determined by the capacitor value and the voltage

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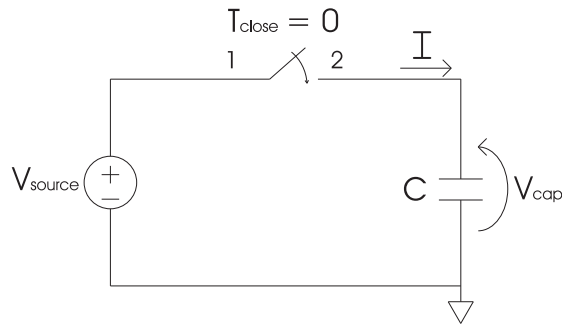


Figure 5.1: Charging of a capacitor by means of a voltage source

change over the capacitor.

$$I = C * \frac{dV_{cap}}{dt} \tag{5.1}$$

Note that the elements in Figure 5.1 are not ideal meaning that both the voltage source and the switch have an internal resistance. Practically, the switch can be a transistor for example. The total energy supplied by the voltage source is

$$\begin{aligned} \Delta E_{source} &= \int_A^B P_{source} * dt \\ &= \int_A^B V_{source} * C * \frac{dV_{cap}}{dt} * dt \\ &= C * V_{source} * \int_A^B dV_{cap} \\ &= C * V_{source} * (V_B - V_A) \end{aligned} \tag{5.2}$$

V_B represents the end voltage over the capacitor.

When the capacitor is fully charged, the end voltage over the capacitor being the same as the voltage delivered by the voltage source, ΔE_{source} can be rewritten as follows:

$$\Delta E_{source} = C * V_B * (V_B - V_A) \tag{5.3}$$

The energy stored in the capacitor during this time is

5.2 Power calculation in a display driver

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$$\begin{aligned}
 \Delta E_{cap} &= \int_A^B P_{cap} * dt \\
 &= \int_A^B V_{cap} * C * \frac{dV_{cap}}{dt} * dt \\
 &= C * \left(\frac{V_B^2}{2} - \frac{V_A^2}{2} \right)
 \end{aligned} \tag{5.4}$$

We can conclude that this is less than the energy supplied by the source. The part of the energy that is lost in the system is given by the difference between the delivered source energy and the energy stored in the capacitor:

$$\begin{aligned}
 E_{lost} &= C * V_B * (V_B - V_A) - C * \left(\frac{V_B^2}{2} - \frac{V_A^2}{2} \right) \\
 &= C * \left(\frac{V_B^2}{2} + \frac{V_A^2}{2} - V_B * V_A \right) \\
 &= C * \frac{1}{2} * (V_B - V_A)^2
 \end{aligned} \tag{5.5}$$

The energy being lost in the switch does not depend on its exact properties such as type of transistors or dimensions of the transistor channels. Instead these properties determine the dynamics of the system, for example how fast the capacitors can be charged.

Another conclusion is that the energy needed only depends on the capacitor value, the end voltage over the capacitor and the difference between begin and end voltage over the capacitor. The capacitor value depends on the display, so this parameter is fixed.

5.2 Power calculation in a display driver

A display consists of at least $R * K$ capacitors with R being the number of rows and K the number of columns. A schematic representation of a PM display is shown in Figure 5.2.

80 Theoretical calculation of the power consumption

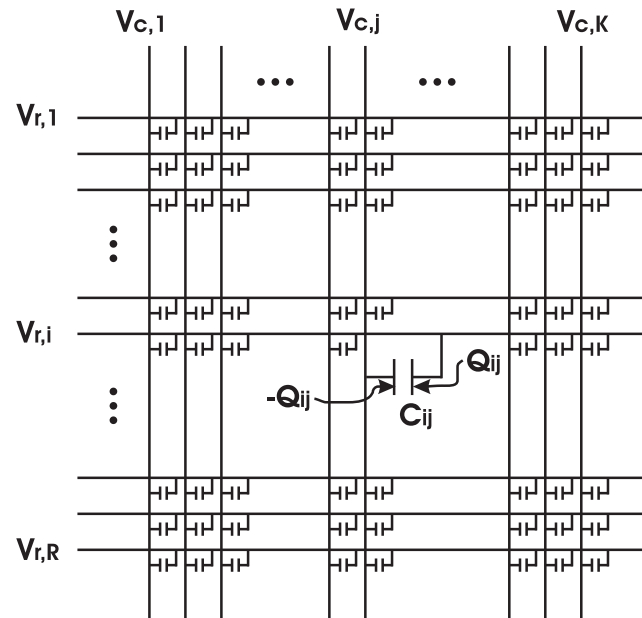


Figure 5.2: A PM display consists of at least $R * K$ capacitors

To calculate the energy supplied by the voltage sources, we look at what happens when all the row and column voltages change from an initial stable state A to a new stable state B.

1. $V_{ri}^A \rightarrow V_{ri}^B; i=1, \dots, R$
2. $V_{cj}^A \rightarrow V_{cj}^B; j=1, \dots, K$

The switch from state A to B occurs on every row and column by means of a multiplexer composed of a number of switches. In the following calculation, the power consumption of the low-voltage part (the logic that drives the switches) is not taken into account.

Let us first focus on one particular row i . After changing the position of the switch, a current I_{ri} will flow to charge or discharge the row capacitors changing the row potential to its new stable value V_{ri}^B . Therefore, during

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the transition from state A to B, the source V_{ri}^B has to deliver an electric power given by:

$$P_{ri} = V_{ri}^B * I_{ri} = V_{ri}^B * \frac{d}{dt} \left(\sum_{j=1}^K Q_{ij} \right) \quad (5.6)$$

Hence, the energy supplied by the source V_{ri}^B to charge or discharge row i from an initial state A to a final state B is equal to:

$$\begin{aligned} \Delta E_{ri} &= \int_A^B P_{ri} * dt \\ &= \int_A^B V_{ri}^B * d \left(\sum_{j=1}^K Q_{ij} \right) \\ &= \int_A^B V_{ri}^B * C_0 * d \left[\sum_{j=1}^K (V_{ri} - V_{cj}) \right] \\ &= C_0 * V_{ri}^B * \sum_{j=1}^K \left[(V_{ri}^B - V_{ri}^A) - (V_{cj}^B - V_{cj}^A) \right] \end{aligned}$$

$$\Rightarrow \Delta E_{ri} = C_0 * V_{ri}^B * \left[K * (V_{ri}^B - V_{ri}^A) - \sum_{j=1}^K (V_{cj}^B - V_{cj}^A) \right] \quad (5.7)$$

It is assumed that all pixel capacitors C_{ij} have the same constant value C_0 . In a very similar way, we obtain the power delivered by the voltage source V_{cj}^B that charges or discharges the pixel capacitors on column j during the transition from state A to B:

$$P_{cj} = V_{cj}^B * I_{cj} = V_{cj}^B * (-1) * \frac{d}{dt} \left(\sum_{i=1}^R Q_{ij} \right) \quad (5.8)$$

The corresponding energy is given by:

$$\Delta E_{cj} = \int_A^B P_{cj} * dt$$

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$$\begin{aligned}
 &= - \int_A^B V_{cj}^B * d \left(\sum_{i=1}^R Q_{ij} \right) \\
 &= - \int_A^B V_{cj}^B * C_0 * d \left[\sum_{i=1}^R (V_{ri} - V_{cj}) \right] \\
 &= -C_0 * V_{cj}^B * \sum_{i=1}^R [(V_{ri}^B - V_{ri}^A) - (V_{cj}^B - V_{cj}^A)] \\
 \Rightarrow \Delta E_{cj} &= C_0 * V_{cj}^B * \left[R * (V_{cj}^B - V_{cj}^A) - \sum_{i=1}^R (V_{ri}^B - V_{ri}^A) \right] \quad (5.9)
 \end{aligned}$$

In order to obtain the total energy needed to bring the whole display from an initial state A to a final state B, we simply add the individual contributions of all voltage sources:

$$\Delta E_{tot} = \sum_{i=1}^R \Delta E_{ri} + \sum_{j=1}^K \Delta E_{cj} \quad (5.10)$$

This results in:

$$\begin{aligned}
 \Rightarrow \Delta E_{tot} &= C_0 * K * \sum_{i=1}^R [V_{ri}^B * (V_{ri}^B - V_{ri}^A)] \\
 &- C_0 * \left(\sum_{i=1}^R V_{ri}^B \right) * \left[\sum_{j=1}^K (V_{cj}^B - V_{cj}^A) \right] \\
 &+ C_0 * R * \sum_{j=1}^K [V_{cj}^B * (V_{cj}^B - V_{cj}^A)] \\
 &- C_0 * \left(\sum_{j=1}^K V_{cj}^B \right) * \left[\sum_{i=1}^R (V_{ri}^B - V_{ri}^A) \right] \quad (5.11)
 \end{aligned}$$

As a final step, we can use the total display capacitance $R * K * C_0$ to normalize the total energy consumption:

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$$\begin{aligned}
 \frac{\Delta E_{tot}}{R * K * C_0} &= \frac{1}{R} * \sum_{i=1}^R [V_{ri}^B * (V_{ri}^B - V_{ri}^A)] \\
 &- \left(\frac{1}{R} * \sum_{i=1}^R V_{ri}^B \right) * \left[\frac{1}{K} * \sum_{j=1}^K (V_{cj}^B - V_{cj}^A) \right] \\
 &+ \frac{1}{K} * \sum_{j=1}^K [V_{cj}^B * (V_{cj}^B - V_{cj}^A)] \\
 &- \left(\frac{1}{K} * \sum_{j=1}^K V_{cj}^B \right) * \left[\frac{1}{R} * \sum_{i=1}^R (V_{ri}^B - V_{ri}^A) \right] \quad (5.12)
 \end{aligned}$$

This normalization of the formula has the advantage of only containing averages of squared or multiplied voltages and products of mean voltages. Therefore this normalized energy does not depend much on the display size and is almost entirely determined by the applied waveform. Formula 5.12 is the normalized energy consumption during the transition from one stable state to another. To display a new image on a display, a number of waveforms containing several voltage transitions are applied [1]. The total energy consumption is the sum of the energy consumed during all of these separate steps. More specifically, during the selection of one row, the row-select waveform is applied to that row. Simultaneously, the row-non-select waveform is applied to all the other rows and the data waveforms are applied to their corresponding columns (see Figure 4.7 and Figure 4.14). For a display refresh all rows have to be selected in succession. Since the normalized energy per row addressing time is almost independent of the display size (certainly for the applications in this Ph.D.), the sum of all these contributions will be proportional to the number of rows. Therefore the obtained result can be divided by the number of rows. Let ΔE_{frame} be the total amount of energy supplied by all the driver sources during a complete frame time in order to display a particular pixel pattern on the screen. So ΔE_{frame} is the sum of all the different contributions ΔE_{tot} needed to create an image on the display. To compare different drive schemes or the portrayal of different images, it is useful to utilize a parameter independent of the number of rows or columns. Dividing ΔE_{frame} by both the number of rows and the total display capacitance results in the parameter α which is called the "nor-

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malized frame energy".

$$\alpha = \frac{\Delta E_{frame}}{R^2 * K * C_0} \quad (5.13)$$

However, there is still a small dependency of α with the number of rows. For displays with a small number of rows, the contribution of the row-select waveform is important. As the number of rows increases, this contribution and hence the dependency of α with the number of rows decreases. Despite of this small dependency, the coefficient α is an excellent parameter to evaluate the performance of different driving schemes as far as power consumption is concerned.

All conclusions made in the following chapters are correct for displays with more than ten rows. In displays with a smaller number of rows, the bigger contribution of the row-select waveform for example will result in other conclusions. This will not be taken into account further on in this book since most practical applications have displays with a lot more than ten rows.

One can conclude from formula 5.12 that the end voltages together with the voltage step on the rows and columns determine the energy consumption. So the normalized frame energy α will be highly dependent of the shape and voltage levels of the applied waveforms.

The comprehension of these formulas allows us to develop a more efficient driver. Chapter 6 explains how the driver system developed in this Ph.D. is optimized based on this knowledge.

5.3 Power consumption in a minimum-swing driven display

Before adapting the waveforms derived in chapter 4, we will first calculate the normalized frame energy in this section for the basic conventional drive scheme shown in Figure 4.7 and the minimum-swing conventional drive scheme (Figure 4.14).

To facilitate the calculation, we turn back to Figure 3.22 (repeated in Figure 5.3). This shows schematically the electro-optical response for the ChLCD used in this Ph.D., with the most important numerical values

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added.

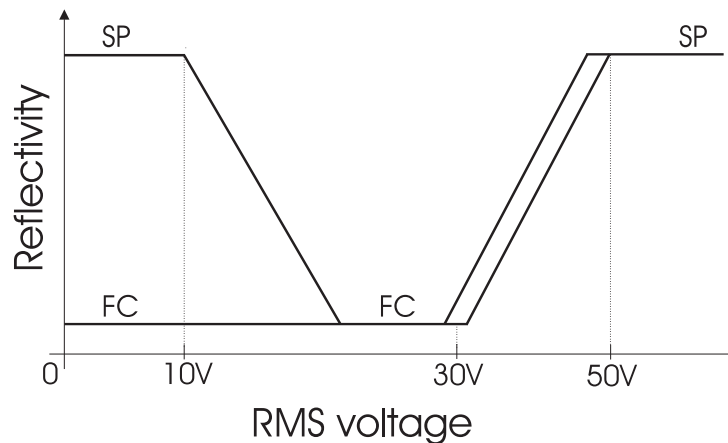


Figure 5.3: Reflectivity of the ChLC as a function of the rms voltage of the applied voltage pulse

Figure 4.7 combined with Figure 5.3 results in the following numerical values for the row and column voltages:

- row-select voltage: $V_R = \frac{V_3+V_4}{2} = \frac{30+50}{2}V = 40V$
- row-non-select: $0V$
- Focal Conic: $V_{C2} = \frac{V_4-V_3}{2} = \frac{50-30}{2}V = 10V$
- Stable Planar: $V_{C1} = \frac{V_3-V_4}{2} = \frac{30-50}{2}V = -10V$

The voltage over a non-selected pixel has an amplitude of $10V$ which satisfies the demand that a pixel on a non-selected row may not be influenced. These waveforms are represented in Figure 5.4. The first waveform is the row-select waveform. The other (non-selected) rows are connected to $0V$. The second waveform is the data waveform to be applied to those columns where the pixel on the selected row must be black (in order to bring the LC to the FC state). The last waveform is the data waveform corresponding to a white pixel on the selected row (LC in the SP state).

The numerical values for the minimum-swing drive scheme are:

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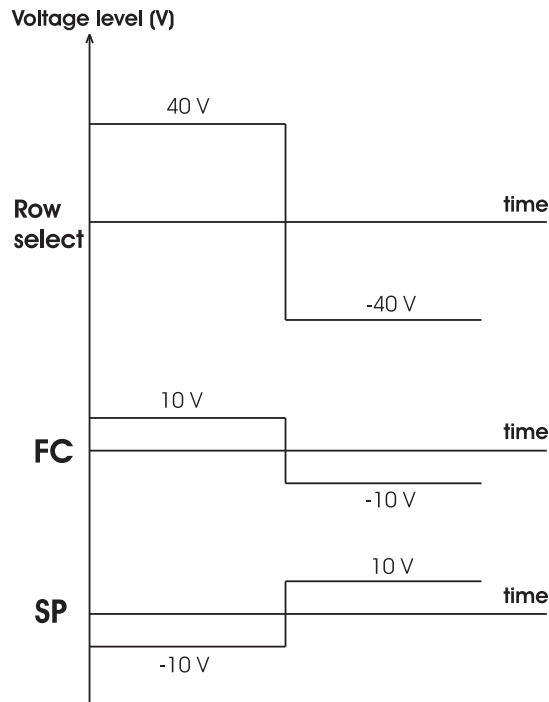


Figure 5.4: Row and column waveforms to drive a ChLCD

- row-select voltage: $V_R = \frac{V_4}{2} = \frac{50}{2} V = 25V$
- row-non-select: $V_{-R} = \frac{-V_3}{2} = \frac{-30}{2} V = -15V$
- Focal Conic: $V_{C2} = \frac{V_4 - 2 \cdot V_3}{2} = \frac{50 - 2 \cdot 30}{2} V = -5V$
- Stable Planar: $V_{C1} = \frac{-V_4}{2} = \frac{-50}{2} V = -25V$

In this case the amplitude of the voltage over a non-selected pixel is also 10V and therefore small enough to keep the optical response of the pixel from changing. The corresponding waveforms are shown in Figure 5.5.

The calculation of the normalized frame energy α , based on formula 5.12, is done for five different images with a resolution of 16x16 pixels. It is assumed that begin and end voltage of every row and column is 0V. With this in mind, the calculated energy represents the total amount of energy dissipated (wasted) in the driver circuits since the initial and final energy

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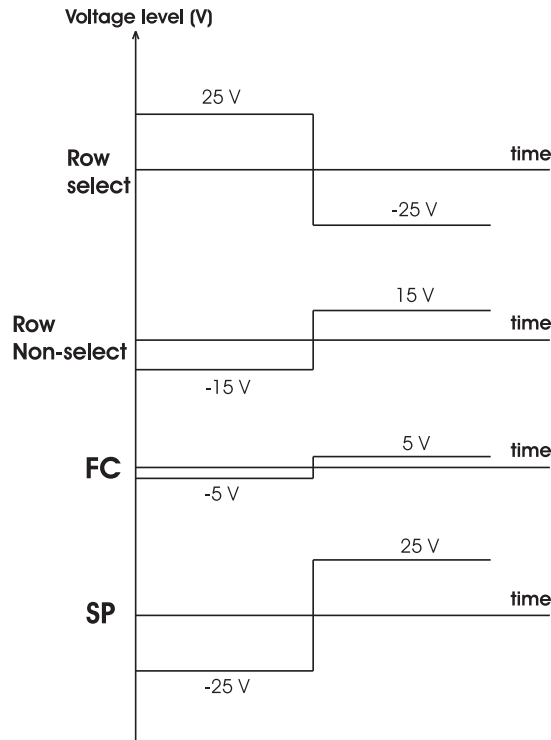


Figure 5.5: Minimum swing row and column waveforms to drive a ChLCD

stored in the display capacitances are exactly the same. The results are represented in Table 5.1. Both drive schemes result in the same energy consumption for these five types of images displayed. To investigate whether this can be generalized for all different kinds of images, we rewrite formula 5.12 as follows:

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Table 5.1: Comparison of α for the conventional drive scheme shown in Figure 5.4 and the minimum swing conventional drive scheme shown in Figure 5.5

	$\alpha = \frac{\Delta E_{frame}}{R^2 * K * C_0} (V^2)$	
	Conventional drive scheme presented in Figure 5.4	Minimum swing conventional drive scheme presented in Figure 5.5
All pixels "FC"	497	497
All pixels "SP"	891	891
Horizontal lines	506	506
Vertical lines	694	694
All gray pixels	706	706

$$\frac{\Delta E_{tot}}{R * K * C_0} = \frac{1}{R * K} * \left\{ \begin{array}{l} K * \sum_{i=1}^R [V_{ri}^B * (V_{ri}^B - V_{ri}^A)] \\ - \sum_{i=1}^R \sum_{j=1}^K V_{ri}^B * (V_{cj}^B - V_{cj}^A) \\ + R * \sum_{j=1}^K [V_{cj}^B * (V_{cj}^B - V_{cj}^A)] \\ - \sum_{i=1}^R \sum_{j=1}^K V_{cj}^B * (V_{ri}^B - V_{ri}^A) \end{array} \right.$$

A rearrangement and rewriting of the terms gives:

$$\frac{\Delta E_{tot}}{R * K * C_0} = \frac{1}{R * K} * \left\{ \begin{array}{l} \sum_{i=1}^R \sum_{j=1}^K [V_{ri}^B * (V_{ri}^B - V_{ri}^A)] \\ - \sum_{i=1}^R \sum_{j=1}^K V_{ri}^B * (V_{cj}^B - V_{cj}^A) \\ + \sum_{i=1}^R \sum_{j=1}^K [V_{cj}^B * (V_{cj}^B - V_{cj}^A)] \\ - \sum_{i=1}^R \sum_{j=1}^K V_{cj}^B * (V_{ri}^B - V_{ri}^A) \end{array} \right.$$

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And further:

$$\frac{\Delta E_{tot}}{R * K * C_0} = \frac{1}{R * K} * \left\{ \begin{array}{l} \sum_{i=1}^R \sum_{j=1}^K \{ V_{ri}^B * [(V_{ri}^B - V_{ri}^A) - (V_{cj}^B - V_{cj}^A)] \} \\ + \sum_{i=1}^R \sum_{j=1}^K \{ V_{cj}^B * [(V_{cj}^B - V_{cj}^A) - (V_{ri}^B - V_{ri}^A)] \} \end{array} \right\}$$

More:

$$\frac{\Delta E_{tot}}{R * K * C_0} = \frac{1}{R * K} * \left\{ \begin{array}{l} \sum_{i=1}^R \sum_{j=1}^K \{ V_{ri}^B * [-(-V_{cj}^A + V_{ri}^A) + (-V_{cj}^B + V_{ri}^B)] \} \\ + \sum_{i=1}^R \sum_{j=1}^K \{ -V_{cj}^B * [-(V_{ri}^A - V_{cj}^A) + (V_{ri}^B - V_{cj}^B)] \} \end{array} \right\}$$

This leads to the following result:

$$\frac{\Delta E_{tot}}{R * K * C_0} = \frac{1}{R * K} * \left\{ \sum_{i=1}^R \sum_{j=1}^K \{ [V_{ri}^B - V_{cj}^B] * [(V_{ri}^B - V_{cj}^B) - (V_{ri}^A - V_{cj}^A)] \} \right\}$$

One can see that the formula for the energy consumption can be rewritten in a formula that only contains terms that represent pixel voltages. Hence, the exact voltage values on the rows and columns are not important, only the difference between them. At first sight, the parameters that can be changed to reduce the power consumption are the end voltage value over the pixels and the value of the voltage transition over the pixels.

Comparing this expression with formula 5.3, one can see that this expression is in fact the sum of the contributions of all voltage sources that charge every pixel separately. The only way to reduce the power consumption in the driver for a certain display with characteristics R,K and C₀, is to reduce the voltage steps over the pixels.

For the conventional drive scheme represented in Figure 5.4, the voltage amplitudes over the pixels in the first half line time are:

- non-selected "FC" pixel: -10V
- selected "FC" pixel: 30V

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- non-selected "SP" pixel: $10V$
- selected "SP" pixel: $50V$

When looking at Figure 5.5, one can see that these pixel voltages are equal when using the minimum swing drive scheme. Thus, mathematically, it is clear that both drive schemes result in the same power consumption. Instinctively, one can understand that in the non-minimum-swing drive scheme higher voltages are used. On the other hand, the non-selected rows are kept at a constant $0V$ potential so there is no energy flow in the non-selected lines. In the minimum-swing drive scheme, there are voltage variations in all rows and columns. As a consequence, the energy flow is spread over all rows and columns and therefore lower voltages can be used. The energy flow is distributed in a different way, but the global power consumption remains the same.

5.4 Conclusion

Based on formula 5.12, one can calculate the energy consumption for any kind of drive scheme and image. To have a display-independent result, the parameter α is used, being the frame energy divided by the display capacitance and the total number of rows.

The minimum swing drive scheme is useful in order to reduce the voltage requirements of the system, but has no advantage regarding the power consumption. The power consumption is only influenced by the voltages over the pixels and not by the absolute value of the row and column voltages. The two parameters that determine the final energy consumption are the voltage transitions over the pixels and the pixel voltages after the pixels are charged or discharged.

References

- [1] J. Doutreloigne, H. De Smet, and A. Van Calster. High-voltage driver for cholesteric lcds. In *Proceedings of Displays and Vacuum Electronics*, number 165, pages 283–287, Garmisch-Partenkirchen, 5 2001. Information Technology Society of VDE.

Chapter 6

Optimization of the drive waveforms to reduce the power consumption

This chapter deals with the optimization of the drive waveforms for a ChLCD based on the theoretical calculation in chapter 5.

Since dynamic driving is useless because no gray values are possible, frame inversion is not recommended for DC-stressing and a minimum-swing conventional drive scheme has no advantage regarding the power consumption, we start from the basic traditional drive scheme represented in Figure 5.4 to derive more power-efficient drive waveforms.

The voltage values in this drive scheme correspond to the rising slope of the electro-optical characteristic of a ChLCD. The choice of the rising slope is mainly based on the advantage of a better contrast. From Figure 4.5, it is clear that the reflectivity corresponding to black on the rising slope is less than the reflectivity corresponding to black on the falling slope. Since the human eye is very sensitive to black, this is an important factor. Another advantage is the speed of the rising slope.

A drive scheme for a bistable cholesteric texture LCD can consist of a reset part and a line-scanning part. In the reset part, the pixels are put in the stable planar state. In this state, the pixels appear white. Resetting the display avoids image sticking. During line-scanning, the rows get a selection signal one at a time. The signals applied to the columns are the data signals that determine the gray scale of the pixels at the intersection

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of the corresponding column and the selected row.
 In the first section, the main principles used to reduce the power consumption are explained. The adaptation of the row and column waveforms during line-scanning and reset is demonstrated in the second and third section respectively. In the end, the theoretical results are discussed.

6.1 Principles to reduce the power consumption

In order to reduce the power consumption in a ChLCD driver, I searched some methods to create more energy-efficient drive waveforms. From the previous chapter we learned that the end pixel voltage (after charging or discharging the pixel) together with the value of the voltage transition determine the resulting power consumption. So the aim is to lower those voltages. The amplitude of the pixel voltages is determined by the electro-optical response. Thus, we have to try to lower the voltage differences. Adding intermediate voltage levels is a solution to this problem and is explained further on. External voltage sources can be used to generate those intermediate voltages, but they can also be created by short-circuiting the appropriate rows or columns. This method is called charge recycling. Since the most efficient drive method differs according to the displayed image, it is useful to calculate the drive waveforms based on the image information.

Depending on the application, some pixels do not change colour every time so it can be interesting to update only a part of the display. In order to do so, an extra memory unit is needed to store the previous image as well as a calculation unit to check which pixels change.

Next, the four principles that can result in a power saving are discussed.

6.1.1 Intermediate voltage levels

In section 5.1, we derived that the energy lost in the switch when charging a capacitor from voltage V_A to V_B is given by:

$$\begin{aligned} \Delta E_{lost} &= C * \frac{1}{2} * (V_B - V_A)^2 \\ &= C * \frac{1}{2} * \Delta V_{cap}^2 \end{aligned} \tag{6.1}$$

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ΔV_{cap} is taken as the voltage step in time. ΔV_{cap} can be split up into two different steps: $\Delta V_{cap} = \Delta V_1 + \Delta V_2$ ($\Delta V_1 > 0$ and $\Delta V_2 > 0$). This step in square can be written as:

$$\begin{aligned} \Delta V_{cap}^2 &= (\Delta V_1 + \Delta V_2)^2 = \Delta V_1^2 + \Delta V_2^2 + 2 * \Delta V_1 * \Delta V_2 \\ &> \Delta V_1^2 + \Delta V_2^2 \end{aligned}$$

This means that the power consumption during a voltage transition is less if that transition would be divided in two separate steps. Let us extend this and divide the transition into n separate steps. For reasons of easy calculation, we assume steps of the same height and a starting value of $0V$ over the capacitor. First, the capacitor is charged to a voltage V_{cap}/n , then to a voltage $2V_{cap}/n$ and so on until its final value V_{cap} is reached. This is represented schematically in Figure 6.1.

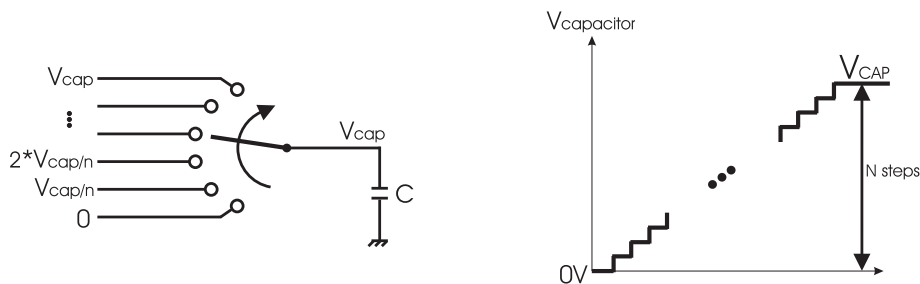


Figure 6.1: Dividing a voltage transition into n separate steps

The total amount of energy that is lost is given by:

$$\begin{aligned} \Delta E_{lost,n} &= \frac{1}{2} * C * \sum_{i=1}^n \left(\frac{V_{cap}}{n}\right)^2 \\ \Rightarrow \Delta E_{lost,n} &= \frac{1}{2} * C * \frac{V_{cap}^2}{n} \end{aligned}$$

For $n = 1$ we find ΔE_{lost} again, as anticipated. Increasing the number of steps reduces the power consumption in an inversely proportional way. For the number of steps n tending to infinity, the energy wasted in the

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driver circuit becomes zero. In the same way, if a capacitor has to be discharged from an initial value V_{cap} to $0V$, it is preferable to do this in n separate steps. The capacitor needs to be connected consecutively to a voltage source $(n - 1)V_{cap}/n$, then $(n - 2)V_{cap}/n$ and so on until $0V$. Again, no energy is lost in the driver circuit for n tending to infinity and the total energy stored in the capacitor will be completely recuperated by the different voltage sources.

In a ChLCD, there are $R \times K$ pixels that can be represented by $R \times K$ capacitors. When writing an image on the screen, several voltage transitions occur in all rows and columns. All these transitions involve a certain amount of energy flowing from the driver sources to the display capacitances or the other way around. When an infinite number of steps is used to complete the transitions, no energy is wasted in the multiplexers. Since the row and column voltages are equal before and after writing the image, the result of all the energy flows during one image refresh is zero. Therefore no extra energy is stored in the pixel capacitances. This in combination with the fact that no energy is wasted in the multiplexers leads to the conclusion that the global energy delivered by the voltage sources is zero.

This seems very nice, but its practical implementation is rather problematic. A first proposal to realize this is to connect each row and column output to an analogue switch of which the other side is connected to a common ramped voltage source. An example makes this more clear. Suppose a voltage source is rising slowly (slow enough for quasi static capacitor charging) from $-40V$ to $40V$ and at a certain instant a column needs to be switched from $-10V$ to $10V$. How do we proceed? During a first interval, in which the voltage rises from $-40V$ to $-10V$, we leave the analogue switch open in order to avoid a discharge of the column capacitance. When the ramped voltage source reaches the $-10V$ value, we close the analogue switch allowing the column potential to gradually follow the source voltage. When the source voltage reaches the $10V$ level, we open the analogue switch again to maintain the correct $10V$ on the column. This way there will not be any power dissipation in the analogue switch. Of course, not all the row and column voltages have to be increased at a specific state transition. Some of them will have to be lowered. For that purpose, we let the voltage source decrease once more from $40V$ to $-40V$ and close and open the analogue switches at the adequate moments. To allow that possibility, the voltage source has to be a double ramp signal.

6.1 Principles to reduce the power consumption

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The analogue switches of the row and column driver circuits have to be closed and opened on the positive or negative slope depending on the desired state transition (on the positive slope for a voltage increase, on the negative one for a voltage reduction).

This technique seems very appealing, but there is a major drawback: once a row reaches its end value (or when there is no transition at all for that row), the corresponding analogue switch is opened. When this occurs, the total charge on that particular row remains constant (an open switch does not allow current to flow and hence there can not be any charge flow). However, parts of the columns have to be charged or discharged. This means that the potentials on the counter electrodes of those pixel capacitances are fluctuating, resulting in an uncontrolled fluctuation of the row potential. Consequently, the voltage pulses over the pixels of a selected row won't have the appropriate rms value to bring the LC to the desired state. Furthermore, pixels on non-selected rows could possibly receive pulses with an rms value high enough to alter the LC state. Obviously, the display can not work properly under those circumstances.

The uncontrolled fluctuations can be solved by combining the use of the double ramp voltage source with fixed voltage sources. Once a row or column reaches its end value, the switch connecting it to the double-ramp voltage source is opened. Then the switch connecting the row or column to the appropriate fixed voltage source is closed.

Another interesting solution would be replacing the double ramped voltage source (corresponding with an infinite number of drive voltages) and the analogue switch per row or column by a finite number of separate supply voltages and a multi-input analogue multiplexer per row or column. This way we avoid unwanted potential variations on the rows and columns. However, since the number of intermediate states is finite, the power dissipation in the multiplexer switches won't be zero any more. Choosing the number of intermediate states sufficiently high reduces the power dissipation in the driver circuits to a level of our choice. Of course, the higher the number of intermediate transitions the more complex the corresponding hardware becomes for both the multiplexers and the logic driving the multiplexers. Moreover, it's not obvious to provide a big range of different voltage sources. In the next section we will see that a good choice has to be made.

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6.1.2 Short-circuiting rows and columns

In what preceded, we assumed that the intermediate voltages were applied by a voltage source. Another way to create extra voltages is to short-circuit the appropriate rows or columns. This has the advantage that part of the charge on the display electrodes is recuperated instead of being carried away to a voltage source. An example will clarify this. Assume that a selected row gets a voltage V_1 and a non-selected row a voltage V_2 . Suppose that both voltages are positive or zero and $V_1 > V_2$ (this is only to simplify the explanation, the conclusions are the same in the other cases). First, row i is selected, afterwards row $i + 1$. This means that row i is connected first with the voltage source V_1 and in the next time frame with the voltage source V_2 . The opposite is true for row $i + 1$. By short-circuiting rows i and $i + 1$ at the moment of transition, the charge on those rows redistributes until both rows are on the same potential $(V_1 + V_2)/2$. As a result, the voltage source V_1 only has to deliver the power to charge row $i + 1$ from $(V_1 + V_2)/2$ to V_1 instead of from V_2 to V_1 ($V_2 < V_1$) which results in a power saving. Short-circuiting rows or columns involves an extra need for switches. Figure 6.2 shows the schematic of a part of a display in which two adjacent rows can be short-circuited by controlling the gate-voltage V_a of a transistor that acts as a switch.

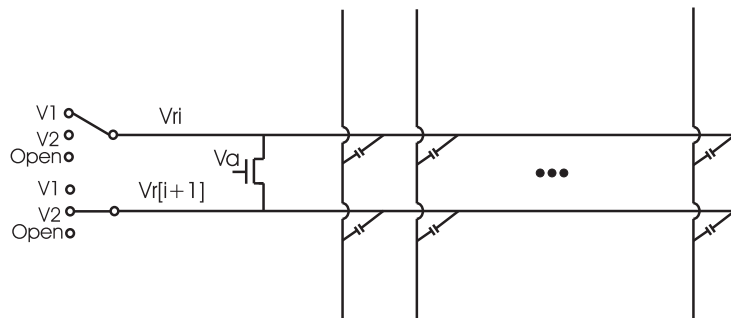


Figure 6.2: Schematic short-circuiting adjacent rows

When V_a is high, the transistor conducts and both rows are short-circuited. Figure 6.3 shows the course of the row voltages and the gate voltage. The upper part illustrates which voltages are selected for the two rows and the gate voltage of the transistor between both rows. When V_a is high, the

6.1 Principles to reduce the power consumption

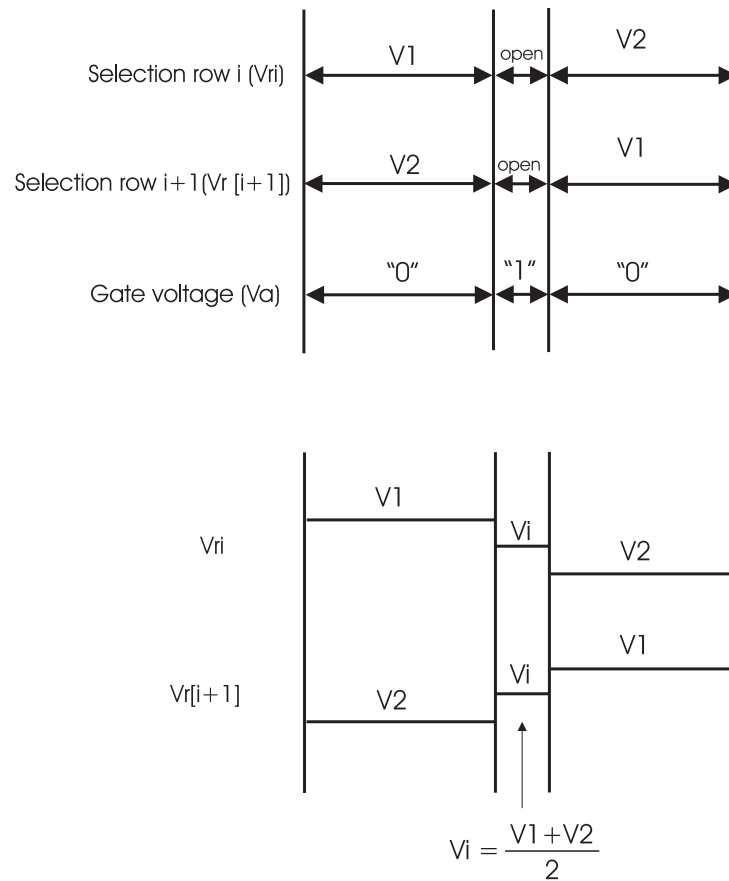


Figure 6.3: Course of the voltages when short-circuiting adjacent rows

other switches connecting row i and row $i + 1$ to an external voltage source are opened. The lower part depicts the resulting voltage levels. In the drive scheme proposed in Figure 5.4, the waveform over a selected row drops from $40V$ to $-40V$ and the voltage of a non-selected row is the constant value $0V$. This means that the voltage of the first selected row at the end of the line time¹ during which the row is selected, is the opposite of the begin voltage of the succeeding row during the next line time (the time during which row $i + 1$ is selected). Short-circuiting those rows when

¹the line time is the time that the pixels on one row are selected

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the transition should take place results in $-20V$ on both rows. Therefore the voltage source has to deliver the power to enhance the potential of row $i + 1$ from $-20V$ to $40V$ instead of from $0V$ to $40V$. In this particular case, short-circuiting works out badly. A simple solution is to reverse the row voltages of the even rows so that their row-selection waveform is one going from $-40V$ to $40V$. If we were to short-circuit with the previous odd row (that still has a row-selection waveform from $40V$ to $-40V$), the voltage source must deliver the energy to change the row potential from $-20V$ to $-40V$. Due to the smaller voltage step, the consumed energy during this transition is less than during the transitions from $0V$ to $40V$ or $0V$ to $-40V$.

However, the question arises whether or not the reversal of the line-select waveform influences the functioning of the display. The answer is yes, of course. Since the pixel voltages change, the optical response of the pixels changes. How this problem is solved, is explained further.

Another option besides short-circuiting to an external source or a row capacitor is to short-circuit to an external capacitor. More information can be found in [1], [2] and [3]. An external capacitor has the advantage being able to charge or discharge the pixel capacitors without the need of an external voltage source and so without power consumption. It can be regarded as a kind of buffer. However, the external capacitor also needs to be charged once. Since the capacitance of this capacitor is big compared to the pixel capacitance, it requires an enormous energy consumption if an external voltage source charges the capacitor. Yet, charging the external capacitor little by little through the pixel capacitors requires a lot of cycles in our case. Hence, for the display driver developed in this Ph.D., an external capacitor is not used.

6.1.3 Generation of image-dependent waveforms

In what preceded, we proved that adding intermediate voltage levels can be useful to reduce the power consumption. We will now calculate the normalized frame energy α for four different kinds of drive waveforms and six different image patterns. The first one of the four drive schemes, A_1 , is the drive scheme proposed in Figure 5.4. The other three are more or less the same, but with small adaptations. In A_2 , an extra $0V$ is added in the middle. Instead of immediately changing the row voltage from $40V$ to $-40V$, the row is first shorted to ground in order to discharge the row

6.1 Principles to reduce the power consumption

Table 6.1: Consecutive voltage levels during 1 line time of four different bipolar waveforms

	Line select				Column FC				Column SP					
A_1	40		-40		10		-10		-10		10			
A_2	40	0	-40		10	0	-10		-10	0	10			
A_3	0	40	-40	0	0	10	-10	0	0	-10	10	0		
A_4	0	40	0	-40	0	10	0	-10	0	0	-10	0	10	0

capacitance and then the row is connected to the $-40V$ source. In version A_3 a similar intermediary state is inserted at the beginning and end (note that the terms "beginning" and "end" are in fact perfectly equivalent) of each line addressing time. Finally, in version A_4 , the row and column capacitances are discharged to $0V$ in the beginning, in the end and in the middle of each line addressing time. We already mentioned that the duration of those intermediate levels must be very small compared to the line addressing time in order not to influence the behavior of the LC. Furthermore, the duration of the intermediate zero level has to be the same for the corresponding rows and columns. The four row-select waveforms together with the column waveforms for a black and a white pixel are presented in Table 6.1. The row-non-select waveform is a constant voltage of $0V$ in each of the four cases.

The normalized frame energy ($\alpha = \Delta E_{frame} / R^2 * K * C_0$) is calculated for seven different types of images. First, there is an image with alternately black and white horizontal lines. Next, there are a complete black, a complete white and a complete gray image (without black or white pixels). The final three images are presented in Figure 10.1. All patterns are 16×16 . The results are presented in Table 6.2.

The power consumption associated with A_2 is always the same or less than the power consumption associated with A_1 . Likewise, A_4 always consumes the same or less power than A_3 .

Since A_2 and A_4 both have an extra zero level in the middle of the waveform (between the transition $40V$ to $-40V$), we can conclude that the middle intermediate $0V$ level is helpful in saving power.

Comparing A_2 and A_4 amongst one another does not seem so obvious. With the horizontal black and white line image, it is a drawback to add the extra $0V$ levels at the beginning and the end of the waveforms. For an image with black and white vertical lines on the contrary, the extra zero

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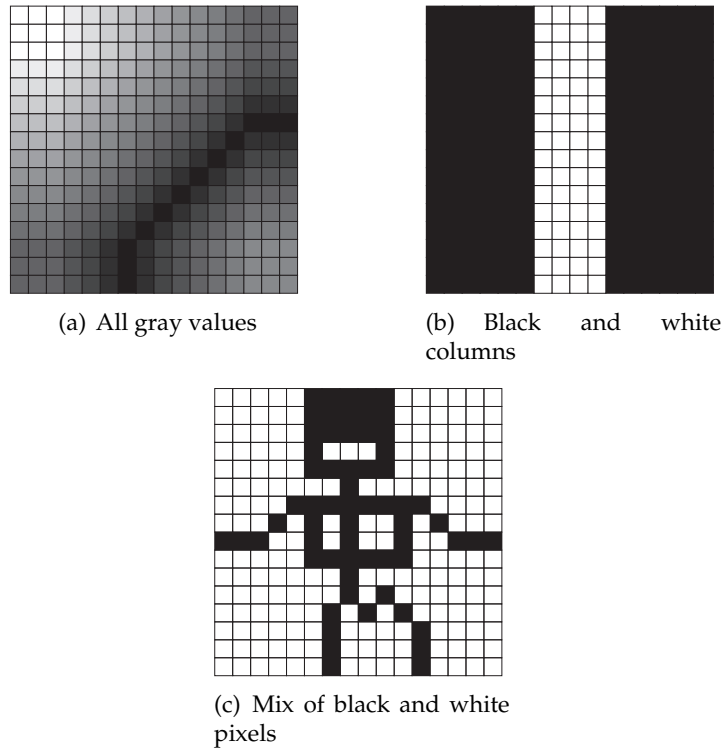


Figure 6.4: Different image patterns

Table 6.2: Normalised frame energy α ($J/F = V^2$) for different images and drive waveforms

	A_1	A_2	A_3	A_4
Horizontal lines	506	306	600	400
All black pixels	497	347	450	300
All white pixels	891	641	750	500
All gray pixels without black and white	706	706	800	800
All gray values	700	685	782	766
Vertical lines	595	420	525	350
Mix of black and white pixels	751	525	676	451

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levels at the beginning and the end of the waveforms are beneficial. So, there is no “best” waveform for all cases. The power consumption depends on the used drive scheme as well as on the displayed image.

Hence, for every image to display, an investigation is needed to determine which drive scheme includes the lowest power dissipation. Therefore some extra logic is needed to perform the calculation over and over.

6.1.4 Selective update

As the name betrays, selective update means that only that part of the screen containing different pixels compared to the previous image, is refreshed. However, since an image is refreshed row by row, all the rows containing at least one changing pixel, have to be updated. A disadvantage is that higher voltages are needed for the reset. This will be clarified further on.

Another energy-saving principle is Multi-Line-Addressing. This is not studied in this Ph.D., but is worth the effort to do so. More information can be found in [4], [5], [6].

6.2 Optimisation of the row-select and data waveforms

To compose the most power-efficient row and column waveforms for every kind of image, we start from the standard pixel voltages (see Figure 5.4) adding as many intermediate voltage levels as possible. The big advantage of a higher number of intermediate voltage levels is the reduction of the power consumption. On the other hand, there are some drawbacks. Some of them were already named before: it is not obvious to have a lot of different voltage levels at one’s disposal and when the number of intermediate voltage levels increases, all multiplexers need extra switches. Those extra switches not only take extra place on the chip (which makes the chip more expensive), they also add complexity to the chip and to the corresponding logic to drive the multiplexers. Furthermore, the level-shifters that control the switches also consume power. We have to make sure that the addition of extra switches does not consume

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more power than it saves. I decided to use only those voltage levels I need anyway to compose the waveforms. If wanted, it is possible to extend the display driver I developed in this Ph.D. with some extra voltage values.

Based on Figure 5.4, we know that the voltage levels $40V$, $10V$, $0V$, $-10V$ and $-40V$ are (all but a constant term) available. In some cases, some extra levels used for the reset waveforms are possible. For example, an extra $15V$ level is used during the reset (see further) of the cholesteric texture LCD used in this Ph.D. In what follows, we won't make use of this extra $15V$ voltage level and restrict us to the voltage levels needed during line-scanning.

Figure 6.5 shows a schematic of the rows and columns connected to the multiplexers. Every multiplexer consists of several switches that can switch to one of the voltage values mentioned above.

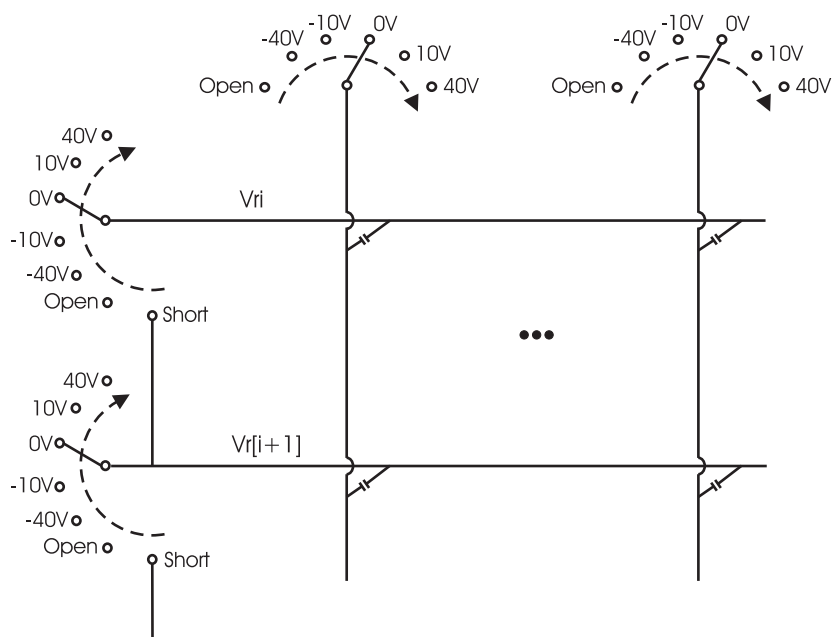


Figure 6.5: Multiplexers connected to the rows and columns

We will now try to determine the most efficient row-select waveform and

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the most efficient column waveforms. As said before, the row-non-select waveform is at a constant $0V$ level. In contrast to the waveforms proposed in Table 6.1, where the same row-select and data waveforms for every pixel with the same colour is used, we will optimize the waveforms pixel per pixel. In our analysis we will assume that the number of rows is sufficiently high, meaning that the pixels on the non-selected rows will have a much greater influence on power consumption than those on the selected row. This number varies from drive scheme to drive scheme, but is approximately about 10 rows. In practical applications, the number of rows is much higher.

Before we proved that the optimal drive scheme differs depending on the image. Therefore we will first find out the most efficient row-select and data waveform for a gray, black and white pixel. Hereby, the focus is on the transitions at half of the line time. In the second iteration, the complete row and data waveforms are composed according to the colour of the preceding or succeeding pixel by adding extra voltage levels generated by external voltage sources. Afterwards it is discussed how extra levels can be created by short-circuiting rows or columns. Next, selective update is mentioned. In the end, some alternative drive waveforms are discussed.

6.2.1 Adding intermediate voltage levels: first iteration

Image with only gray pixels

To obtain gray levels, the pixel waveform has to be a combination of the waveform for black and the waveform for white. This is realized by means of pulse width modulation (PWM). When the $10V$ level is applied, corresponding to the data signal for black, the LC molecules in the cell start to turn horizontally. However, applying $-10V$, the voltage level corresponding to the data signal for white, turns some of them vertically again and brings them in the TP state. Which percentage of the LC domains in the pixel relaxes to the FC respectively to the SP state (see section 4.1.1) depends on the duration of both levels. Their relative proportion defines the exact location on the rising slope of the electro-optical response characteristic and so the resulting reflectance. Figure 6.6 shows an example of a waveform for a gray pixel with a gray level of 33.3% ($=5/15$) white and 66.6% ($=10/15$) black. The corresponding reflectance is shown in the right figure.

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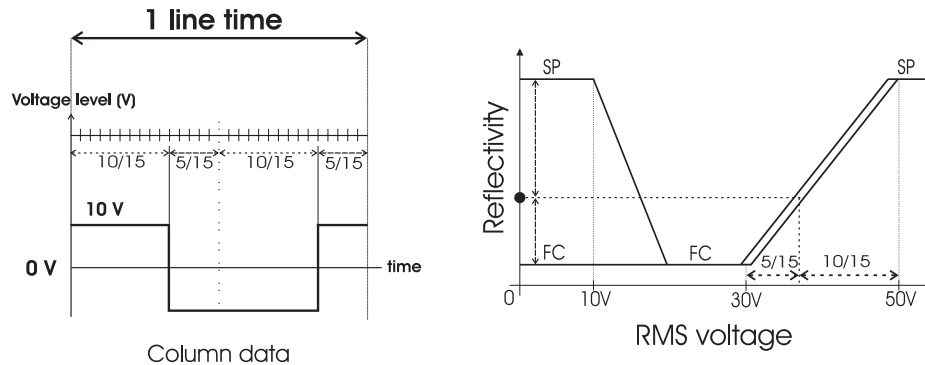


Figure 6.6: Gray pixel as a combination of black and white

The waveform profile in the second half of the line time is the inverse of the first half of the line time.

The moment the row-select waveform makes the transition from $40V$ to $-40V$ (after half a line time), the voltage in the column stays at a constant level. So, adding intermediate levels in the row-select waveform during this transition is always beneficial. It is important that the duration of the added levels is very small compared to the time step so the behavior of the liquid crystal is not influenced, but long enough to allow the system to settle. The time step is half the line time divided by the number of gray values minus one (black and white included). Figure 6.7 makes all of this more clearly. The profile of the second row voltage and an arbitrary column voltage are shown for a 3×3 display and a drive scheme that includes 14 different gray values besides black and white.

The upper curve is the waveform corresponding to the second row. During the first and the last line time, the voltage of the row waveform is $0V$. During the second line time, the row is selected and therefore the row-select waveform is applied.

The lower waveform is an example of a column waveform for a column with three gray pixels. In the first line time, the waveform corresponds to the voltage values needed for the first (row 1) pixel on that column, in the second line time for the second pixel and in the last line time for the third pixel. The first pixel has a gray value consisting of $14/15$ black and $1/15$ white. The second one is $8/15$ black, $7/15$ white and the last one $1/15$

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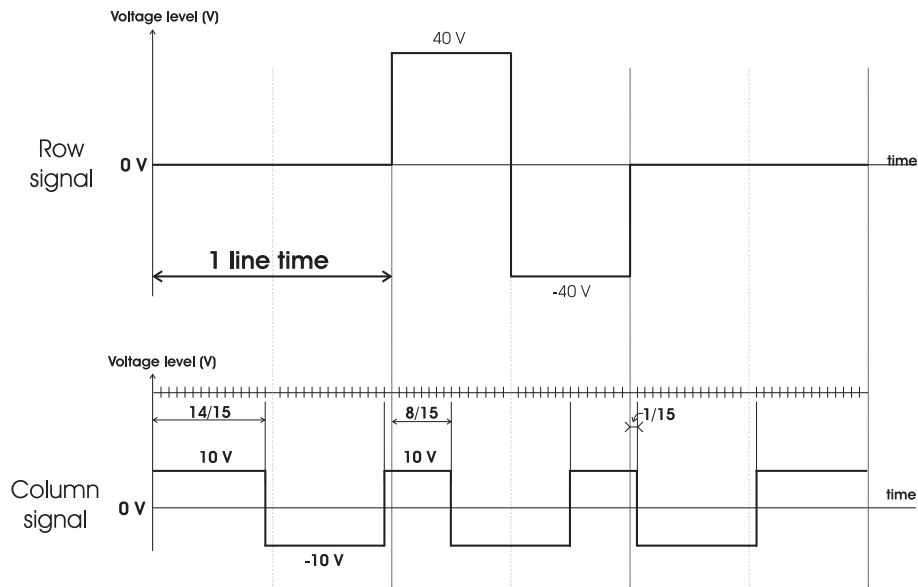


Figure 6.7: Profile of a row and column waveform in a 3x3 display

black and 14/15 white.

Now we have a general idea of the waveforms on the rows and columns during line selection, we can continue optimizing them. As said, we will add as many intermediate voltage levels as possible during the 40V to -40V transition. The available voltages are 10V, 0V and -10V, so these three are added. Except the fact that the duration of these voltage steps must be small enough compared to the time step, there are no other conditions that must be fulfilled yet. The same analysis can be made for the transition in the beginning and the end of the row-select waveform.

The moment the 10V to -10V or the -10V to 10V transition takes place in the columns, the corresponding row-select waveform stays constant, namely 40V or -40V respectively. So adding an extra 0V level is an advantage. The ideal row-select and column waveform and the corresponding pixel waveform for an image with only gray pixels are shown in Figure 6.8. In this figure, the duration of the intermediate states has been exaggerated to emphasize their effect on the waveforms. As said, the duration must be

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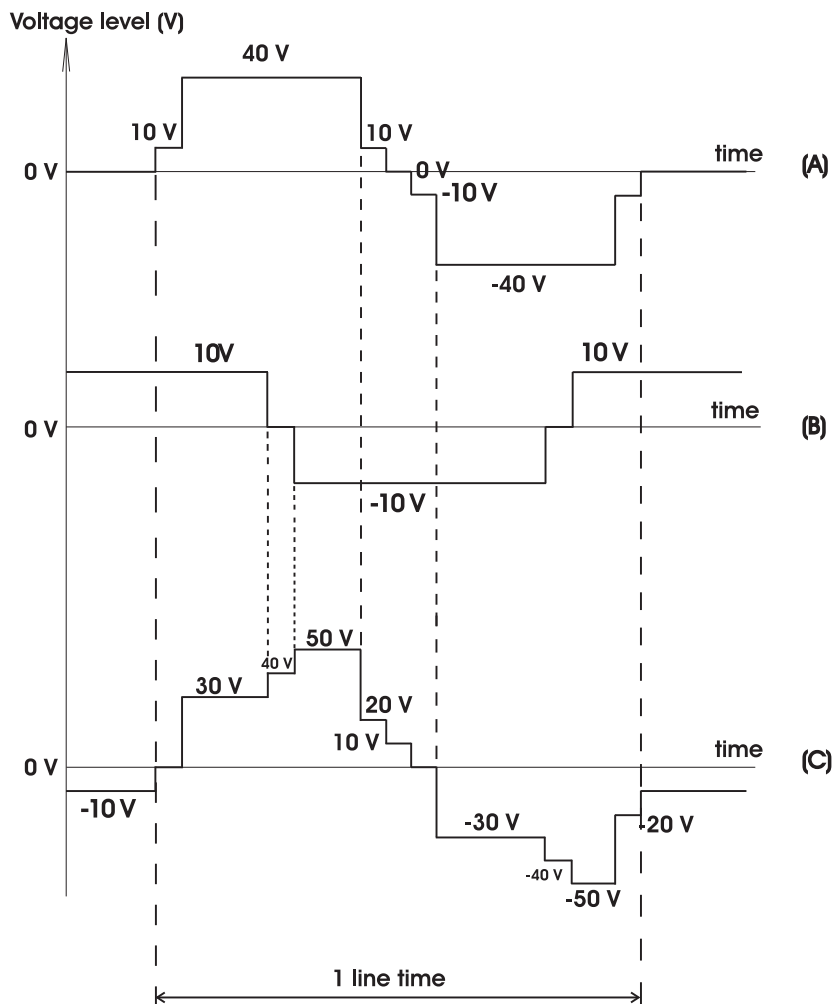


Figure 6.8: Row-select waveform (A) and example of a column waveform (B) with the corresponding pixel voltage (C) in case of an image with only gray pixels

small in relation to the time step in order to avoid a reduction of the rms value of the AC pulses. However, it should be large enough to discharge the row and column capacitances to the requested voltage.

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Waveform for a black pixel

As can be seen in Figure 5.4, the transition in the row-select waveform from $40V$ to $-40V$ takes place at the same moment the data waveforms for black and white make their transition from $10V$ to $-10V$ or inverse. This means that the exact timing of transitions and the duration of the intermediate levels becomes important. The pixel waveform of a black pixel makes a transition from $30V$ to $-30V$. Achieving an extra intermediate level during this transition can be done in two ways:

- Adding an intermediate voltage level to the row waveform during a time span in which the column voltage stays constant
- Adding an intermediate voltage level to the row waveform the same time the column voltage makes a transition

Given the important contribution of the pixels in the non-selected rows to the power consumption and the results from Table 6.2, one can already conclude that an intermediate zero level during the transition $10V \rightarrow -10V$ in the data waveform can be beneficial.

Looking back at the row-select-waveform derived for a gray image (Figure 6.8) where three extra intermediate voltage levels are added during the transition $40V \rightarrow -40V$, we can deduce that the two transitions in the data waveform have to take place at the same time of two of the transitions in the row-select waveform.

In order to have as much transitions as possible in the resulting (selected) pixel voltage, the relative position of the transitions has to be chosen well. A simple table with the resulting pixel voltage for the possible row and column voltages makes the analysis more simple (see Table 6.3).

The aim is to let the black pixel voltage drop from $30V$ to $-30V$ with as many intermediate voltage levels as possible with the condition that the added voltage level needs to be lower than the previous one (otherwise the extra transition would involve an extra power consumption). The maximum number of extra voltage levels to be added in this particular case is equal to the number of extra voltage levels during the transition $40V$ to $-40V$ in the waveform for row-selection. This means, three extra levels between $30V$ and $-30V$ are possible. Let us choose $10V$, $0V$ and $-10V$. These extra levels can be achieved by making the transitions in the row-select and data waveform as shown in Figure 6.9.

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Table 6.3: Possible row minus column voltages for a black pixel

column	10V	0V	-10V
row			
40V	30V	40V	50V
10V	0V	10V	20V
0V	-10V	0V	10V
-10V	-20V	-10V	0V
-40V	-50V	-40V	-30V

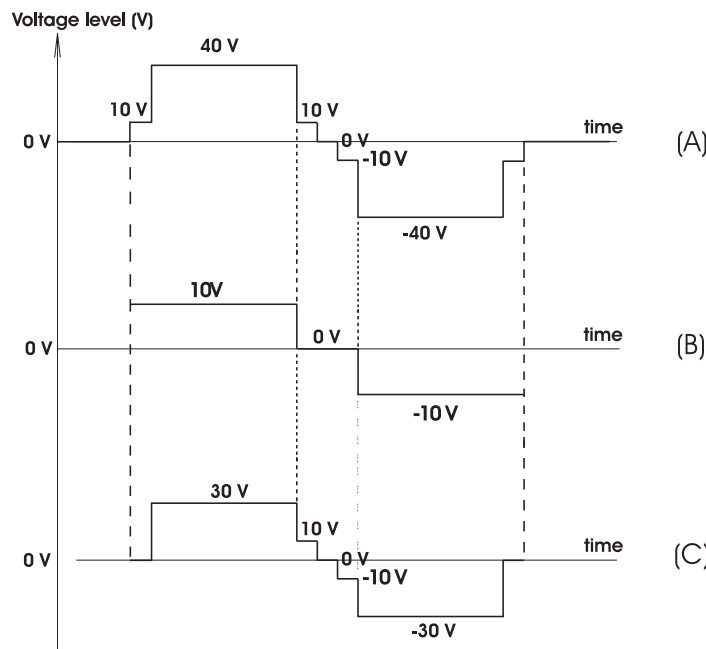


Figure 6.9: Row-select (A), data (B) and pixel waveform (C) for a black pixel

The 40V to 10V transition in the row-select waveform occurs at the same moment the data waveform goes from 10V to 0V. This results in the pixel voltage going from 30V to 10V. The transition 10V → 0V → -10V takes place during the time the column voltage stays at the constant level of 0V. The final transitions, -10V to -40V in the row and 0V to -10V in the column, also take place at the same moment. It is really important that all

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the simultaneous transitions happen at exactly the same moment. Again, in Figure 6.9, the duration of the different voltage levels are not correct, but are exaggerated to ease the understanding of the construction of the drive waveforms.

Figure 6.9 only focuses on the transitions made in the middle of a line time. What happens in the beginning or the end of a line time, is discussed further on.

Waveform for a white pixel

Contrary to the row and data waveform for a black pixel, the row and data waveform for a white pixel make a transition in the opposite direction after half a line time. This implies that there are three possibilities to add extra voltage levels to the corresponding pixel waveform:

- Adding an intermediate voltage level to the row waveform during a time span in which the column voltage stays constant
- Adding an intermediate voltage level to the column waveform during a time span in which the row voltage stays constant
- Adding an intermediate voltage level to the row waveform the same time the column voltage makes a transition

As a result the maximum number of energy-saving intermediate voltage levels that can be added to the pixel waveform (the moment the row makes the transition $40V \rightarrow -40V$) is equal to the sum of the number of intermediate voltage levels in the middle of the row-select waveform and the number of intermediate voltage levels in the middle of the column waveform plus one. In this particular case, this implies that there are five extra intermediate voltage levels possible. The possible pixel voltage levels are shown in Table 6.4. The maximum number of intermediate voltage levels is only reached in case the row and column transitions occur during a period of constant voltage on the column and row respectively.

To achieve the maximum number of intermediate voltage levels (that include a power saving), one has to choose five different voltage values from the table with the restriction that every voltage level needs to be in the same row or column as the previous voltage level and needs to have a

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Table 6.4: Possible row minus column voltages for a white pixel

column	-10V	0V	10V
row			
40V	50V	40V	30V
10V	20V	10V	0V
0V	10V	0V	-10V
-10V	0V	-10V	-20V
-40V	-30V	-40V	-50V

lower value. A possible choice is indicated in bold in Table 6.4. The corresponding row, data and pixel voltage is shown in Figure 6.10.

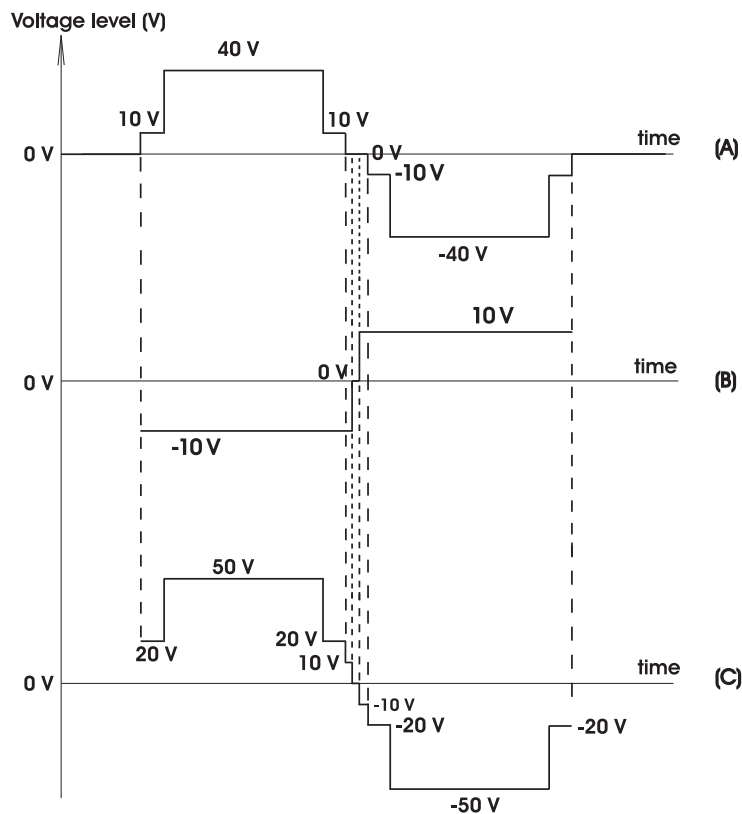


Figure 6.10: Row-select (A), data (B) and pixel waveform (C) for a white pixel

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For the row-selection as well as for the data waveforms for black and white, we added all the intermediate voltage levels that are available on the board during the transition at the middle of the line time. By choosing these transitions at the right time and with the correct duration in relation to each other, one can compose the most efficient waveforms for a gray, black and white pixel. Again we mention that the duration must be short enough in order not to influence the optical response of the liquid crystal, but long enough to allow the system to settle. Once the row-select signal is determined, one can adjust the data-signals in the appropriate way.

Next, we will complete the row and data waveforms by adding the begin and end voltage levels.

6.2.2 Adding intermediate voltage levels: second iteration

If a column contains only gray pixels, there is no voltage transition in this column at the end nor the beginning of the line time (see Figure 6.7). Therefore the exact timing of the voltage transition from $0V$ to $10V$ in the beginning or the transition from $-10V$ to $0V$ at the end of the row waveform proposed in Figure 6.8 is not important. The same applies to the beginning of the line time when a gray or black pixel is preceded by a white or gray pixel or when a white pixel is preceded by a black pixel, and at the end of the line time when a gray or white pixel is succeeded by a black or gray pixel or when a black pixel is succeeded by a white one. However in the transitions black \rightarrow gray, gray \rightarrow white, black \rightarrow black and white \rightarrow white, the data-signals in the column make a voltage step at the same moment of the row-signal. Therefore we need to study these transitions in more detail.

Transition black \rightarrow black

A sketch of the situation is shown in Figure 6.11.

When the number of rows is high enough, there are a lot more pixels on the non-selected rows than there are on the selected row. So the influence of voltage transitions over the pixels on the non-selected rows is dominant concerning the power consumption. Therefore, a zero level must be added between the transition from the $-10V$ level at the end of the data wave-

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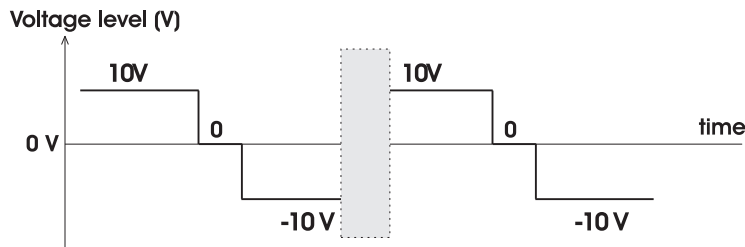


Figure 6.11: Transition between two black pixels

form of the first black pixel and the 10V level at the beginning of the data waveform of the succeeding black pixel. Now we still have to examine at what time the 0V must be applied and how long it must take. Therefore, we compare the transitions of the data-signal with the transitions in the row-select waveform. This is shown in Figure 6.12.

The upper curve is the row-select waveform corresponding to the first black pixel, the row-select waveform on the second row is the one corresponding to the second black pixel. Since the row-select and the data signal make transitions in the same direction, the optimal timing for the transitions is making a data transition at the same time of a row transition. The other row transitions happen when the column voltage stays at a constant level.

Looking at Figure 6.12, one can see that there are still two possibilities left. For example the transition from $-10V$ to $0V$ at the end of the first black data signal can happen the same moment the first row-select waveform changes from $-40V$ to $-10V$ or the moment it changes from $-10V$ to $0V$. A simple calculation shows that the first one is the most energy-efficient since the resulting pixel waveform has an extra voltage level. Also, one can see that the transition from $0V$ to $10V$ in the beginning of the second black data waveform is ideally performed the moment the second row-select waveform goes from $10V$ to $40V$.

Transition black → gray

Since the beginning of the profile of a gray data waveform is equal to that of a black data waveform, the timing and duration of the intermediate zero level at the transition from a black to a gray data signal is the same as

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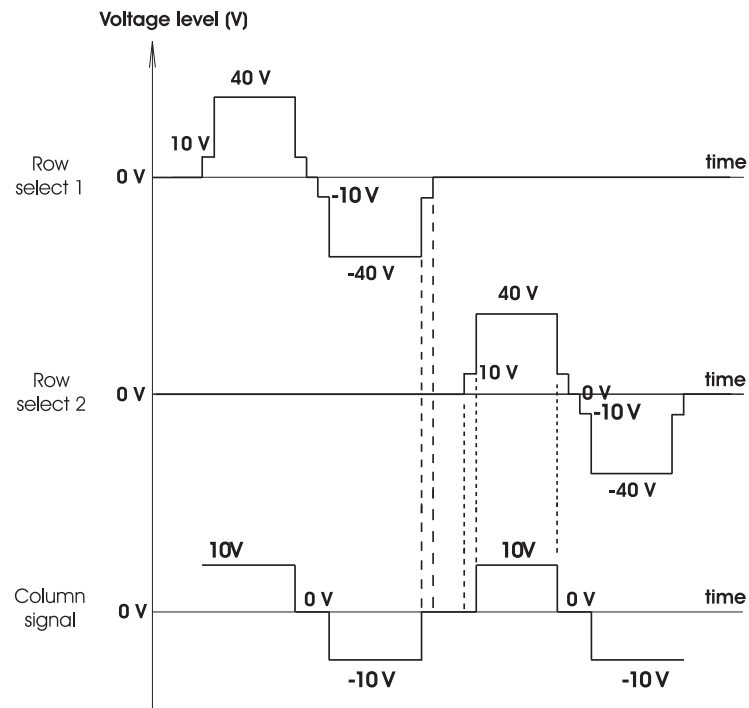


Figure 6.12: Transition between two black pixels

if the black pixel were succeeded by another black pixel.

Transition white → white

A similar analysis as of the case black → black can be made. As can be seen in Figure 6.13 however, contrary to the case black → black, the column voltage drops from 10V to -10V.

Again, since the influence of data transitions is bigger in the non-selected rows, an extra zero level must be added. The 10V → 0V and 0V → -10V transitions must take place the moment the row-select waveform is at a constant voltage value. The best transitions are shown in Figure 6.14.

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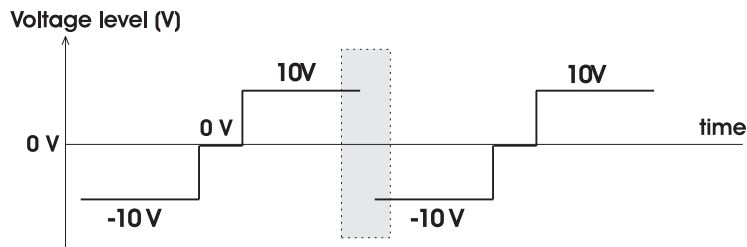


Figure 6.13: Transition between two white pixels

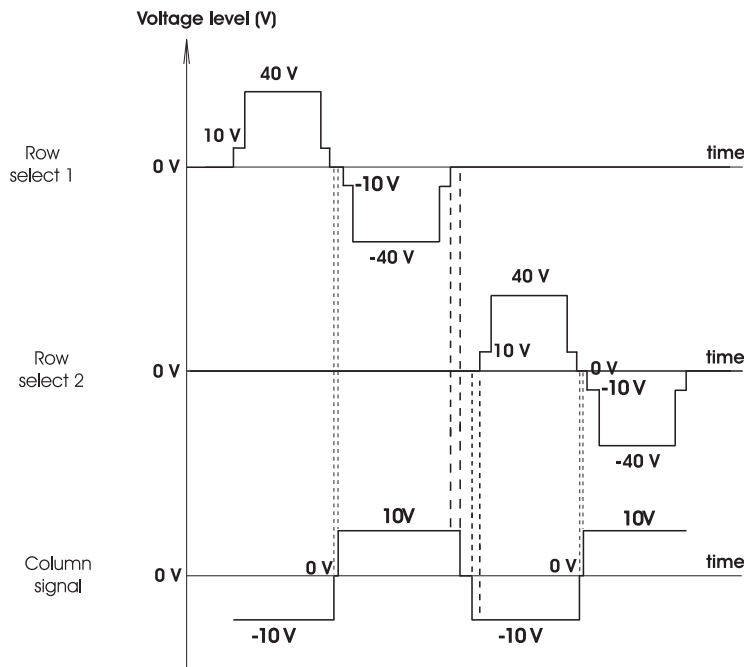


Figure 6.14: Transition between two white pixels

Transition gray → white

The profile at the end of a gray waveform is the same of a white waveform ending, so the same transitions of white → white are valid.

A summary of the possible row and column waveforms is given in Fig-

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Figure 6.15.

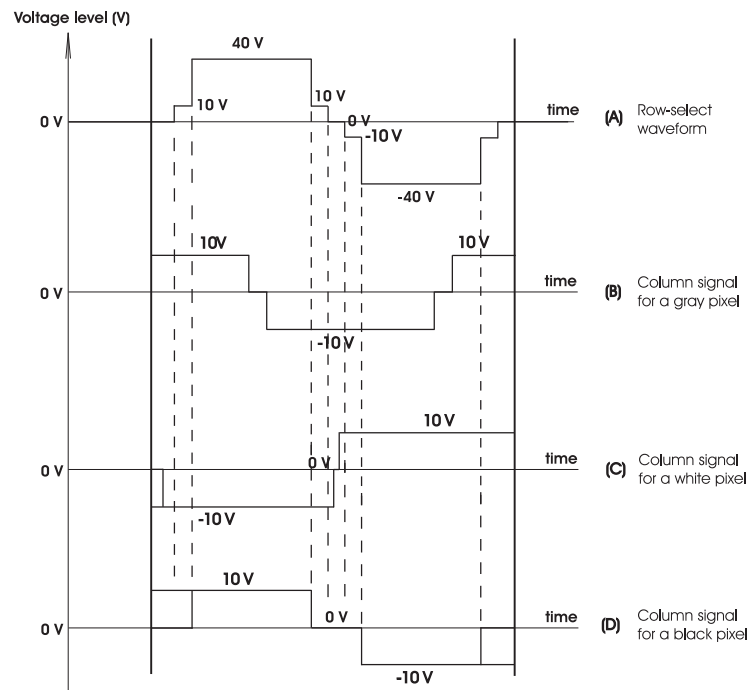


Figure 6.15: Possible transitions of the row and column waveforms

Curve (B) in Figure 6.15 represents a gray waveform, (C) the waveform for a white pixel and (D) the waveform for a black pixel. (C) and (D) show that there are two possible data waveforms for a white as well as for a black pixel.

6.2.3 Short-circuiting rows or columns

The advantages of charge recycling can not only be achieved by applying extra voltage levels to the rows or columns by means of an external voltage source, but also by short-circuiting the appropriate rows or columns. First, we will investigate how we can short-circuit the different rows and afterwards, we will look at the columns.

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Since the non-selected rows are at the constant level of $0V$, it has no use to short-circuit them mutually. So, we will focus on the selected row. Short-circuiting the selected row with a row that does not succeed the selected one is useless as well. This is so because the short-circuiting will result in a certain voltage ($\neq 0V$) on the non-selected row and an external voltage source would be needed to discharge that row again. So, only the possibility of short-circuiting the selected row with the succeeding row is left.

The row-select waveform roughly drops from $40V$ to $-40V$. Short-circuiting the selected row, which is at $-40V$ at the end of the line time, with the succeeding row, which is still at $0V$ at that moment, results in both rows being at $-20V$. Before we mentioned that the selection waveform starts at $40V$. This would mean that the succeeding row, currently selected, must be charged from $-20V$ to $40V$. One will agree that this is not the most power-efficient way to proceed.

An interesting idea would be reversing the waveforms for consecutive rows. The row-select waveform on the odd rows stays as shown in Figure 6.15, but the row-select waveform on the even rows is reversed. So, the voltage is $-40V$ in the first half of the line time when the row is selected and $40V$ in the second half of the line time. When an odd row is short-circuited with the succeeding row at the end of its row-selection time, both rows will be at a voltage of $-20V$. However, this time it is beneficial. The row that was selected first needs to be discharged from $-20V$ to $0V$ instead of from $-40V$ to $0V$. The even row that is selected afterwards, is charged from $-20V$ to $-40V$ instead of from $0V$ to $-40V$. A benefit is achieved twice. But reversing the row waveforms implies that the corresponding column waveforms also have to be reversed to make sure the pixel waveform does not change. Using the same idea of intermediate levels as explained before, we obtain the waveforms shown in Figure 6.16 for the row-select waveforms.

The differences between Figure 6.16(a) and the row-select waveform shown in Figure 6.15 are situated at the beginning and the end of the waveforms. The voltage levels of $20V$ and $-20V$ are the result of short-circuiting the $40V$ or $-40V$ level of the selected row with the $0V$ level of the succeeding row. The duration of this $20V$ level depends on the column information (similar as explained before for the waveforms in Figure 6.15).

6.2 Optimisation of the row-select and data waveforms

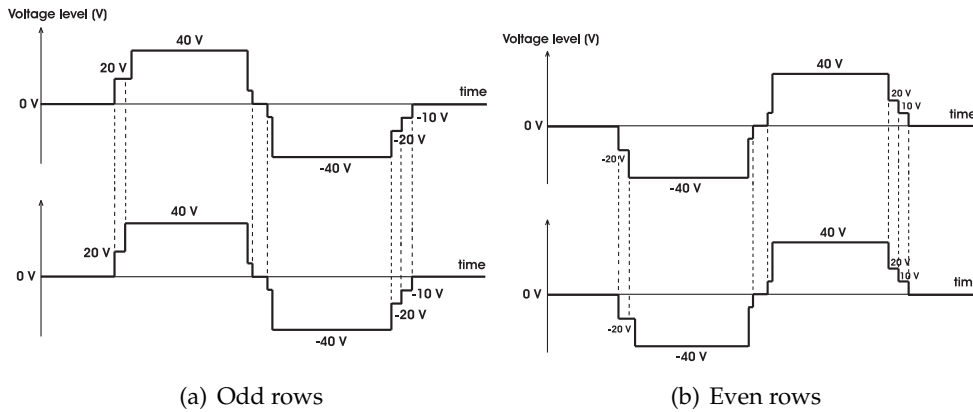


Figure 6.16: Row-select waveforms when successively selected rows are short-circuited

As mentioned before, the column waveforms have to be reversed so the pixels on the even rows remain at the correct pixel voltages. Figure 6.17 shows 3 waveforms for a gray pixel.

The first one is the one we use for an odd row and is the same as in Figure 6.15 (B). The second one is the first one reversed and therefore usable for the pixels on the even rows. However, the problem we face in this case is the transition between the 10V and -10V level that occurs in the columns each time a next row will be selected. Since these transitions increase the power consumption, we adapt the waveform for a gray pixel on an even row by switching the voltage levels of the waveform as shown in Figure 6.17. This has no influence on the image because only the duration of the voltage levels across the liquid crystal influences the pixel colour and not the exact order of the voltage levels.

For the odd rows, the column waveforms for black and white are basically the same as in Figure 6.15. For the even rows, they have to be reversed. Depending on the value of the pixel itself and the data information of the pixels on the previous and the succeeding row, a zero-level with the appropriate time duration has to be added. This is not explained in detail anymore since it is completely similar to what is explained before. Figure 6.18 and Figure 6.19 show the row and column waveforms relatively to one another if the row-selection waveforms would be those shown before in Figure 6.16. Waveform (A) represents the row-selection waveform, (B),

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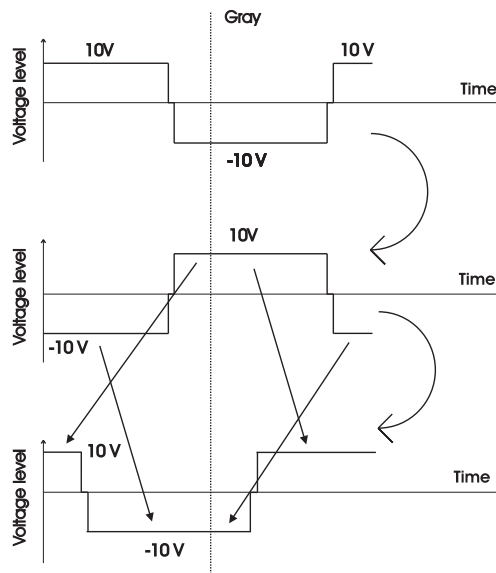


Figure 6.17: Adaptation of the column waveform for a gray pixel on an even row when successively selected rows are short-circuited

(C) and (D) are the data waveforms for gray, white and black respectively.

Charge recycling by short-circuiting can also be used for the columns. To derive in which cases this would be useful, we look at the pixel voltages in the non-selected rows since they have the most influence on the power consumption. The voltages occurring in the column waveforms are $-10V$, $0V$ and $10V$. Calculations show that it is not interesting to short-circuit to an average of $0V$. Let us explain this with an example. Suppose column 1 has a voltage of $10V$ and column 2 $-10V$ (both are not necessarily adjacent columns). The voltage can change in different cases:

- In the next step, column 1 needs to be at $10V$ and column 2 at $10V$.
- In the next step, column 1 needs to be at $-10V$ and column 2 at $10V$.
- In the next step, column 1 needs to be at $-10V$ and column 2 at $-10V$.

The third case is in fact the same as the first, so we won't discuss it.

6.2 Optimisation of the row-select and data waveforms

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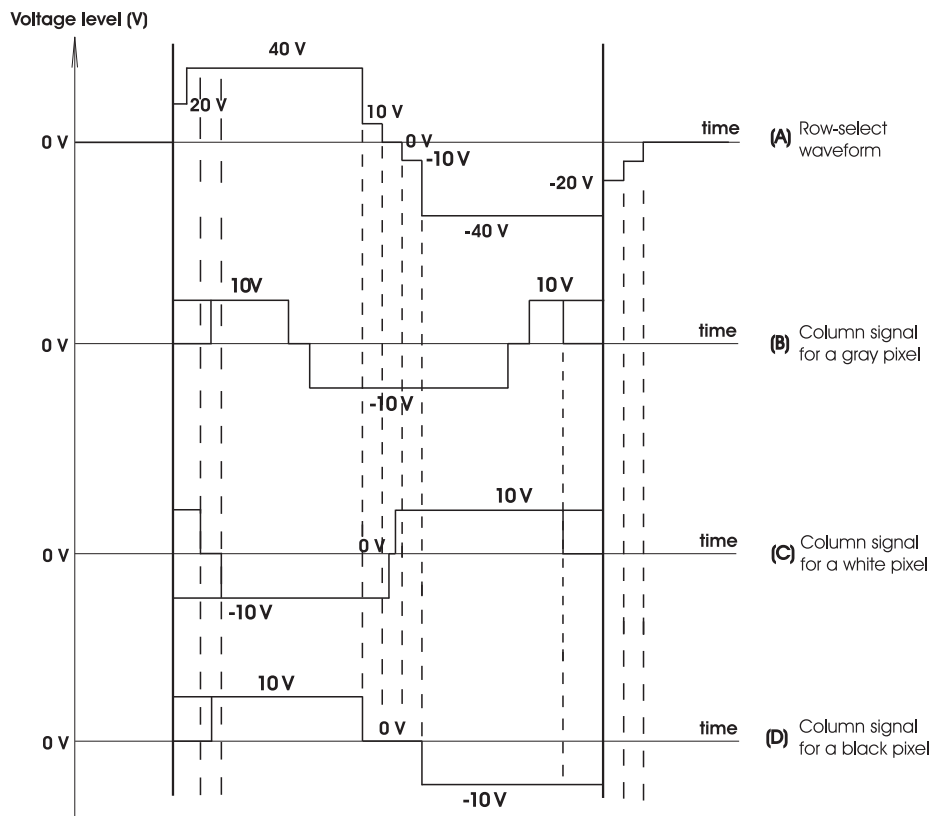


Figure 6.18: Possible transitions of the odd row and column waveforms in case adjacent rows are short-circuited

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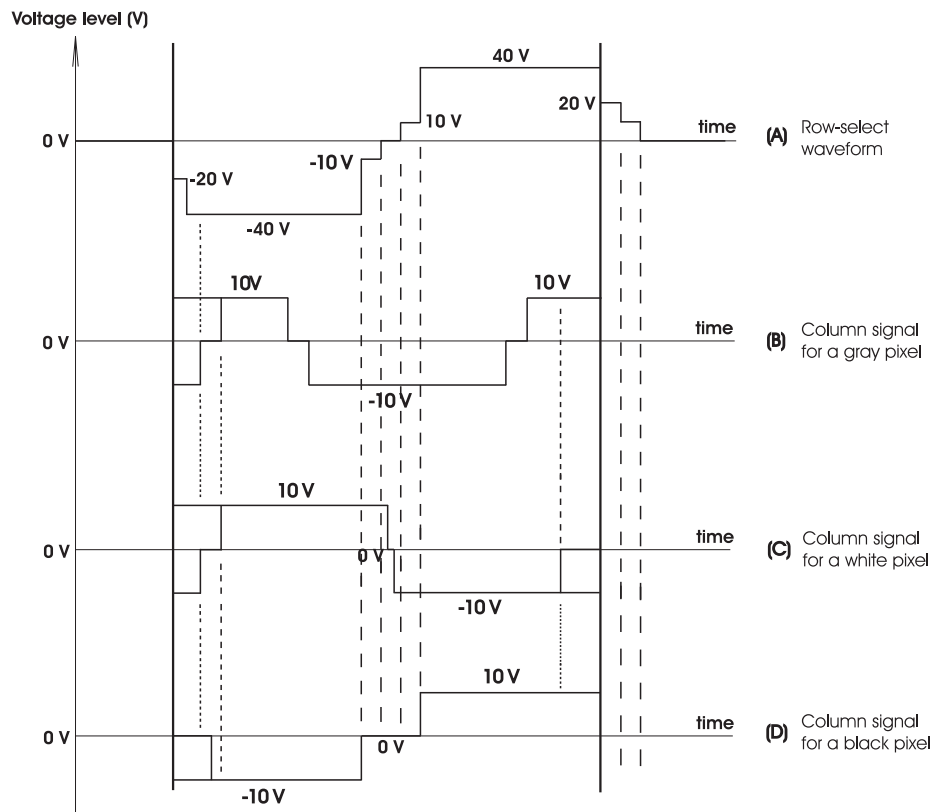


Figure 6.19: Possible transitions of the even row and column waveforms in case adjacent rows are short-circuited

6.2 Optimisation of the row-select and data waveforms

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After both rows are short-circuited, they are both at $0V$. In the first case, they have to be charged with an external voltage source to $10V$. For column 1, this involves extra power consumption since the column was originally at $10V$. In column 2 there is no gain since bringing the column to $0V$ is similar to connecting that column with ground, which does not consume power as well. So there is only loss.

In the second case, there is neither loss nor gain due to the same reason. Short-circuiting the columns mutually involves a need for extra switches, so the result is a loss and therefore short-circuiting to $0V$ is useless.

In a few cases, it is useful to short-circuit to an average of $-5V$ or $5V$. For example, let us assume column 1 needs to be discharged from $10V$ to $-10V$ and column 2 must be charged from $-10V$ to $10V$. First, column 1 is connected to ground. No power is wasted. Next, column 1 (now at $0V$) is short-circuited with column 2. As a result, both are at $-5V$. In the next step, an external voltage of $-10V$ is connected to column 1. This source has to deliver the power to go from $-5V$ to $-10V$ instead of from $0V$ to $-10V$ leading to less power consumption. For column 2, there is no difference in power consumption: after the short-circuiting, the column is connected to ground and afterwards charged with an external voltage source to $10V$.

The power saving in these two columns together during this transition is 25%. However, it is important to mention that this power saving is only reached in the case of two columns making an opposite transition at the same moment. This is only the case when there is a fair amount of black and white pixels. In fact, the profit that can be achieved by using charge recycling in the column drivers is very small. If we take into account that short-circuiting columns means more switches are needed and the complexity of the logic is increased, we decide that it is not recommended to exploit this possibility.

6.2.4 Selective update

Selective update means that only that part of the display containing pixels that change colour, is updated. So, only those rows and columns that correspond to these pixels need select or data waveforms. However, this is only advantageous when the new image differs from the previous one

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in a limited number of rows. If even one pixel in a row has to change, the whole row must be rewritten. Indeed, to change a pixel, the row-select signal is applied to the corresponding row. So all the pixels on that row are effected by the row-select signal having an amplitude of $40V$. Since the threshold voltage is only $10V$, the LC in those cells will rearrange and the pixel colour will change.

6.2.5 Alternative drive waveforms

Alternative way of DC compensation

Figure 6.6 shows an example of a waveform for a gray pixel that is composed by the waveforms for black and white. The second half of the line time is the inversion of the first half of the line time. This can also be seen as the mirror image around the time axis. Another way to compensate is to mirror around the time axis as well as mirroring around a vertical axis. An example is given in Figure 6.20 showing the column voltage of an arbitrary gray pixel as well as the corresponding pixel voltage.

Instead of two transitions in the column waveform (see Figure 6.6), there are now three transitions in an opposite direction. This is a big drawback in terms of power consumption because the course of this waveform is the same as the course of the inverse waveform over all the non-selected pixels on that column. Assuming there are several rows in the display, the contribution of the non-selected pixels is not negligible. Furthermore, these drive waveforms result in a step from $50V$ to $-50V$ over the selected pixel consuming more energy as if the waveform were to go first to $-30V$ before going to $-50V$.

Succession white → black in the composition of gray

Another alternative for composing the waveform corresponding to a gray pixel, is to apply first the voltage corresponding to a white pixel and afterwards the voltage corresponding to black. The resulting waveform for a gray is shown in Figure 6.21.

The relative proportion of the duration of the voltage levels determines the pixel colour.

The column waveform and thus the pixel waveform over the non-selected

6.2 Optimisation of the row-select and data waveforms

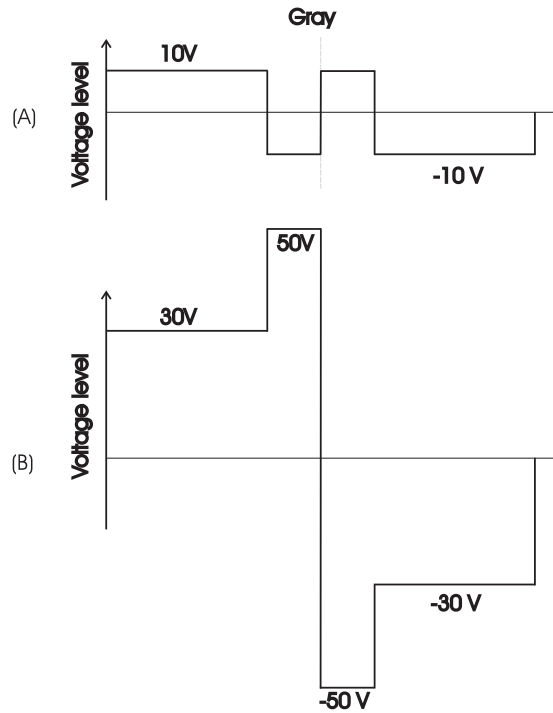


Figure 6.20: Column (A) and pixel (B) waveform in case the profile of the data waveform in the second half of the line time is the mirror image around the X and Y direction of the profile in the first half of the line time

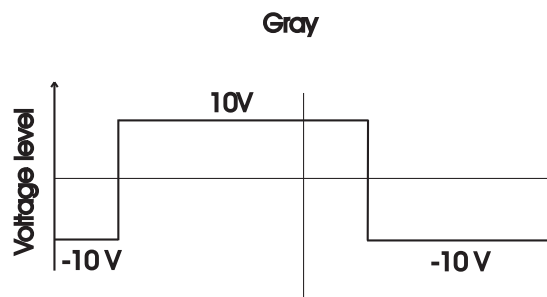


Figure 6.21: Gray pixel as a combination of white and black

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pixels has the same transition as the drive scheme proposed in Figure 6.6 (mirrored over the time axis). This means the power consumption remains unchanged in the non-selected rows if the image were composed of only gray pixels. Neither does the power consumption in the selected row change in case of a gray image. What does change is the power consumption in case of succeeding black and white pixels. Which drive scheme is the most power-efficient depends on the image. Figure 6.22 makes this more clear.

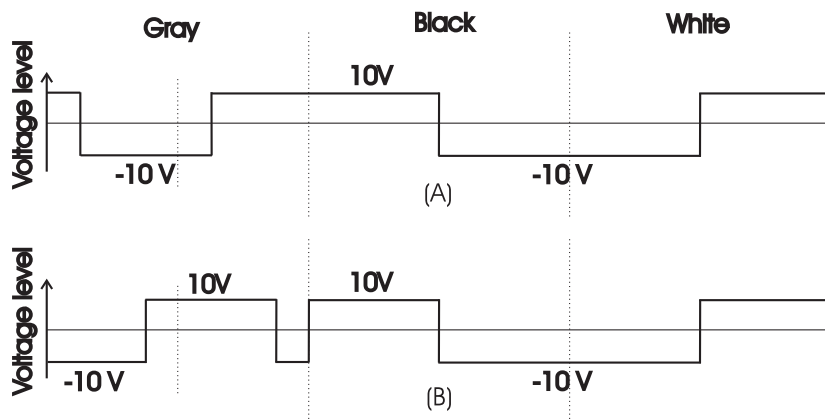


Figure 6.22: Gray pixel followed by a black and a white pixel

The first part of the upper curve (A) represents the gray pixel composed of the voltages belonging to black and white in the order black → white, the lower curve (B) in case the order white → black is used. As can be seen in the graph, the upper curve makes fewer transitions than the lower curve and therefore leads to a lower energy consumption. The opposite is true when the succession gray → white → black occurs.

Further on in this Ph.D., the data waveform for a gray pixel will always start with the 10V voltage level corresponding to black.

6.3 Optimization of the reset waveforms

During reset, the purpose is to put every pixel in the stable planar state. This has two advantages:

6.3 Optimization of the reset waveforms

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- The duration of the transition $FC \rightarrow SP$ takes $0.3s$, the transition $SP \rightarrow FC$ takes $1ms$ [7]
- Due to the hysteresis on the rising slope in the electro-optical characteristic of Figure 5.3, there is a difference in gray value between a pixel originally in the FC state and a pixel originally in the SP state.

To get the pixels in the planar state, a $55V$ square pulse is put over them. It needs to be mentioned that the voltage applied over a pixel to get a white colour is $50V$. This $50V$ voltage corresponds to the top of the rising slope, but is still on the slope of the electro-optical characteristic. While displaying, it is important that all applied voltages are part of the slope to obtain a linear set of gray values. For a reset it is important to be fully in the SP state to avoid image sticking. So a higher voltage, corresponding to the horizontal part of the electro-optical characteristic, is used.

To achieve a square wave with a $55V$ amplitude over the pixels, voltage pulses of $15V$ to $-40V$ are applied to the rows while the pulses applied to the columns change in the opposite way, from $-40V$ to $15V$. For the adaptation of these waveforms, the same principles of adding intermediate voltage levels, short-circuiting rows and/or columns and selective update are used. Of course, the reset of the display does not depend on the image that will be displayed.

Figure 6.23 shows a possible row and data waveform that can be used to reset the display making use of intermediate voltage levels.

The upper waveform is the one applied to the display rows, the lower one is applied to the display columns. The reset waveforms are applied to all the rows and all the columns at the same time. The transition between $15V$ and $-40V$ is done through the extra voltage levels of $10V$, $0V$ and $-10V$. These voltage levels are already used during line scanning and so no extra voltage sources are needed. The addition of these intermediate levels is chosen so that the resulting pixel waveform has as many different voltage levels as possible that are beneficial to the power consumption. Just like the waveforms during line-selection, the duration of the added voltages has to be small enough so they have no influence on the electro-optical response, but long enough to allow the system to settle.

Another option to reduce the power consumption is to make use of charge recycling by short-circuiting all the rows and columns of the display. For

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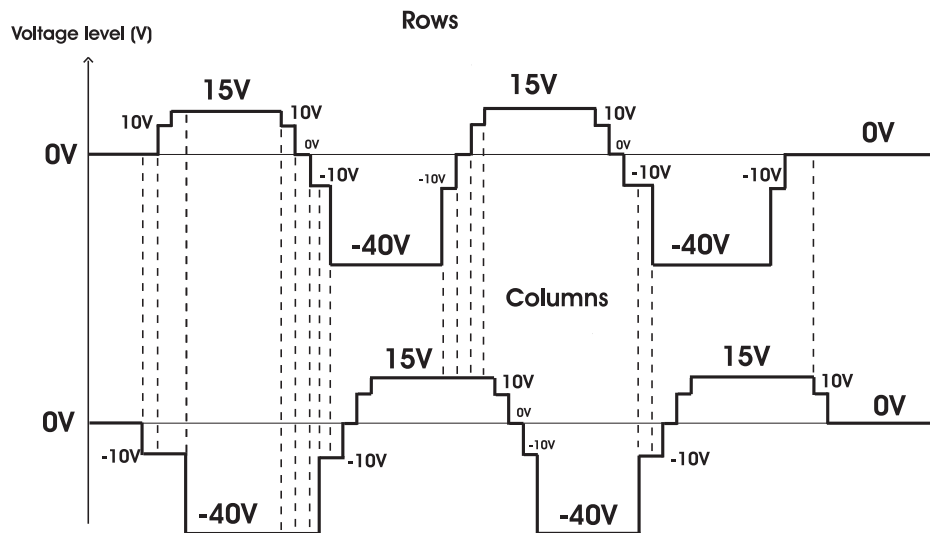


Figure 6.23: Reset pulses using intermediate voltage levels

example, the moment the rows have to make a transition from 15V to -40V (and the columns from -40V to 15V), a big power saving can be achieved by first short-circuiting them altogether since all the rows and columns will then have the common voltage of -12.5V. Meaning that the pixel capacitances have to be charged from 0V till 55V instead of starting from -55V and so implying a power saving. The result of these waveforms is shown in Figure 6.24.

As can be seen in the figure, the charging from -12.5V to 15V is done by applying the voltage levels -10V, 0V, 10V and 15V one after another. In section 6.2.3 we mentioned that we would not short-circuit the columns mutually because too many switches are needed. This problem can be eliminated with the reset pulses. The multiplexers connected to the rows and columns are all equal. Since the columns do not use the 40V voltage source, the corresponding switches providing a conductive path between the 40V source and the columns are not used. Instead of connecting the 40V voltage supply directly to the corresponding switches, we add an extra switch between the voltage supply and the switches of the multiplexers. During line-selection, the extra switch is always in the conducting state. Therefore this makes no difference compared to the situation be-

6.3 Optimization of the reset waveforms

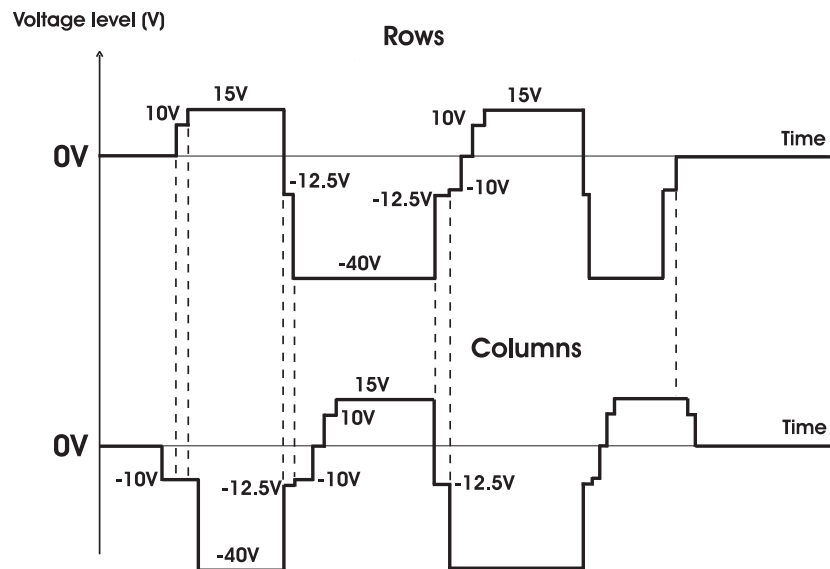


Figure 6.24: Reset pulses using charge recycling by short-circuiting all rows and columns

fore. During reset, the switch is opened. If all the rows and columns are connected to the 40V path (which is not at 40V anymore since the extra added switch is opened), this is the same as short-circuiting them all. We only need one extra switch instead of $K - 1$ ($K =$ number of columns) and we can profit from the benefit of short-circuiting.

In Figure 6.23 and Figure 6.24, only 2 reset pulses are shown. In the driver I designed, 5 reset pulses are applied during the reset phase. Normally, 1 or 2 reset pulses are enough. However, if the display has not been refreshed for a long time, more reset pulses are needed. The number of reset pulses also depends on the type of image on the display, a gray image for example is easier to remove than a pattern of black and white columns. Moreover, not only the number of reset pulses is important, but also the duration. To conserve power it is more efficient to have 2 reset pulses that take a longer time than 5 reset pulses with a shorter duration.

A final method to reduce the power consumption is selective update. As mentioned before, this means that only the rows containing pixels with another value compared to the previous image have to be rewritten. How-

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ever, this implies that a selective reset also is needed. The previously proposed reset waveforms are not appropriate because the row as well as the column voltages change with high amplitude during a reset.

To solve this problem, the drive scheme for the reset must be adapted in such a way that the voltage across the pixels on the rows needing a reset is the same as before. Furthermore, the voltage across the pixels on the rows containing not a single pixel changing colour, must be lower than a certain threshold value (see Figure 5.3).

This is accomplished by applying the same constant voltage level to all columns and those rows that do not need an update, while applying a high-amplitude bipolar voltage pulse to those rows that do need an update. By setting this constant voltage level to 15V and switching the rows that need an update between 70V and -40V, a selective bipolar reset pulse of 55V amplitude is obtained over the appropriate pixels. To minimize the power consumption, as many intermediate voltage levels as possible are added to the waveform by using the voltages that are already available on the board. The resulting row waveform is illustrated in Figure 6.25.

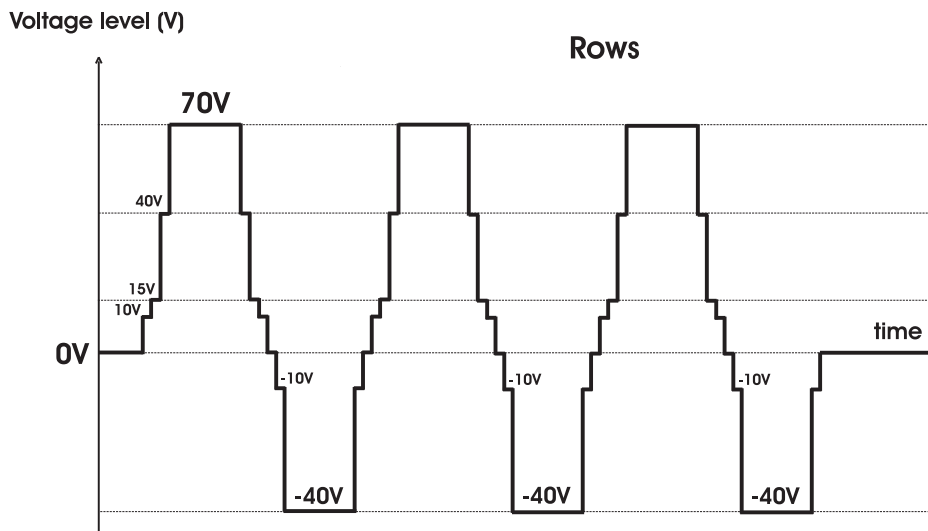


Figure 6.25: Row waveforms during the reset for a selective update

6.4 Theoretical results

6.4.1 Power consumption during line scanning

To estimate the power saving that can be realized, we compare the normalized frame energy (formula 5.13) of the discussed driving schemes with the traditional schemes A1..A4 (table 6.1) for different kinds of images. The normalized frame energy α is the total energy consumption ΔE_{frame} in the driver during the line scanning of 1 entire frame, divided by $R^2 * K * C_0$ where R and K are the number of rows and columns respectively and C_0 the pixel capacitance:

$$\alpha = \frac{\Delta E_{frame}}{R^2 * K * C_0}$$

ΔE_{frame} is the sum of all the different contributions ΔE_{tot} (formula 5.11) related to all the voltage transitions during the complete frame refresh. A more detailed description is given in section 5.2.

In table 6.2, a comparison of the normalized energy consumption for seven different images and the drive schemes A1..A4 is made on a theoretical base. Next, we will show the theoretical results for the same images when they are driven by the waveforms shown in Figure 6.15 and Figure 6.18/Figure 6.19. Both drive schemes are compared to each other as well as to the standard drive scheme A1. Figure 6.15 depicts the derived drive waveforms without the use of charge recycling by short-circuiting rows or columns. Figure 6.18/Figure 6.19 shows the derived waveforms if adjacent rows are short-circuited. Some of the images are shown in Figure 10.1. The results are shown in Table 6.5.

In Table 6.6, the power consumption of the drive scheme of Figure 6.15 is given as a percentage compared to the traditional ones. A look at A4 shows that the power saving of an image with only black pixels is only 16% and the image presented in Figure 10.1(b) 22% . However, these are not realistic images. When we look at the other image patterns, the power saving is higher. For a completely gray image, the power saving is even as high as 59%. The average power saving compared to the drive scheme A4 is 39%. Compared to A1, A2 and A3, the average power saving for the chosen images is 57%, 42% and 56% respectively.

The proportion of the power consumption of the drive scheme presented

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Table 6.5: Normalized frame energy α [$\frac{J}{F} = V^2$]

	A1	Figure 6.15	Figure 6.18/ 6.19
Horizontal lines	506	206	281
All black pixels	497	251	169
All white pixels	891	325	294
All gray pixels without black and white	706	325	306
All gray pixels	700	321	303
Vertical lines	595	272	200
Mix of black and white pixels	751	290	274

Table 6.6: Percentual power consumption of the driving scheme of Fig. 6.15 compared to the traditional ones

	A1	A2	A3	A4
Horizontal lines	41	67	34	52
All black pixels	51	72	56	84
All white pixels	36	51	43	65
All gray pixels without black and white	46	46	41	41
All gray pixels	46	47	41	41
Vertical lines	46	65	52	78
Mix of black and white pixels	39	55	43	64
Average	43	58	44	61

6.4 Theoretical results

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Table 6.7: Percentual power consumption of the driving scheme of Fig. 6.18/Fig. 6.19 compared to the traditional ones

	A1	A2	A3	A4
Horizontal lines	56	92	47	70
All black pixels	34	49	38	56
All white pixels	33	46	39	59
All gray pixels without black and white	43	43	38	38
All gray pixels	43	44	39	40
Vertical lines	34	48	38	57
Mix of black and white pixels	36	52	41	61
Average	40	53	40	54

in Figure 6.18/Figure 6.19 to the power consumption of the traditional drive schemes is given in Table 6.7.

For the chosen images, the average power saving is larger with the drive scheme of Fig. 6.18/Fig. 6.19. Indeed, Table 6.5 shows that only for the image with an alternation of black and white rows, the drive scheme of Figure 6.15 is more power efficient than the drive scheme of Figure 6.18/Figure 6.19. The usefulness of CR in the rows depends on the image that will be displayed. In fact, the use of CR includes a small energy-saving in the selected row itself, but depending on the pixel data, it is possible that there is an extra energy-consumption in the non-selected rows. It is important to mention that the results are for a 16x16 display. In a display with a large number of pixels, the influence of the non-selected rows is much bigger than of the selected rows. Therefore, the difference between both drive schemes will decrease with an increasing number of rows. Especially, when the number of rows increases, the use of CR will only have a favourable influence on the power consumption when the image contains many black and white pixels with a pronounced column-striped pattern.

For both drive schemes we can say that a power saving of about 50% is achieved. It is very clear that the novel drive waveforms always have the lowest power consumption in theory.

In the designed display driver, there is the possibility for the user to choose

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Table 6.8: Normalized reset energy β for different reset pulses

Traditional reset pulse	Figure 6.23	Figure 6.24	Figure 6.25
11495	2250	3960	2700

whether or not CR must be used for the row-select and/or for the reset.

6.4.2 Power consumption during reset

Table 6.8 compares the power consumption during reset for the drive schemes depicted in Figure 6.23, Figure 6.24 and Figure 6.25 to the traditional reset pulse. The reset waveforms are all composed of five reset pulses. The value used to compare the power consumption of the different drive schemes is the "Normalized reset energy" β , being the energy consumed in one pixel divided by the pixel capacitance (C_0) and the number of reset pulses (N). The unit is V^2 .

$$\beta = \frac{\Delta E_{reset}}{N * R * K * C_0}$$

ΔE_{reset} is the energy consumed in the display driver if the complete reset waveforms were applied to all the rows (R) and columns (K) of the display. The total energy consumed during the display reset is the energy consumed in one pixel multiplied by the number of pixels.

It is clear that the most power efficient reset pulses are those presented in Figure 6.23. However, it can be profitable to use a selective update if only a few rows need to be updated.

6.4.3 Comparison of the power consumption between different bistable display technologies

We will compare the normalized energy consumption α in a ChLCD, a BiNem LCD and an EPD. In order to calculate α two factors are important:

- the profile of the drive waveforms
- the exact voltage levels

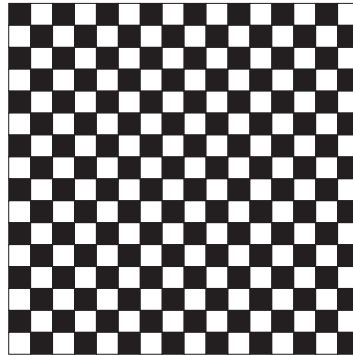


Figure 6.26: Checkerboard pattern

Table 6.9: α [$\frac{J}{F} = V^2$] for different display technologies

ChLCD	212
BiNem	48.5
EPD	219

α is calculated for the 16x16 checkerboard pattern shown in Figure 6.26.

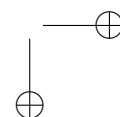
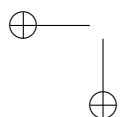
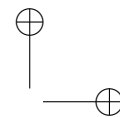
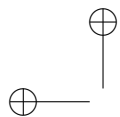
The results are shown in Table 6.9.

The result for the ChLCD is based on the drive scheme developed in this Ph.D., the result for the BiNem LCD is based on the drive waveform used by the French company Nemoptic and the result for the EPD is based on the PM drive scheme used by SiPix. One can see that the value of α is about the same for the ChLCD and the EPD, but is about 4 times less for the BiNem. Applying the algorithms proposed in this Ph.D. will lower the energy consumption in the BiNem and EPD even more.

6.5 Conclusion

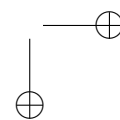
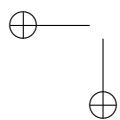
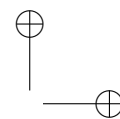
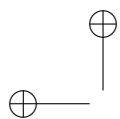
Developing a driver with extra logic that calculates the drive waveforms for every new image based on the principles of charge recycling results in a theoretical power saving of about 50%. This makes it worthwhile to design such a driver. In the next chapters, the design of the driver is described.

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Chapter 7

Description of an existing test board consisting of a ChLCD driver

In this chapter, an explanation is given of a driver that was developed before I started my Phd. With the help of this driver, a first test of the logic described in chapter 6 is possible. More specifically, the use of intermediate voltage levels, image-dependent drive waveforms and selective update can be tested. The first section depicts the block diagram of the driver. A more detailed description of the switches used in the multiplexers is given in section 7.2. Section 7.3 describes the test board that was developed to drive a 16x16 cholesteric texture LCD (ChLCD).

7.1 Block diagram of the driver

Research on power consumption reduction in bistable display drivers is not new. For a number of years people at our research lab have already been investigating the hardware part of bistable cholesteric texture LCD drivers. Some new CMOS-circuits were developed, for example power-efficient level-shifters, high-voltage (HV) multiplexers and HV generators [1]. Figure 7.1 shows the simplified block diagram of a low-power HV driver developed a while ago [2].

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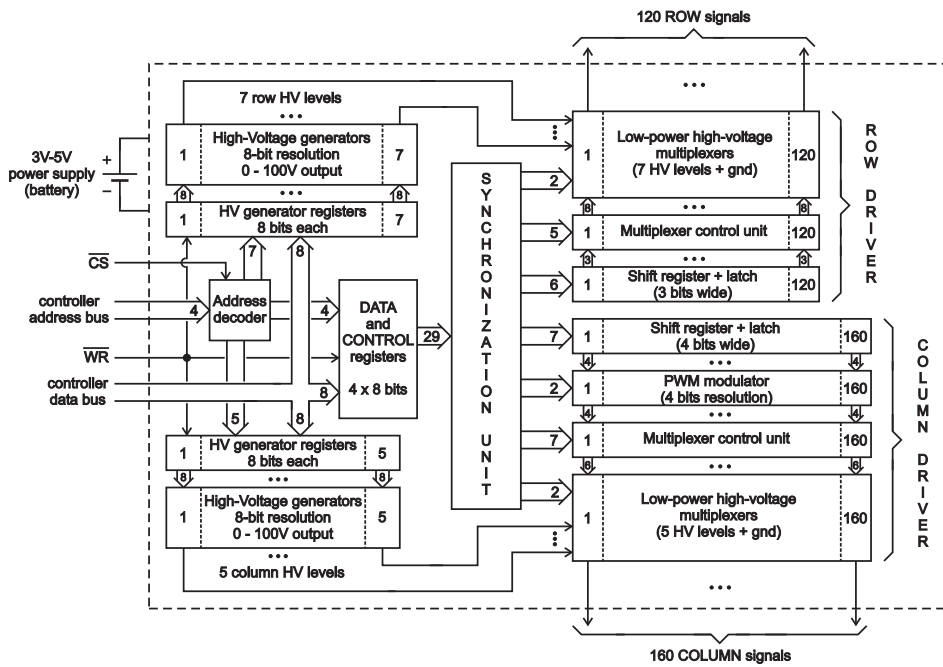


Figure 7.1: Block diagram of the low-power HV bistable display driver ALPHA3D.

7.2 Design of the switches

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This chip contains all the necessary electronics to drive a 120x160 passive matrix ChLCD using a 3V to 5V battery power supply with a minimum of internal power consumption. Even the HV levels are generated internally (with the exception of the external inductors used for voltage boosting) by a set of 12 digitally programmable high-efficiency charge-pumps. Each of these converts the 3V to 5V battery power supply into 1 out of 256 linearly distributed voltage levels between 0 and 100V. The outputs of the 12 HV generators are applied to the low-power output multiplexers of the row and column drivers responsible for synthesizing the required waveforms. In the display driver, data and control bits are processed serially. The shift register and latch are responsible for a serial-to-parallel conversion. Based on this information and a number of mode-selection bits, the appropriate switches in the output multiplexers are selected. A pulse-width modulator produces 4-bit gray levels, but it is possible to convert them internally into Amplitude-Modulated gray scales as well. The operation of the entire chip is controlled by 16 internal registers that are directly accessible from a microcontroller through a standard data, address and control bus architecture.

The user passes the appropriate data and control signals to the driver each time a new image must be displayed. An appropriate choice of these control signals generates the correct addressing scheme. For example, a bipolar or unipolar driver operation [3] can be selected, as well as a high-speed dynamic [4] or a low-speed conventional addressing scheme. One can also generate a global reset before the line scanning.

7.2 Design of the switches

A major problem in the development of high-voltage driver chips lies in the design of the level-shifter circuits needed for converting the 3V digital signals into appropriate high-voltage signals to control the DMOS transistors in the high-voltage switches of the output multiplexers. The level-shifters in standard high-voltage display driver chips continuously dissipate power, an important drawback for battery-powered applications. Examples of the schematics of such a conventional high-voltage level-shifter and accompanying high-voltage output stage are shown in [5] and [6].

In order to solve this severe problem of continuous power consumption, a

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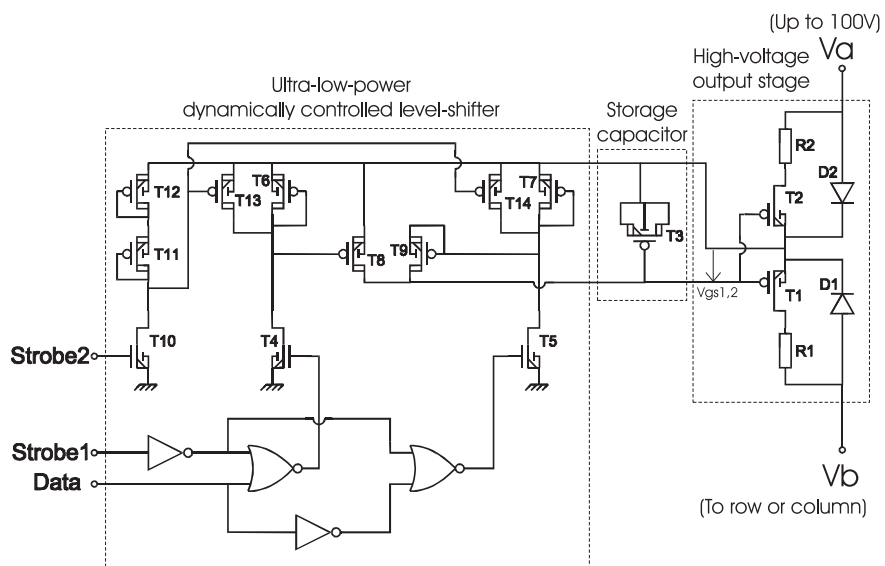


Figure 7.2: Circuit schematics of a micro-power HV analogue switch.

7.2 Design of the switches

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completely new level-shifter architecture with no static power consumption at all was designed [7] [8]. Figure 7.2 shows the schematics of a high-voltage analog switch, as used in the output multiplexers of the presented driver chip, employing this new type of low-power level-shifter. The operation of this low-power level-shifter is controlled by two special Strobe signals. When the Strobe signals are activated, one of the 2 transistors T4 or T5 (according to the logical value of the Data signal) will carry a $30\mu A$ drain current, causing a voltage drop of approximately $4.7V$ over the p-type load transistor T6 or T7. For a "0" bit at the Data input, the $4.7V$ drop across T6 switches on transistor T8. Consequently the source-gate capacitance of the p-type DMOS transistors T1 and T2 is completely discharged (i.e. $V_{GS1,2} = 0V$). T1 and T2 will switch off and the high-voltage switch between the nodes Va and Vb will insulate the two nodes. For a "1" bit at the Data input on the other hand, the $4.7V$ drop across T7 will pull down the gate potential of T1 and T2 through transistor T9 (used as a p-n diode between its drain and bulk). Thereby yielding a source-gate voltage $V_{GS1,2}$ of approximately $-4V$ for the T1 and T2 output transistors, hence activating T1 and T2, resulting in a bi-directional conductive path between the nodes Va and Vb. When the Strobe1 signal is switched to "0", T4 and T5 are switched off and consequently, T8 will also be turned off (if the Data input was a logical "0" during the Strobe pulses) or the 'diode' T9 will be reverse-biased (if the Data input was "1"). In both cases, the gate electrodes of the p-type DMOS transistors T1 and T2 become electrically insulated from the rest of the level-shifter circuit. As a result, the charge that was previously stored on their gate capacitance during the Strobe1 pulse (i.e. $V_{GS1,2}$ equal to $0V$ or $-4V$, according to the Data signal) will remain unchanged until the next Strobe pulses are applied. This unique 'dynamic charge control' approach, where the gate capacitance of the DMOS output transistors is used as a kind of dynamic memory cell whose charge is updated at the rhythm of the strobe signals synchronized to the data flow, yields an enormous reduction in power dissipation. This only applies if the duration of one strobe pulse can be kept very short compared to the duration of one bit of input data (since power is consumed only during the strobe pulses!). This is definitely the case for bistable LCD drivers as these bistable LCDs usually require very low image frame rates. To improve the performance of this low-power level-shifter even more, some extra features have been added in the schematics of Figure 7.2. Transistors T10 to T14, activated directly by the Strobe2 signal, were added in order

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to ensure that the active loads T6 and T7 are completely discharged after each Strobe1 pulse. The pulses Strobe1 and Strobe2 are set high at the same moment. The duration of Strobe2 is the same or a bit longer than Strobe1. Without this feature, sub-threshold currents in T8 might cause charge leaking from the gate capacitance of T1 and T2 in between consecutive Strobe pulses. The effect of parasitic charge leaking can be reduced even further by adding transistor T3, acting as a storage capacitor in parallel to the gate capacitance of T1 and T2. Finally, diodes D1 and D2 combined with the resistors R1 and R2 prevent the triggering of substrate currents in T1 and T2 due to reverse conduction under certain operating conditions.

7.3 Description of the test board

The driver used for the test board is not the one depicted in Figure 7.1, but a similar one able to generate the signals for 12 rows or columns. The high voltages are generated by an external voltage source instead of on-chip. A photograph of the 12-output driver chip, designed in the 100V 0.7 μ m CMOS I²T technology (Intelligent Interface Technology) of AMIs, is shown in Figure 7.3. The display being used is a 16x16 cholesteric texture LCD of which the first three rows are connected to the output of the driver corresponding to the first row. Similarly, the final three rows are connected to the output corresponding to row number 12. The same applies for the columns. This way, two 12-output display drivers drive the 16x16 display.

The test board consists of two parts. The first one contains all the necessary components needed to generate the control signals for the row and column driver. The second part, the driver board, contains the drivers and the connections to the display. The two parts are connected by a flat cable connecting the 24-bit control signals from the first board to the driver chips on the second one.

A picture of the first part of the test board is shown in Figure 7.4. The schematic is shown in Figure 7.5.

An important component on the board is the DS89C420 microcontroller. From an external computer, the appropriate data and control signals are sent to the microcontroller through an RS232 cable (section 8.1.1 explains this in more detail). To incorporate the possibility to work stand-alone, an

7.3 Description of the test board

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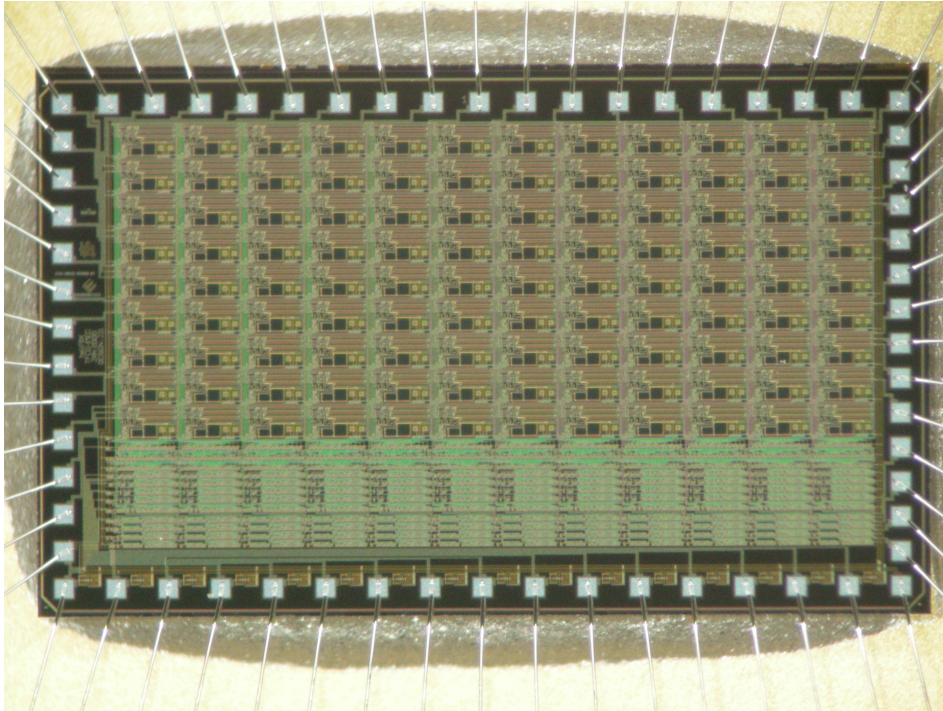


Figure 7.3: Photograph of the 12-output driver

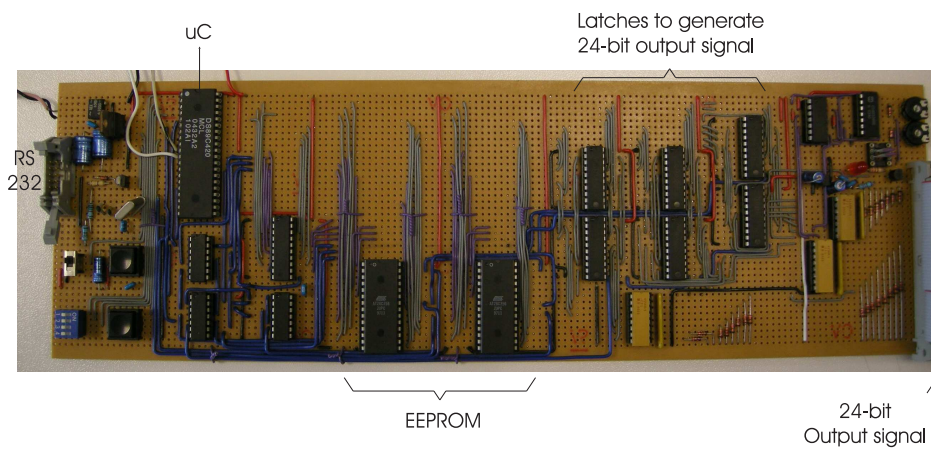


Figure 7.4: Test board containing the logic to send the 24-bit control signals to the display driver

7.3 Description of the test board

EEPROM memory (AT28C256) was added to the test board. This way, the data and control signals (of four images in our specific case) can be stored in the EEPROM. By means of DIP switches and a push button, the user is able to display one of the images stored in the EEPROM. More specifically, the position of the DIP switches determines which of the four patterns stored in the memory must be displayed. When pushing the ‘start’ button, the microcontroller reads the appropriate memory block in which the data and control signals belonging to the chosen image are stored. These signals are then applied to the output latches (DM74LS373N).

By means of an inverter and some OR ports, the correct chip-enable pulses for the EEPROM and the enable pulses for the six latches (upper right in Figure 7.5) controlling the 24-bit output signal are generated. The EEPROM consists of two separate chips to enlarge the memory range.

The output signal connected to the driver board is a 24-bit signal. The data-bus P0 of the microcontroller is an 8-bit bus. Therefore, three latches are needed to hold the three 8-bit signals. Three extra latches being enabled at exactly the same time are needed to generate the 24-bit output signal synchronously.

The 24-bit output signal is connected to the driver board. A picture of the driver board is shown in Figure 7.6.

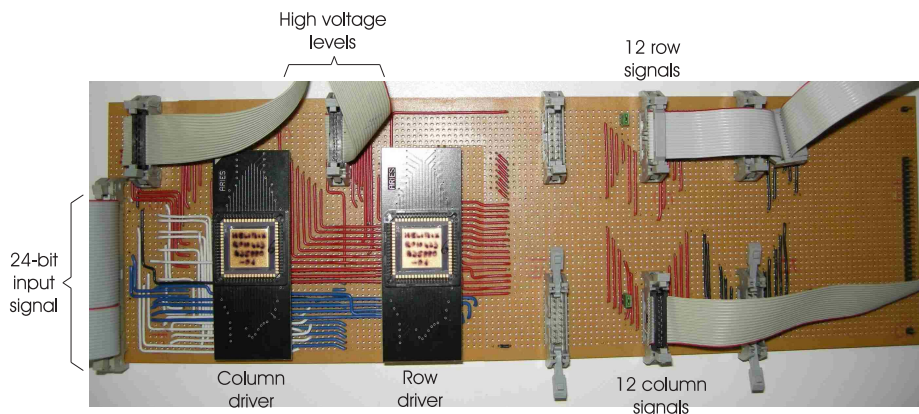


Figure 7.6: Driver board

There are two drivers on the board. One generating the 12 (16) row signals and one generating the column signals. Both drivers are connected to a set of high voltages (input connectors situated near to the drivers). Based on

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the 24-bit input signal, the drivers apply the correct voltage values to the row and column connector. There are three row and column connectors on the board. The mutual difference is the way the 12 driver outputs are connected to the 16 rows or columns. Only one of each is used. As mentioned before, I chose those where the first (last) row (column) output of the driver is connected to the first (last) three rows (columns) of the display. These signals are then connected to the rows and columns of the cholesteric display (Figure 7.7).

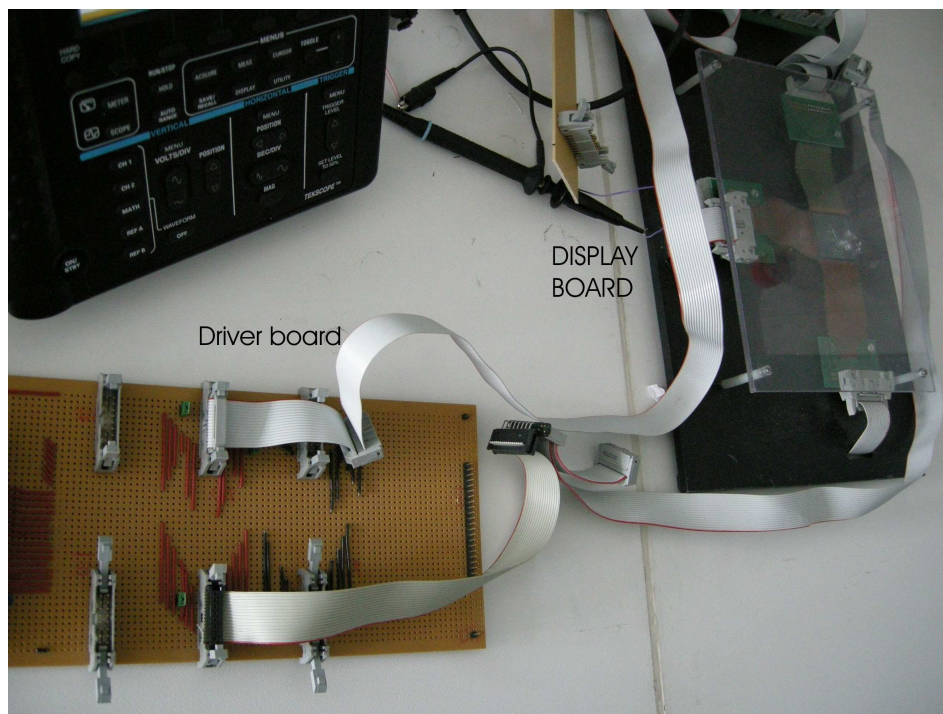


Figure 7.7: Connection between the driver board and the cholesteric texture LCD

The display board is shown more clearly in Figure 7.8.

7.4 Conclusion

The major drawback of the system described in this chapter, is the fact that all the control signals are fixed the moment they are stored in the

7.4 Conclusion

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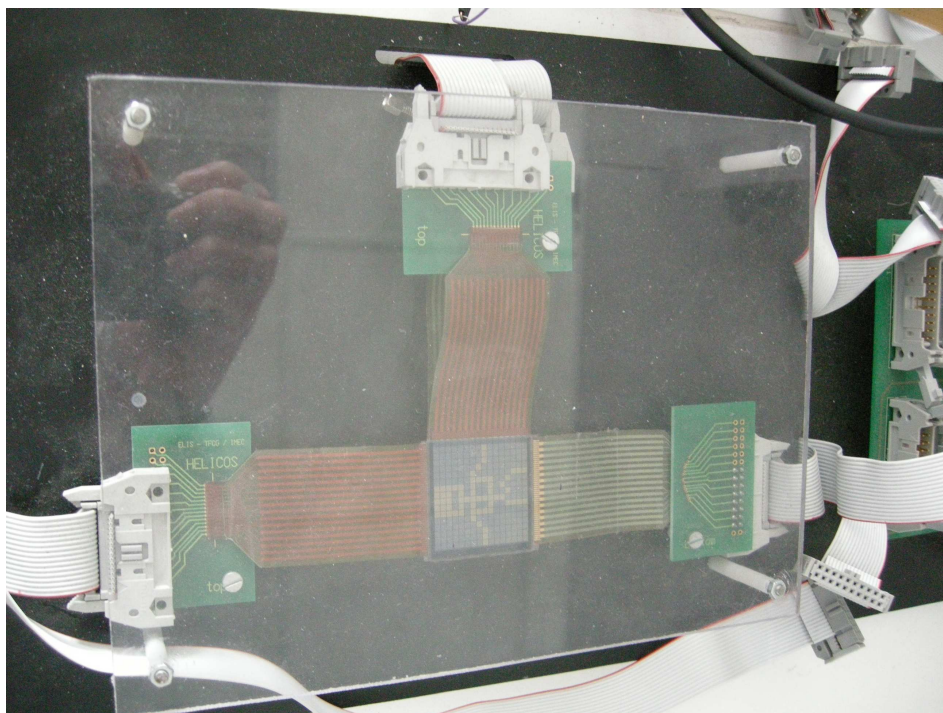


Figure 7.8: Picture of the display board

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EEPROM. This means that they already have to be calculated by the user. Once a particular addressing scheme is chosen, one can not manipulate it any further.

In the next chapter, we will explain how this existing test board is used to test the influence of some of the waveforms described in chapter 6.

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Chapter 8

Testing of the power-efficient waveforms by means of an existing test board consisting of a ChLCD driver

This chapter describes how the hardware presented in chapter 7 is adapted to test the influence of some of the waveforms described in chapter 6. The goal is to develop a driver able to drive a display with a minimum use of power only needing the data information as input. This in contrast to the driver described in chapter 7, which also needed the control signals applied by the user. With the help of the existing board, it is possible to test the use of intermediate voltage levels and the generation of image-dependent waveforms. The influence of short-circuiting adjacent rows or columns can not be tested yet since the necessary switches are not provided. The use of selective update can also be tested with this driver. This chapter explains how the hardware of the existing driver board is changed and how software is developed in order to implement the developed logic and measure the energy consumption. At the end of the chapter, the results of the measurements done with this test equipment are discussed.

Testing of the power-efficient waveforms by means of an existing test board consisting of a ChLCD driver

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8.1 Implementation of the software and adaptation of the hardware in order to set up the test board

To be able to test the advantage of the drive signals described in chapter 6, the test board was adapted in a small way. An extra communication channel is added to set up a communication line between a computer and the driver board. Some resistors are added to measure the power consumption and the microcontroller is reprogrammed. The communication between a computer and the driver board is important to allow the user to create text files containing the image information of a certain pattern and send this information to the memory on the driver board. The tasks of the microcontroller can be divided as follows:

- to store the image information sent from the computer into the EEPROM memory
- to read the appropriate image information from the EEPROM memory when this image needs to be displayed
- to calculate the most power-efficient row and column waveforms
- to send the correct data and control signals to the display driver

In what follows, the adaptations to the test board are discussed. The two main challenges were software related. The first one was situated on the computer side, more specifically the setup of the communication between the computer and the microcontroller; the other one was the implementation of the developed drive logic into the microcontroller.

First, the hardware and software to set up the communication between the computer and the microcontroller is explained. Then the implementation of the drive logic into the microcontroller is handled. Afterwards, the hardware and software to measure the power consumption are discussed.

8.1.1 Communication between the computer and the test board

Serial interface

In chapter 7, we mentioned the existence of the ability to send data from a computer to the driver board. This was realized by connecting an RS232

8.1 Implementation of the software and adaptation of the hardware in order to set up the test board 155

cable between the serial port of the computer and the driver board.

The display patterns were stored in a simple text file. To communicate with the microcontroller, a programme was written in Borland C. That programme reads the display pattern from the text file and sends this information together with all the control signals through the serial port to the microcontroller.

Since Borland C is getting out-of-date, it seemed a good idea to modernize. Hence, C++ from the Visual Studio environment was chosen to set up the interface between computer and driver board. However, Microsoft Windows XP applies a strict control over its I/O ports and does not allow any user to write to the serial port. To circumvent that problem, the PortTalk driver was installed. This driver can be called from the C-programme.

The goal of the C-programme also was to read the text file specified by the user containing the pixel information of the image to display. If wanted, the user can also choose the line time (the time during which one row is selected) of the drive signals and where exactly the image must be stored in the EEPROM memory. All the information is then sent to the UART (Universal Asynchronous Receiver/Transmitter) from the computer that converts the bytes to binary electrical impulses. Through the RS232 cable that is connected to the computer's serial port, this data is sent to the driver board.

USB interface

The most challenging part about the communication channel between computer and microcontroller was the adaptation to Windows XP and Visual C++. The communication itself is still done through the serial port of the computer. Since the newest computers often do not contain an RS232 serial port anymore, it is an interesting idea to set up the communication through the USB (Universal Serial Bus) port. This task was given to a thesis student. To create a more user friendly interface, the choice was made to use C# as development environment. Figure 8.1 shows the interface of the developed application.

The program allows one to store an image in the on-board memory and to choose an image to display. It is also possible to store a set of 16 images at once in the on-board memory. Besides the pixel pattern, the line

Testing of the power-efficient waveforms by means of an existing test board consisting of a ChLCD driver

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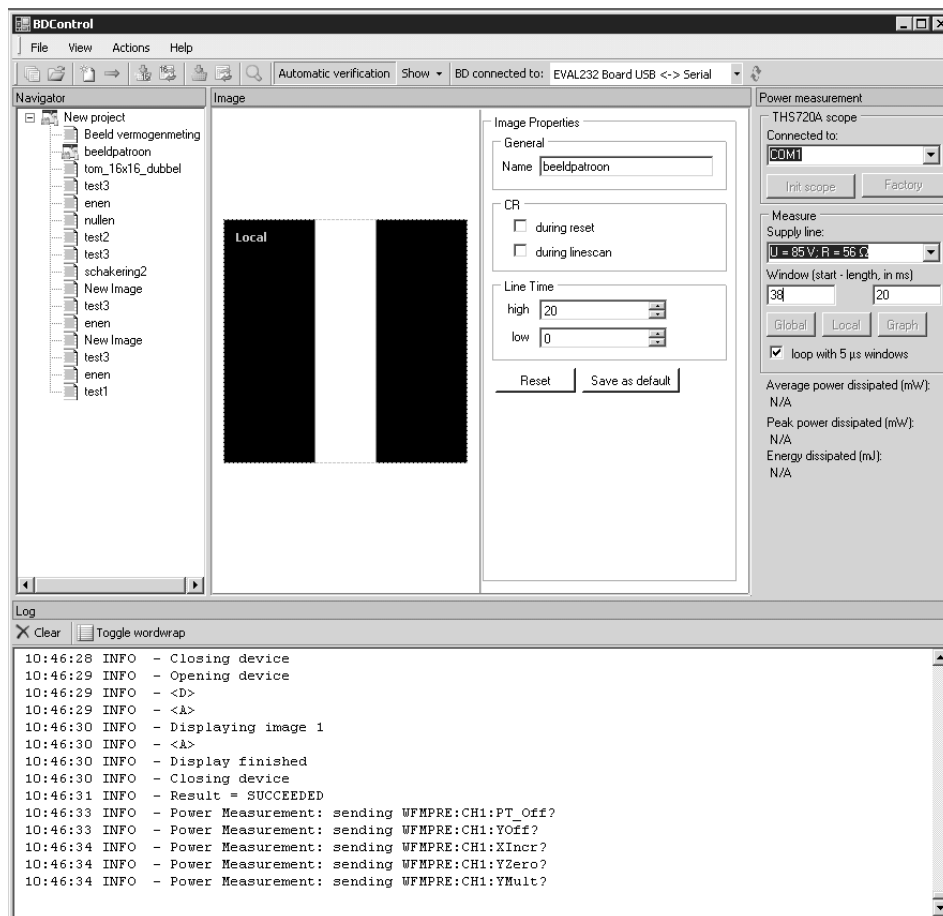


Figure 8.1: User interface to communicate with the printed circuit board

8.1 Implementation of the software and adaptation of the hardware in order to set up the test board 157

time and whether or not charge recycling must be used during reset or line-scanning must also be filled in by the user. This program was written during the last year of my Ph.D. and is meant for the printed circuit board (PCB) that was developed later on. The memory on that PCB board is a flash memory (AT29C010A). Flash is a specific type of EEPROM that is erased and programmed in large blocks instead of byte by byte. Therefore, the software to write images (and the accompanying image information) to the flash differs a little from the software that writes images to the EEPROM.

Another feature of this program is the ability to communicate with the THS720A oscilloscope. This is very interesting when measuring the power consumption. The program is written so that the user has to specify which resolution needs to be used and which range in time has to be measured. When finished, the resulting energy consumption during that time is displayed. It is also possible to display the measured waveform onto the computer screen. More information can be found in [1]. This program is used to measure the power consumption in the driver described in chapter 9.

8.1.2 Implementation of the drive logic into the microcontroller

In chapter 6, the profile of the optimized drive waveforms was discussed. The second step is translating the profile of these drive waveforms into the assembler programming language.

Since the display driver on the test board does not allow the use of charge recycling, only the influence of intermediate voltage levels, the adaptation on the image information and the selective update can be tested. Since the advantages and drawbacks of selective update are obvious, this is not tested anymore. Furthermore, the use of selective update is limited to images only differing in a few rows from the previous image.

Figure 6.15 shows the row-selection and some possible column waveforms. The composition of the column signals depends on the colour information of the pixels on that particular column. For a gray pixel, the column signal that must be applied when the pixel is selected only depends on the exact gray level of the pixel itself. The beginning of a white pixel and the ending of a black pixel can change in accordance with the colour of the previous and the succeeding pixel respectively. Therefore the microcontroller also needs to compare the adjacent pixels. Based on

Testing of the power-efficient waveforms by means of an existing test board consisting of a ChLCD driver

that information, the column signals can be composed.

Once the calculation is done, the correct data and control signals can be sent to the driver. As already mentioned in chapter 6, the timing of the signals that control the driver switches, is very important.

8.1.3 Measurement of the power consumption

Hardware

In order to measure the power consumption, a small board is developed on which some resistors are added. Between every high-voltage source and the connection of this voltage to the row or column driver a resistor is placed. By measuring the voltage over these resistors, one can calculate the power consumption.

Software

The voltage over the resistors is measured by means of an oscilloscope. A waveform captured by the oscilloscope consists of 2500 data points. These data points can be sent to a computer through an RS232 interface. Programs like excel or matlab can import the data and reconstruct the waveform if wanted.

The display driver consists of a low-voltage and a high-voltage part. We will only calculate the power consumed in the high-voltage part. This is done by adding the power delivered by the different high-voltage sources.

$$P_{total} = \sum P_{source}$$

The power delivered by a voltage source can be calculated by means of the resistor placed in the power connection.

$$\begin{aligned} P_{source} &= V_{source} * I_{source} \\ &= V_{source} * \frac{V_{resistor}}{R} \end{aligned}$$

8.2 Measurement results

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R is the resistor value, chosen small enough so the influence of the voltage over the resistor is negligible, but large enough to be observable.

To determine the energy delivered by the voltage source, the voltage change over the resistor during the complete frame time (the time the whole display is written) has to be known.

$$E_{source} = \frac{V_{source}}{R} * \int V_{resistor} * dt$$

To compare the usefulness of the different drive schemes, the energy consumption is measured two times. Once with the display connected to the driver and once without. The energy consumed when no display is connected to the driver, in other words the energy consumed in the level shifters, can also differ for each drive scheme since a difference in the number of voltage transitions, and hence the number of times the switches open and close, can exist.

8.2 Measurement results

The energy consumption is measured for the three images depicted in Figure 10.1 and for both the drive scheme A4 and the one presented in Figure 6.15. These measurements were done manually and took a very long time because the energy pulses needed to be measured twice (once with and once without the display connected to the display) for each of the seven HV sources. Moreover, during one linetime, drive scheme A4 contains 33 pulses and the drive scheme presented in Figure 6.15 counts 68 pulses. The different pulses had a width of about $5\mu s$ and the spacing between some of them was about $800\mu s$. Since the aim of the measurements was to have a global idea about the correctness of the developed theory, I decided not to measure the energy consumption during the complete frame time, but only during one line time. The resulting 'normalized frame energy' α is calculated based on the energy consumed during that one line time.

$$\alpha = \frac{\sum E_{source}}{R * K * C}$$

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Table 8.1: Measured values of α for the images shown in Figure 10.1

	$\alpha(V^2)$	
	Figure 6.15	A4
All grey values	361	642
Black and white columns	229	353
Mix of black and white pixels	361	507

R represents the number of rows (16), K the number of columns (16) and C the pixel capacitance. In order to have an idea about the display capacitance, we short-circuit all the rows and columns respectively. This way, all pixel capacitances are placed in parallel and the resulting display capacitance is the sum of all these pixel capacitances. The value of the display capacitance can be measured with a simple circuit as shown in Figure 8.2.



Figure 8.2: Circuit to measure the display capacitance

If a square wave is applied to this RC circuit, the display capacitance is charged or discharged with a certain time-constant $\tau = R * C$. The time-constant can be measured by an oscilloscope and the resistor value is known. This way, we can calculate the display capacitance. However, since the capacitance is determined by the liquid crystal state as well, the result will not be correct. This is caused by the fact that the relation between the capacitance and the voltage value over the liquid crystal is not linear [2]. Since the most important aim is to compare the measurement results of the different drive schemes to one another, the exact capacitance value is not that important.

The measurement results are given in Table 8.1.

8.3 Conclusion

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Table 8.2: Theoretical values of α for the images shown in Figure 10.1

	$\alpha(V^2)$	
	Figure 6.15	A4
All grey values	321	766
Black and white columns	272	350
Mix of black and white pixels	290	451

The theoretical values of α for the same images are repeated in Table 8.2. The main conclusion is that the measured energy consumption is less when the drive scheme proposed in Figure 6.15 is used compared to the drive scheme A4. For the three proposed images, the average energy consumption is 37% less.

Compared to the theoretical results, the same trends are observed and the order of magnitude is the same, but the exact values differ. This is due to the fact that the theoretical values are based on the energy consumption during the complete frame time and the measured values are the result of measurements during the first line time only. Moreover, the dependency of the pixel capacitance on the voltage over the cell is an important unknown factor. However, the aim of the research, which was to prove that the drive scheme proposed in Figure 6.15 is more energy-efficient than drive scheme A4, is reached.

To form an idea on the order of magnitudes, we compare the power consumption of the ChLCD proposed in [?] with the one proposed in this Ph.D. (theoretically), both containing 800x600 pixels each the size of $0.4 \times 0.4 \text{ mm}^2$. The update rate is 12ms. The first one amounts to 190mW (difference between power consumed during image generation and between image writes) while mine is 34mW. However, one should bare in mind that I assumed that the pixel capacitance was the same although this could differ.

8.3 Conclusion

With the help of an existing driver board, it was possible to test the influence of a new drive scheme that uses intermediate voltage levels and

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adapts the drive waveforms to the pixel information. The measurement values confirm the theoretical analysis proving that the implementation of these principles provides good results in reducing the energy consumption.

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Chapter 9

Optimization of the hardware

In this chapter, the newly developed integrated driver is presented. This driver has a completely different architecture than the one described in chapter 7. Only the high-voltage switches are basically the same. But even they are optimized. The first section describes the block diagram of the driver consisting of an analogue part and a digital part. The analogue part, more specifically the design of the multiplexers and the optimization of the switches, is discussed in section 9.2. Section 9.3 discusses simulation results of the switches and the designed analogue chip. Section 9.4 shows the way the digital logic is implemented in an FPGA. The last section presents the practical implementation of the driver.

9.1 Block diagram of the integrated display driver

The major drawback of the driver in Figure 7.1 is that once the type of addressing scheme has been determined, one can not manipulate the waveforms any further. To solve this problem, an extra logical block can be added to the driver. The purpose of this logical block is to calculate the most appropriate waveforms to be applied to the rows and columns of the display in order to achieve minimum power consumption. The user only needs to specify which image must be displayed, the duration of the pulses and whether or not charge recycling must be used. This contrasts to the first presented driver where the user has to specify what the applied waveforms will look like. The added logical block calculates the

most power-efficient waveforms for the rows and columns for each specific image. The resulting block diagram of the new driver is shown in Figure 9.1.

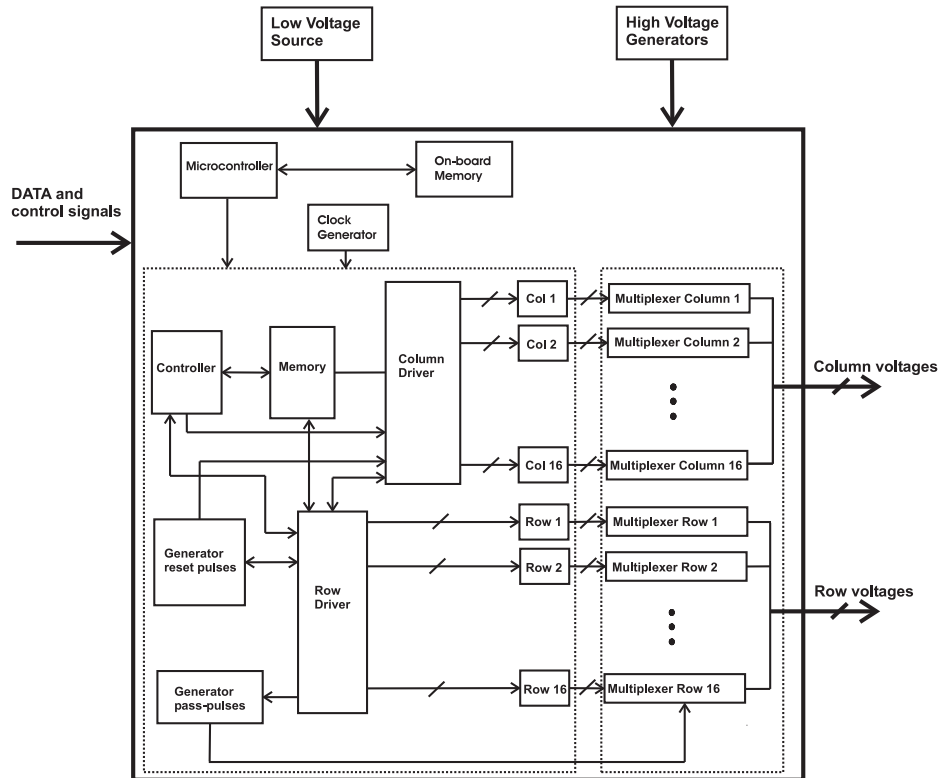


Figure 9.1: Block diagram of the proposed minimum-power HV bistable display driver.

The block diagram can be divided into 3 parts: the two parts indicated in dotted lines and the components outside the dotted lines. These last ones are a microcontroller and on-board memory amongst others. The main task of the microcontroller is to take care of the communication between an external computer, the on-board memory and the FPGA (Field Programmable Gate Array). The FPGA is represented by the first framework indicated in dotted lines. It contains the digital logic calculating the waveforms to drive the display based on the methods explained in chapter 6. The analogue part consisting of the HV analogue multiplexers, the

9.2 Optimization of the switches and design of the multiplexers 167

second framework indicated in dotted lines, is connected to the rows and columns of the display. The schematic of a multiplexer is shown in Figure 9.3. The digital part ensures the right switches are closed at the right moments. More specifically, a 4-bit input is provided for each multiplexer indicating which switch has to be closed combined with the pass-pulses specifying the opening and closing time of the switches. The analogue part of the driver is discussed in section 9.2. The realization of the digital part is explained in section 9.4.

9.2 Optimization of the switches and design of the multiplexers

The schematic of the switches is copied from the driver that was developed before (see chapter 7) and is shown in Figure 7.2. Changes include the transistor values and the layout of the switch. The length and width of the transistor channels are adapted in accordance with the driver demands. More specifically, an optimal equilibrium is found between the time needed to bring the row or column voltage to the level set by the voltage source and the current. A short switching time is wanted to decrease the duration of the intermediate voltage levels of the drive waveforms as much as possible. However, a restriction of the maximum current is desired to reduce the power consumption. Another practical limitation is set by the HV source: the maximum current that can be delivered is $10mA$. Besides optimizing the dimensions of the transistors, I also investigated whether or not it is beneficial to replace the transistors T_4 and T_5 by a cascode. Figure 9.2 makes this more clear.

Generally, the cascode arrangement offers high gain, high stability, and high output impedance. The aim of the cascode is reducing the current in the active load. However, the drawback is that the time needed to charge the pixel capacitors is higher. Indeed, since T_4 and T_5 are DMOS transistors, their channel length is a fixed value determined by the technology in which the chip is designed. This means that there is a lower limit for the proportion W/L and thus for the current in the level-shifter. A lower current results in a slower charging of the gate capacitances of T_1 and T_2 and therefore a slower charging of the display capacitance. Whether or not the cascode configuration should be used depends on the application.

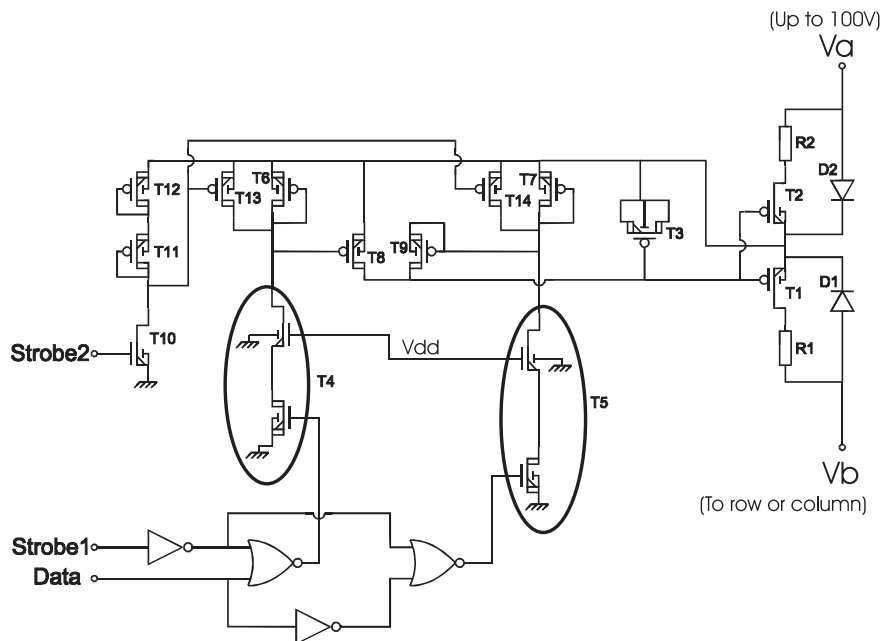


Figure 9.2: Use of a cascode in the switch

I designed the switches without the cascodes so the duration of the Strobe pulses can be less than $4\mu s$.

After optimizing the design of the switches, the schematic of a multiplexer consisting of eight switches is designed. There are nine different situations that can occur in the multiplexer, meaning there are nine possible output values:

- the low reset voltage
- the high reset voltage
- the low row-select voltage
- the high row-select voltage

9.2 Optimization of the switches and design of the multiplexers 169

- the low data-signal voltage
- the high data-signal voltage
- the zero-level voltage
- short-circuiting the succeeding row
- open

The schematic of the multiplexer is shown in Figure 9.3. Each switch has a different HV input. HV 8 is connected to the HV output signal of the succeeding row. To provide the ability to switch to the right HV level, a 4-bit input is added representing the positions the multiplexer has to switch to. These four bits are converted to 8 bits. Every one of the eight bits is connected to a different switch. The schematic of the four to eight bit converter is depicted in Figure 9.4.

One analogue driver chip contains eight multiplexers and is therefore able to drive eight rows or columns. The schematic is given in Figure 9.5. One can indeed see that the schematic of the complete chip consists of eight blocks. These are the eight multiplexers with the 4 to 8-bit converter integrated. So, each block has a 4-bit data input and one high-voltage output. At the right side, two signal lines for the strobe signals are used (also called pass pulses). The strobe signals of the different multiplexers are connected since they all need to be driven at exactly the same time. The seven lines to the left of the schematic represent the seven high voltage inputs generated by an external voltage supply source. A connection between adjacent multiplexers also exists, allowing the possibility of short-circuiting the output voltages.

To obtain a usable chip, it is not sufficient to have a schematic. The following task is the design of the layout of the chip. Since the length and width of the transistors in the switches are different compared to the switches used in the existing driver, the layout had to be redesigned. It is a full-custom layout meaning that it is an analogue chip for which parametric cells for the HV components are at hand, but no digital standard cells can be used. As usual, the aim is to decrease the dimensions of the chip as much as possible. The area of the chip is 9.43mm^2 , the package is a PLCC68 (Plastic Leaded chip carrier with 68 pins). The design is done through an MPW-run (Multi-Project Wafer) of Europractice. The technol-

ogy in which the chip is designed is the $100V$ $0.7\mu m$ *CMOS I²T* technology (Intelligent Interface Technology) of AMIs. The layout of one switch is shown in Figure 9.6.

The layout of the complete multiplexer is shown in Figure 9.7. One can see the structure of the eight switches on top of one another, with the 4 to 8-bit converter below.

The layout of the chip containing eight multiplexers and the necessary connections to drive eight rows or columns is given in Figure 9.8. The width of the chip layout is $4.1mm$, the height is $2.3mm$.

This chip is given the name DILA being the abbreviation of 'Driver for Intelligent Line Addressing'. A picture of the designed chip is depicted in Figure 9.9.

One can see the eight multiplexers side by side. In every multiplexer, the eight switches placed above each other can be recognized. Around the chip are the bond paths used to make an outside connection. The discussed schematics and layouts are made with the help of the development software Cadence.

9.3 Simulation results

In this section, the results of some simulations done with Cadence, are given. To simulate the driving of a display, we assumed that the first four outputs of the driver chip are connected to a row and the final four outputs are assumed to be column outputs. A capacitor is added between every row and column. The capacitor value is $33.2pF$. The 4-bit digital input applied to the first multiplexer first switches the output of the first row to $5V$, then to $60V$ and $45V$. The result is shown in Figure 9.10. The output to the first row is shown together with the course of the pass-pulses.

It is clear that the correct voltage values are switched to the output. Every time a pass-pulse occurs, the output voltage drops a little and is recovered when the pass-pulse is finished. This is due to the level-shifter current during the pass-pulses.

Figure 9.11 shows the $5V$ to $60V$ transition in detail.

It takes $8\mu s$ for the row output to reach its end value. The shortest intermediate voltage level takes $16\mu s$. So a switch behavior as in Figure 9.11 is fast enough. The rise and fall time of the pass pulses are determined by

9.3 Simulation results

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Cadence. In reality, they are less than $10ns$.

The current delivered by the $60V$ source is depicted in Figure 9.12.

The peak current is almost $6mA$. The transitions in the other rows and columns are similar. Still worth mentioning are the events that occur when two rows are short-circuited. Therefore, we simulate the following example. Suppose the digital inputs for row 3 and row 4 are as follows:

Row 3:

- $0 \rightarrow 120\mu s$: 0101 (= $45V$)
- $120\mu s \rightarrow 130\mu s$: 0100 (= $55V$)
- $130\mu s \rightarrow 150\mu s$: 0111 (= $85V$)
- $150\mu s \rightarrow 160\mu s$: 0100 (= $55V$)
- $160\mu s \rightarrow 170\mu s$: 0101 (= $45V$)
- $170\mu s \rightarrow 180\mu s$: 0011 (= $35V$)
- $180\mu s \rightarrow 200\mu s$: 0110 (= $5V$)
- $200\mu s \rightarrow 210\mu s$: 1000 (= short-circuit next row)
- $210\mu s \rightarrow 220\mu s$: 0000 (= all switches open)
- $220\mu s \rightarrow 240\mu s$: 0011 (= $35V$)
- $240\mu s \rightarrow 300\mu s$: 0101 (= $45V$)

Row 4:

- $0 \rightarrow 200\mu s$: 0101 (= $45V$)
- $200\mu s \rightarrow 210\mu s$: 0000 (= all switches open)
- $210\mu s \rightarrow 260\mu s$: 0110 (= $5V$)
- $260\mu s \rightarrow 270\mu s$: 0011 (= $35V$)
- $270\mu s \rightarrow 280\mu s$: 0101 (= $45V$)
- $280\mu s \rightarrow 290\mu s$: 0100 (= $55V$)

- $290\mu s \rightarrow 300\mu s$: 0111 (= 85V)

It is important that the column voltages do not change during the time two rows are short-circuited or when the output of a certain row is floating. The duration of the voltage levels are not realistic, but chosen in a way to ensure the right conclusions can be made and the simulation time is not too long.

The resulting output waveforms of row 3 and row 4 are shown in Figure 9.13.

One can see that the output levels correspond to the digital input signals. Figure 9.14 shows in detail what happens during the time both rows are short-circuited.

Between $200\mu s$ and $210\mu s$, both rows are short-circuited, resulting in both rows being at the same voltage level. The exact voltage value of this level depends on the pixel voltages in both rows before they are short-circuited. In this specific case the resulting row voltage should be $\frac{5V+45V}{2} = 25V$. However, one can see in Figure 9.14 that the resulting row voltage is only about 21V. This lower voltage level is caused by the level-shifter current in the switch that short-circuits with the other row. It is very important that all of the column voltages are connected to an external voltage source when some rows are short-circuited or disconnected from any voltage source. A change in the column voltages when two rows are short-circuited results in an uncontrolled voltage change in these rows.

9.3 Simulation results

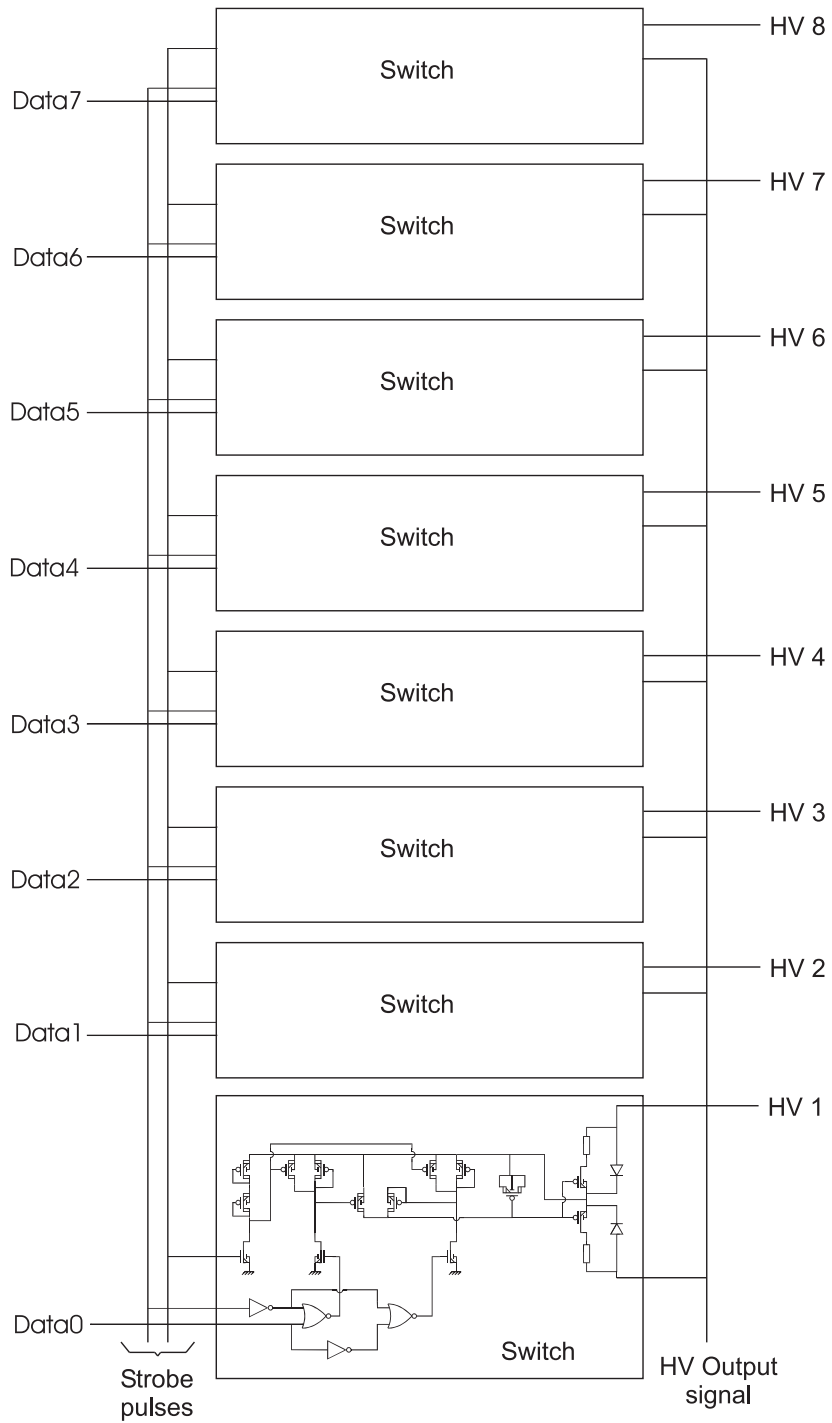


Figure 9.3: Schematic of the multiplexer

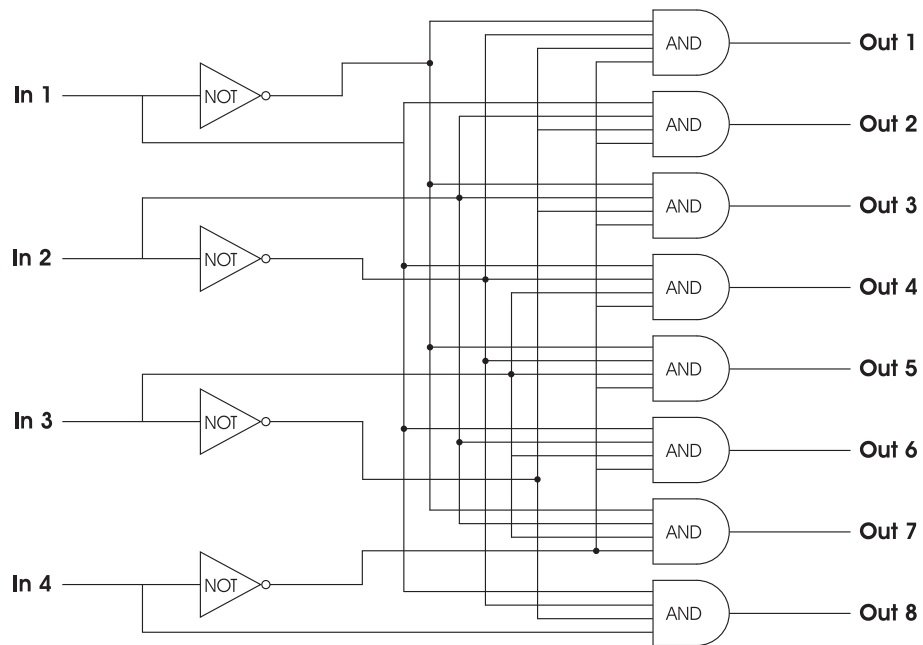


Figure 9.4: Schematic of the four to eight bit converter

9.3 Simulation results

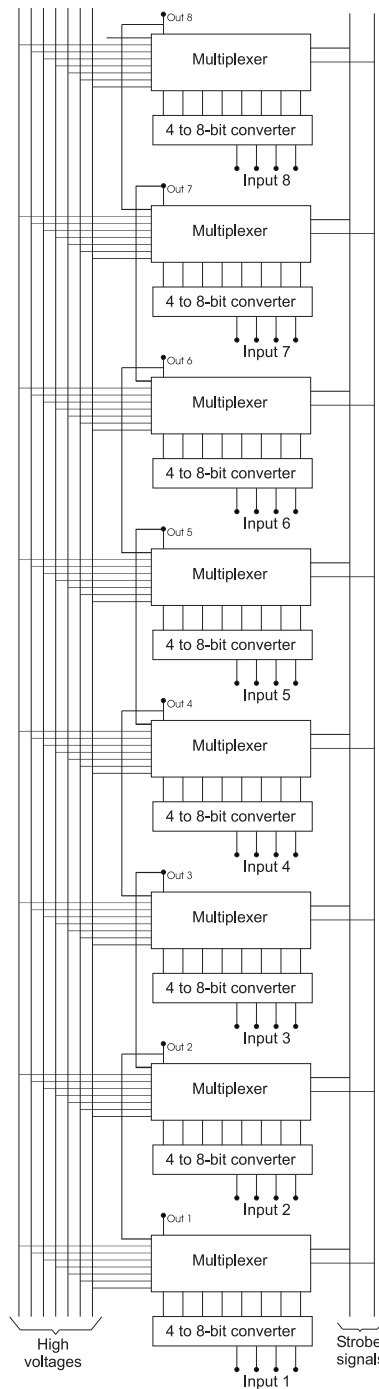


Figure 9.5: Schematic of the chip driving eight rows or columns

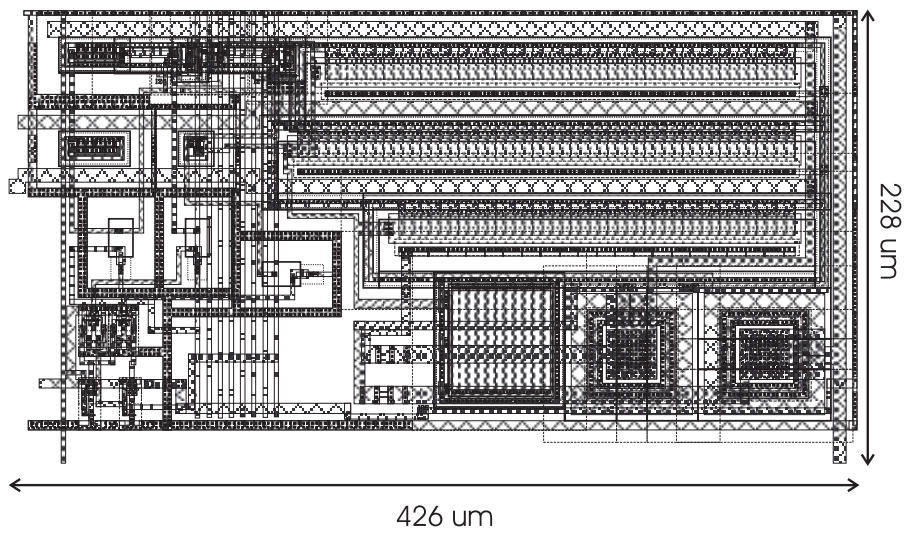


Figure 9.6: Layout of one switch

9.3 Simulation results

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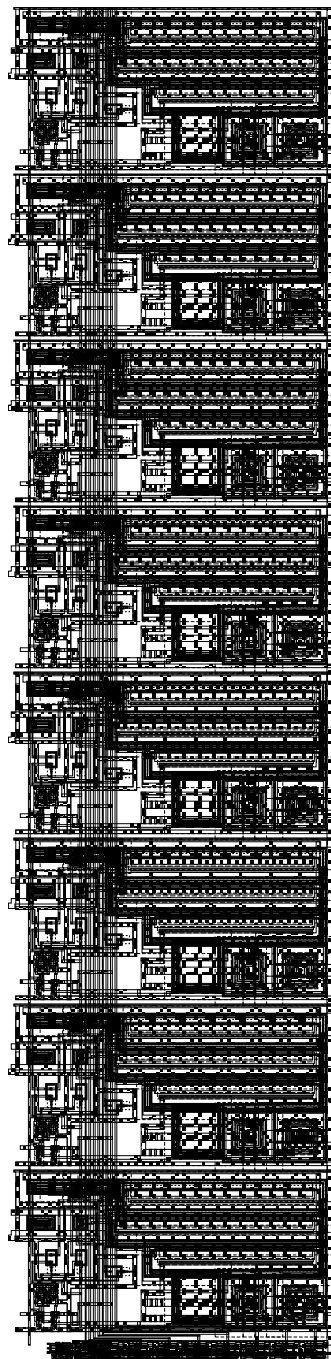


Figure 9.7: Layout of the multiplexer

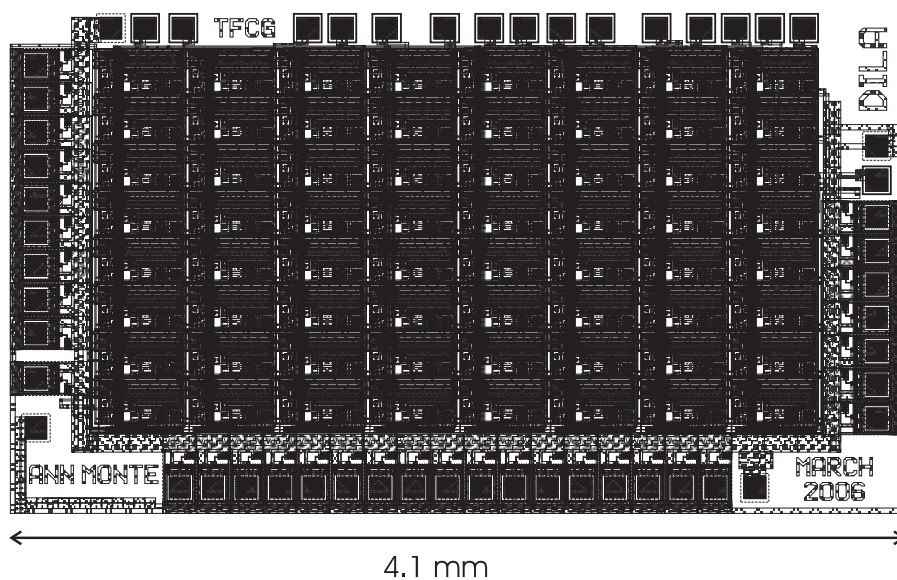


Figure 9.8: Layout of the 8-output display driver

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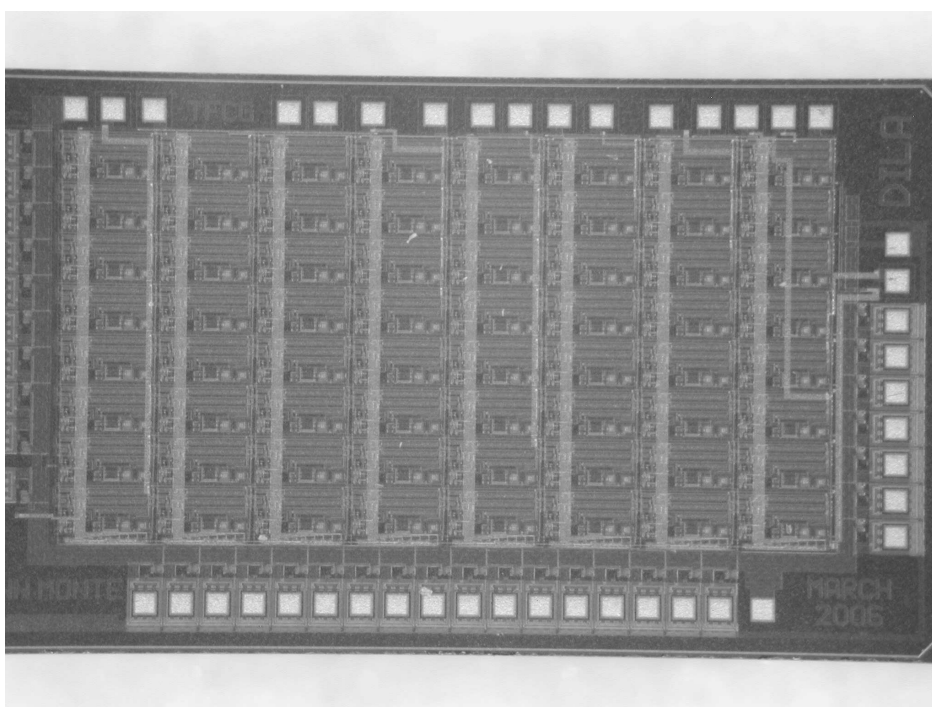


Figure 9.9: Picture of the designed DILA chip

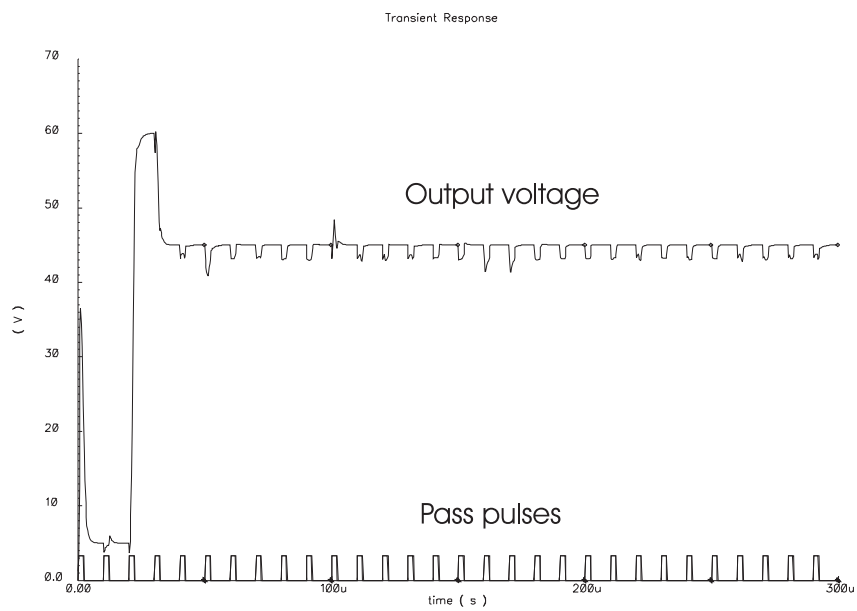


Figure 9.10: Example of a row output

9.3 Simulation results

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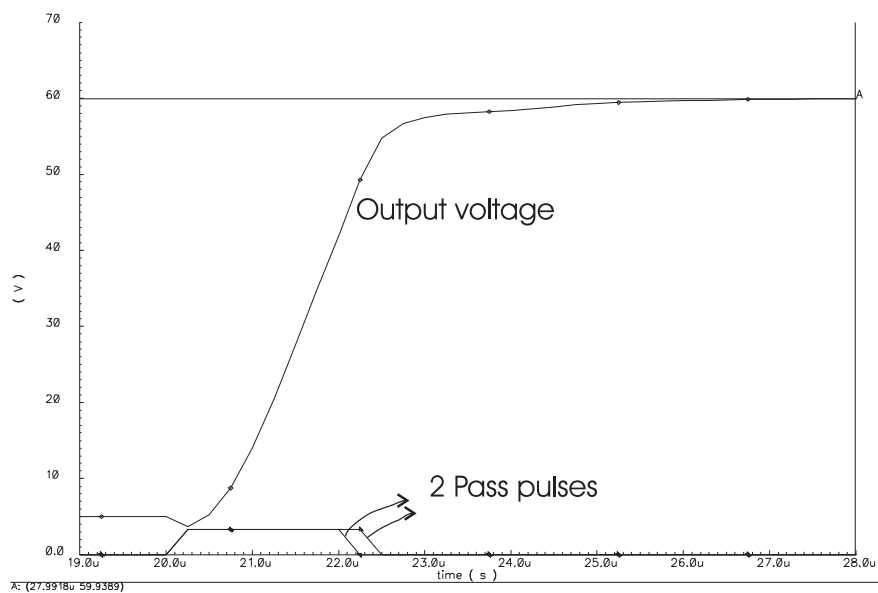


Figure 9.11: Detail of the 5V to 60V transition in the first row output

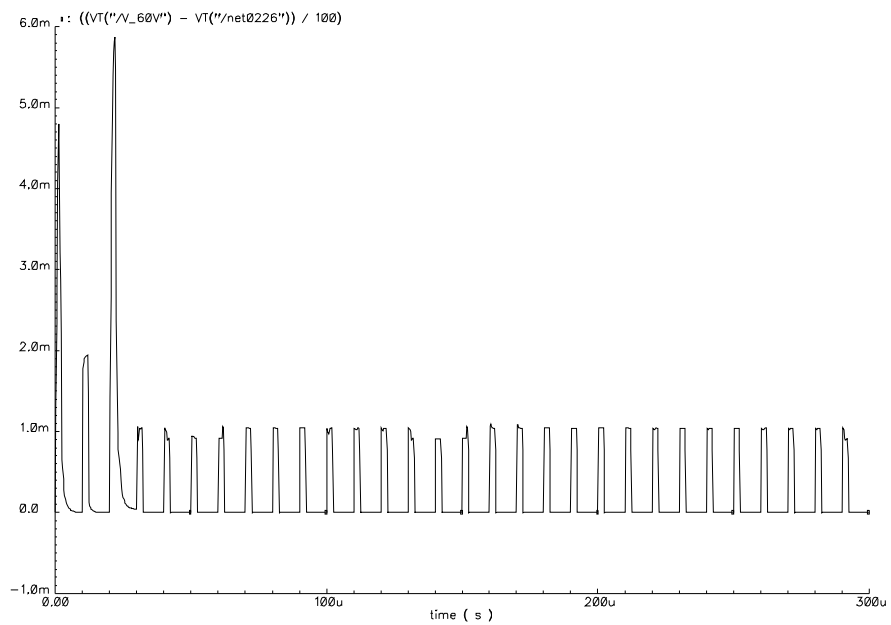


Figure 9.12: Current delivered by the 60V source during the transition 5V to 60V in the first row output

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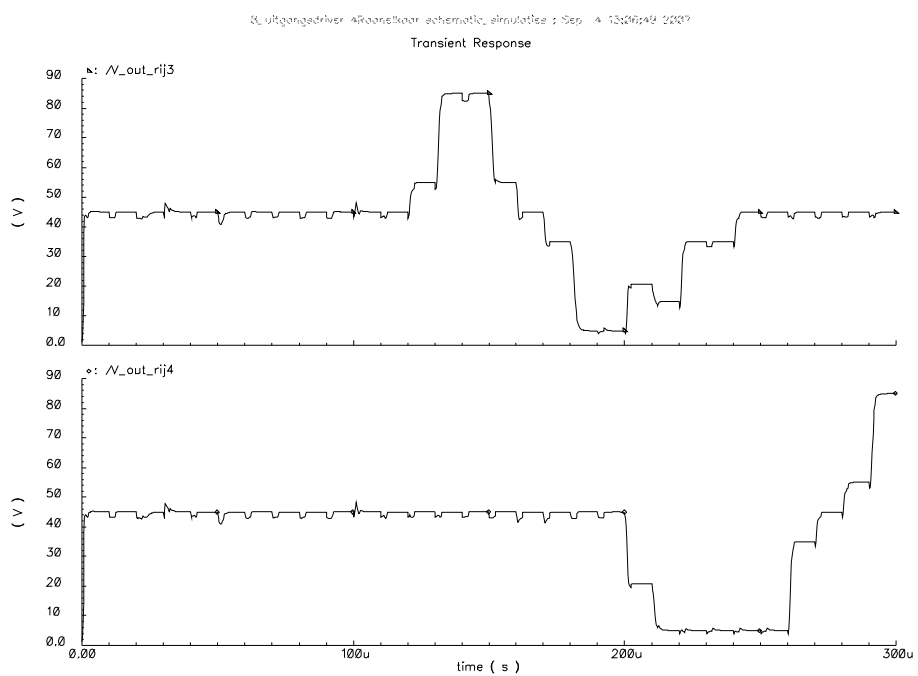


Figure 9.13: Possible output of row 3 and row 4

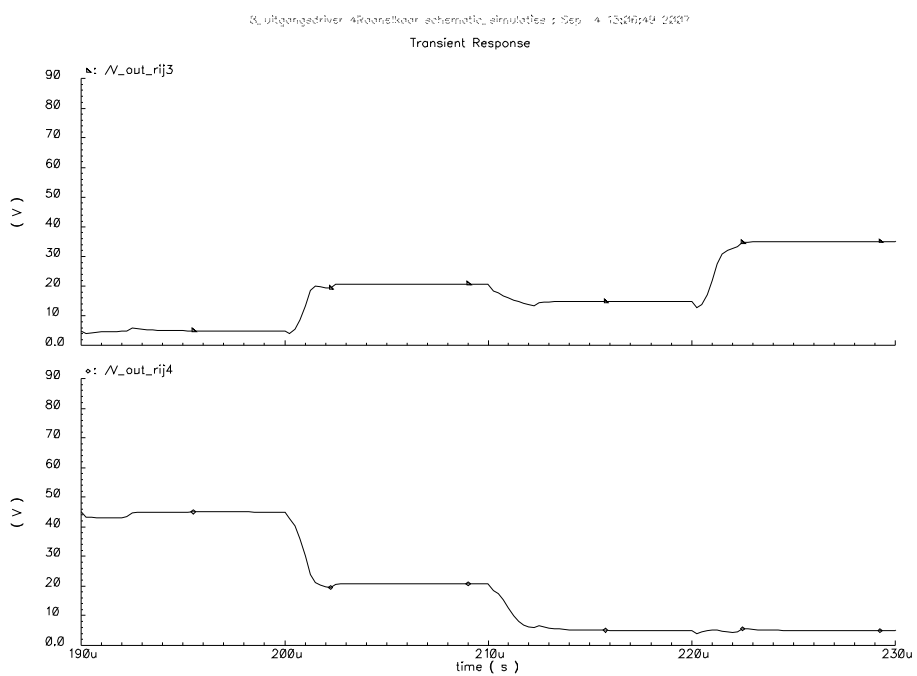


Figure 9.14: Short-circuiting row 3 and row 4

9.4 Implementation of the digital logic by means of an FPGA 185

9.4 Implementation of the digital logic by means of an FPGA

To implement the digital logic of the driver, an FPGA is used. FPGA is short for Field Programmable Gate Array. The FPGA used is the Cyclone EP1C6Q240C6 from Altera. This device supports configuration through a low-cost serial configuration device (the EPC2) [1]. By choosing this FPGA, we have one big enough in case extra features have to be added afterwards. There are 240 pins of which 180 are I/O pins. The developed driver board is used to drive a display with 16 rows and 16 columns, therefore the FPGA needs to generate the output signals to drive 32 multiplexers. The following I/O pins are needed:

- 8 data input bits for the transmission of the 260 bytes image information
- 2 control signals to control the communication with the microcontroller
- 32 x 4 data bits to drive the 32 multiplexers
- 2 pass pulses for the multiplexers
- one control signal for an external switch

The image information is processed serially. To control this incoming information, extra control signals are added such as a reset signal and a DAV (data available) signal. The reset is set to signal to the FPGA that the microcontroller is prepared to send an image. The DAV signal informs the FPGA when data can be captured.

Based on the image information, the FPGA calculates the most power-efficient drive waveforms with a line time specified by the user. Whether or not charge recycling is used, is also specified by the user. The calculation by the FPGA and the microcontroller described in subsection 8.1.2, are similar.

In order to write the software for the FPGA, the program QuartusII from Altera is used. The reset pulse, DAV, the external clock signal and dataIN are shown in Figure 9.15. The figure is a printscreen from the Quartus simulator.

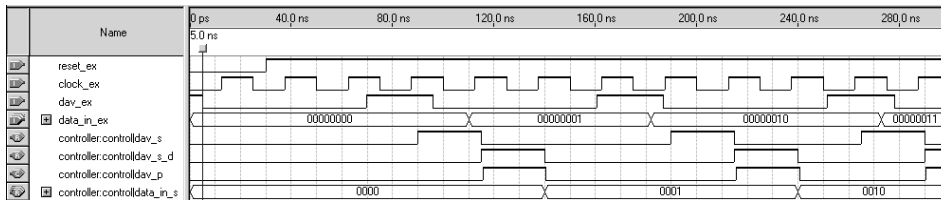


Figure 9.15: Timing of the data input signals of the FPGA

The external clock, represented by the second curve in Figure 9.15, is needed when not all of the logic is combinatorial, but timing is also important. The curve above is the reset signal, where a zero level resets the appropriate signals in the FPGA. Now, the DAV signal, the third waveform, becomes important. The fourth one is data_in_ex, representing 260 image-related signals. The next signals are internally generated signals. Figure 9.16 shows the 32 (4-bit) output signals being connected to the analogue part.

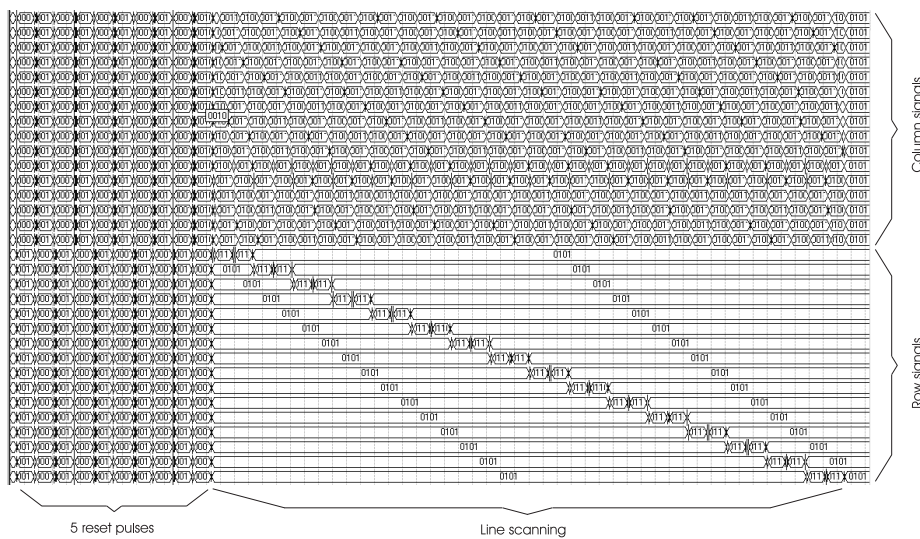


Figure 9.16: Row and column output signals of the FPGA

One can see the successive selection of the different rows. It is also possible to recognize the signals for the five reset pulses.

9.5 Practical implementation of the integrated display driver 187

9.5 Practical implementation of the integrated display driver

So far, the analogue and the digital part were discussed. However, in order to drive a display, both parts have to be able to communicate with each other and with the outside world. Therefore, a printed circuit board is designed with all the needed functionalities integrated. Integrating everything in one ASIC (Application-Specific Integrated Circuit) was also a possibility, but since doing so reduces the chance to fix any possible shortcomings, a printed circuit board was chosen.

The complete driver board contains a microcontroller responsible for the communication between a computer and the on-board flash memory on the one hand, and between the on-board flash memory and the FPGA on the other. The flash memory can contain several images. The choice of the image to be displayed is determined by the position of DIP switches or can be specified using the application interface on the computer. When an image needs to be displayed, the image information is sent to the FPGA. This then calculates the most appropriate reset and line-select waveforms to be applied to the display rows and columns and sends the correct control signals to the multiplexers in the DILA driver chips. The complete schematic of the driver board is depicted in Figure 9.17. Figure 9.18 shows a picture of the driver board.

The following components are found on the board:

- 5V voltage regulator
- 3.3V voltage regulator
- 1.5V voltage regulator
- decoupling capacitors
- RS232 connector
- MAX232 converter chip
- DS89C420 microcontroller with a 32MHz crystal oscillator
- AT29C010A 1-megabit flash memory
- DM74LS373 latch

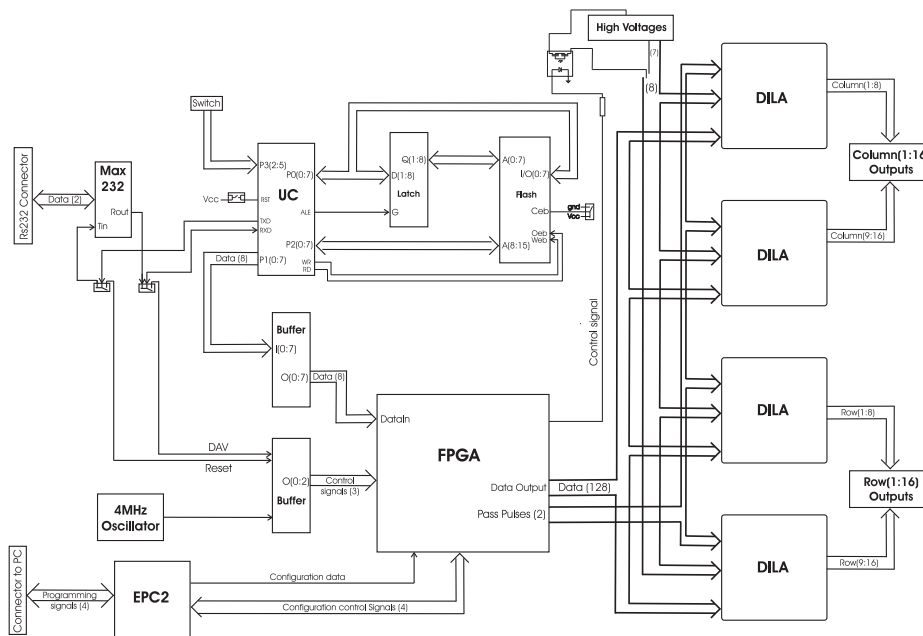


Figure 9.17: Schematic of the driver board

9.5 Practical implementation of the integrated display driver 189

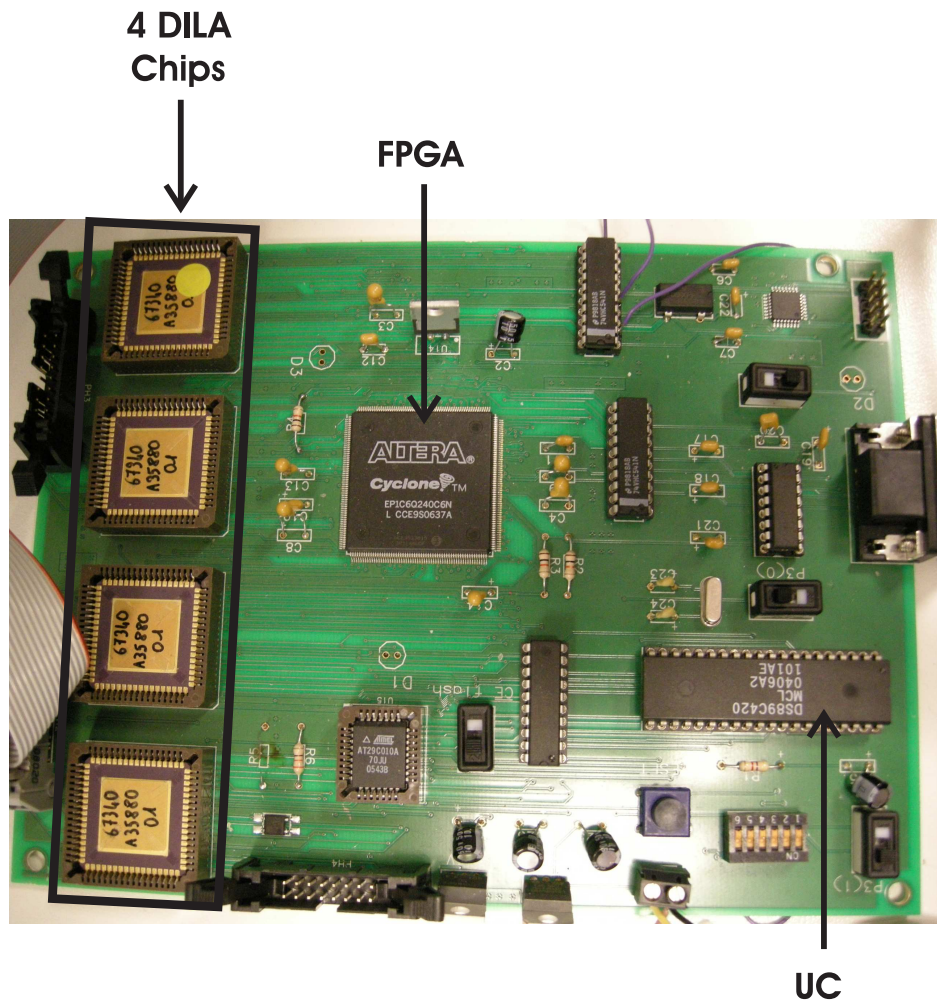


Figure 9.18: Picture of the driver board

- 74VHC541 buffer
- EP1C6Q240C6 FPGA
- JTAG connector
- EPC2 FPGA programmer
- 4 MHz Crystal Oscillator
- AQY210S switch
- 16 pin connector
- DILA chips

Next, all these components and how they are related to each other, are discussed in more detail.

9.5.1 Voltage regulators

There are three low voltages needed on the board: 3.3V used by the FPGA and the DILA chips for example, 5V used by the microcontroller and the flash memory and 1.5V used by the FPGA as well. The three voltage regulators provided on the board are shown in Figure 9.19.

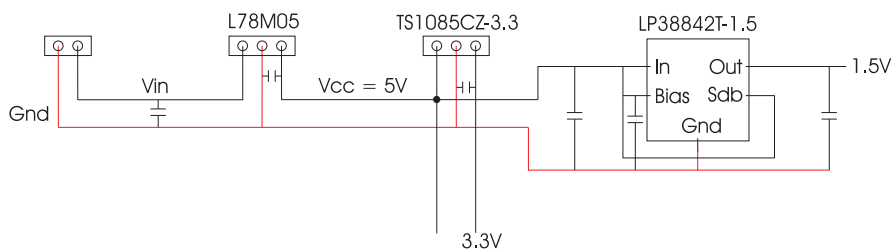


Figure 9.19: Voltage regulators to generate 5V, 3.3V and 1.5V

An external low-voltage source is connected to the board in order to deliver both a voltage around 7V and the related gnd signal. The L78M05 converts this voltage to a stabilized 5V. This 5V voltage is connected

9.5 Practical implementation of the integrated display driver 191

to the TS1085CZ-3.3 voltage regulator generating a stabilized 3.3V. The LP38842T-1.5 voltage regulator converts the input voltage to a stabilized 1.5V. Decoupling capacitors are added between the different voltage lines to avoid noise.

9.5.2 Microcontroller

The microcontroller is responsible for two tasks:

- to store the image information sent by the user by an external computer to the on-board memory
- to send the correct image information to the FPGA when a certain image must be displayed

The communication with the computer is established by an RS232 cable (already discussed in section 8.1). Therefore an RS232 connector is added together with a MAX232 chip to convert the voltage levels of the signals. Figure 9.20 gives the schematic of the microcontroller connections providing the communication with an external computer.

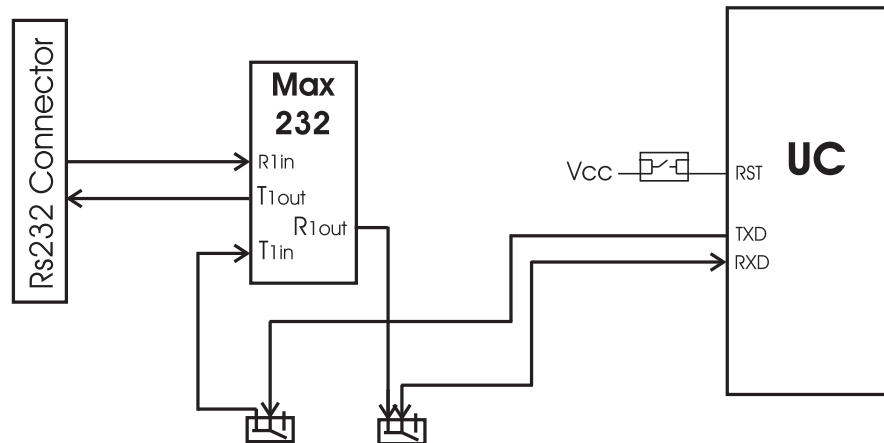


Figure 9.20: Communication between the microcontroller and an external computer

One can see the switch between the T_{1in} pin from the MAX232 and the TXD pin from the microcontroller on one hand and the one connecting the R_{1out} pin from the MAX232 and the RXD pin from the microcontroller on the other hand. These switches ensure that the microcontroller pins $P_{3,0} = RXD$ and $P_{3,1} = TXD$ can be used for other purposes.

The communication between computer and microcontroller aside, one still needs the appropriate connections with the flash memory. When writing a byte to the memory, the two address bytes and the data byte have to be specified, making three bytes in total. Since the microcontroller does not have enough I/O pins, an extra latch is used to hold the lowest address byte. The ALE (Address Latch Enable) pin controls the latch, making it transparent or hold its output. The schematic is shown in Figure 9.21.

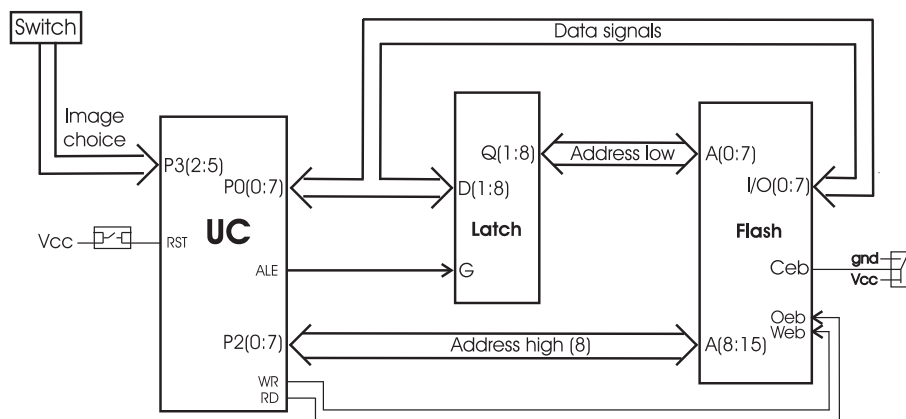


Figure 9.21: Communication between the microcontroller and the flash memory

The microcontroller first fills port P0 with the lowest address-byte, this byte is held by the latch. Next, the data-byte is sent to P0, while P2 holds the highest address-byte. As the WR-signal gets high, the data-byte is written in the flash memory to the address set by the address-byte.

The second task of the microcontroller consists of providing the correct image-information to the FPGA, therefore dip-switches are provided. Based on the position of these switches, the microcontroller determines

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a 4-bit number can be used. In order to drive a 16x16 display, 32 of these 4-bit signals need to be generated by the FPGA. The FPGA also generates the two strobe (or pass) signals controlling the timing of the switches. The connection of the FPGA with the analogue DILA chips generating the output waveforms, is depicted in Figure 9.24.

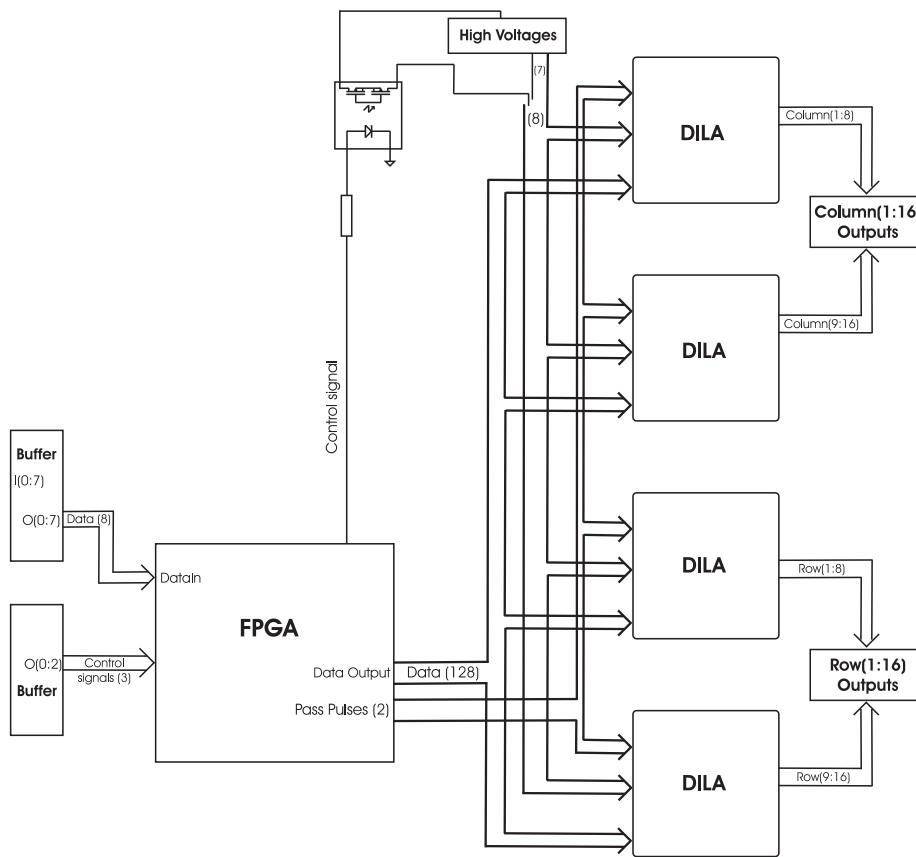


Figure 9.24: Connection between the FPGA and the driver chips

As one can see in this figure, one output signal of the FPGA is connected to a switch. When the signal is high, the switch is closed and the high row-select voltage is connected to the DILA chips. A low signal disconnects the high row-select voltage from the chips. This is done in order to provide the possibility of short-circuiting all the rows and columns without the need

for extra switches between the columns.

9.5.4 DILA chips

The in and output signals of one chip are:

- eight 4-bit input signals defining the output voltage of the rows or columns connected to the chip
- the two pass-pulses from the FPGA controlling the timing
- the HV supplies
- the low voltage supply 3.3V
- gnd
- the eight row or column outputs
- the input signal of one switch in the multiplexer connected to the last row or column, to be connected to the output of the first row or column in the next DILA chip

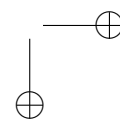
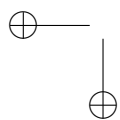
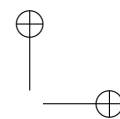
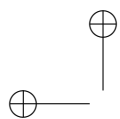
The schematic is shown in Figure 9.24.

9.6 Conclusion

A completely new test platform is developed for the new driving methods. A new test board is designed consisting of a uC, an FPGA containing the digital logic and some low-power HV driver ASICs. Both the extra logic and the design of the dynamically controlled HV multiplexers are an important feature in the design of the driver to obtain a power saving. Level-shifters in standard display driver chips exhibit continuous power dissipation, which is unacceptable since our goal is developing low-power applications. The level-shifters used in this new design however have no static power consumption at all due to the dynamic control of the charge on the gates of the output transistors, instead of the traditional voltage-control approach. The use of these dynamically controlled level-shifters leads to a significant reduction of the overall power consumption of the chip compared to conventional driver chips.

References

- [1] Altera Corporation. *Cyclone Device Handbook*, 2005.



Chapter 10

Measurement results

This chapter describes and compares the results of the measurements done with the developed driver board. In the first section, a number of plots of the most important signals are depicted. Section 10.2 shows the measured power consumption in the display driver when three different images are displayed. The measurements are performed once without the use of charge recycling by short-circuiting adjacent rows and once with the implementation of this method. Furthermore, the power measurements done in chapter 8 for the driving scheme *A4* are repeated with the new driver board.

10.1 Illustration of the output voltages and the power consumption

To verify the functioning of the developed driver board, the row and column output signals of the board are connected to a 16x16 cholesteric texture display. The selection signal of the first row when displaying Figure 10.1(c) if adjacent rows are short-circuited is shown in Figure 10.2. One can see the short intermediate voltage levels. Notice that this row-selection signal is not a square pulse from 40V to -40V, but from 85V to 5V. Since the substrate of the driver chip is chosen to be the reference potential (0V) and a voltage of at least 5V in relation to the substrate is needed at the output to ensure the proper functioning of the level-shifters, all the row and data signals are shifted over 45V. Part of the data-signal

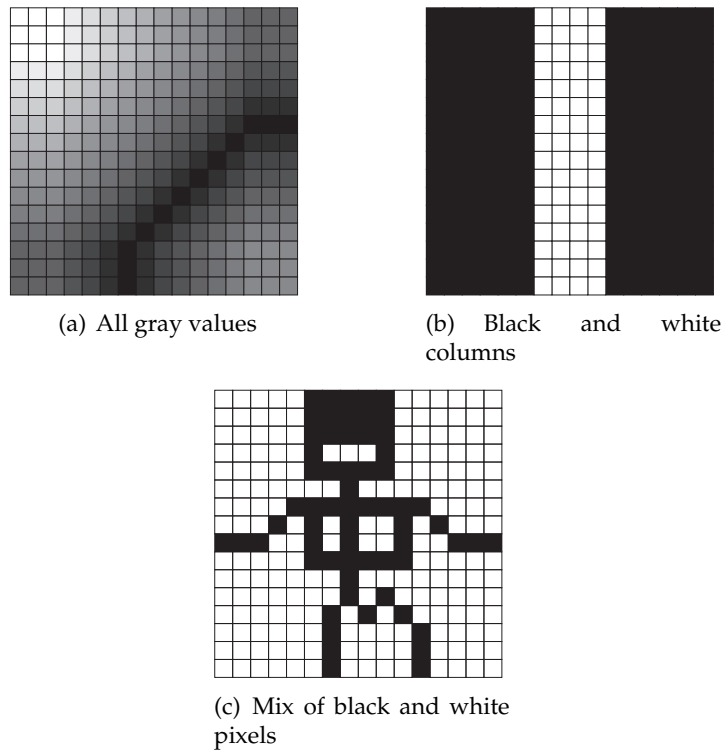


Figure 10.1: Different image patterns

applied to one of the columns is shown in Figure 10.3. It is clear that these voltage waveforms live up to the expectations.

A detailed plot of the selection waveform start is shown in Figure 10.4. One can see the transition from $45V$ to $85V$ passes through the $55V$ intermediate voltage level. Another notable fact in the row-select waveform as well as in the data waveform are the small voltage drops. An explanation for these voltage drops is given in Figure 10.5 showing the voltage over the resistor added near one of the high-voltage sources. This equals the current delivered by the high-voltage source multiplied by the resistor value. The voltage drops occur at the same time of the current pulses. When the pass pulses are set, the transistors in the levelshifters are in the conducting state and therefore cause a voltage drop over the transistors in the output stage. Figure 10.6 shows three of the current pulses in more detail. The

10.1 Illustration of the output voltages and the power consumption

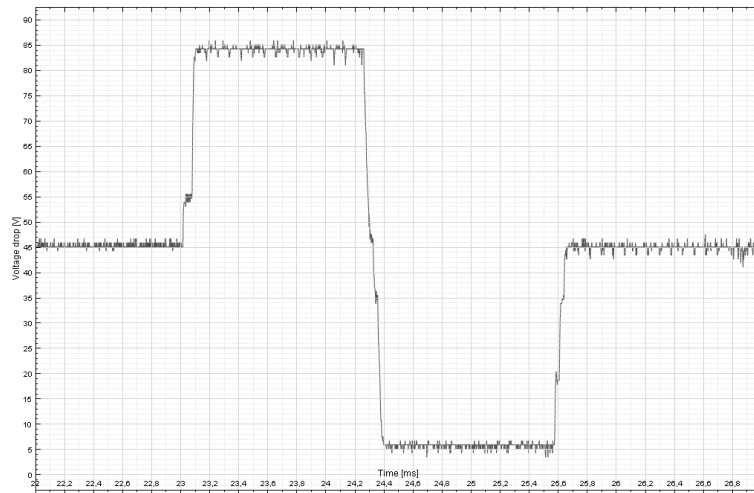


Figure 10.2: Row-select waveform

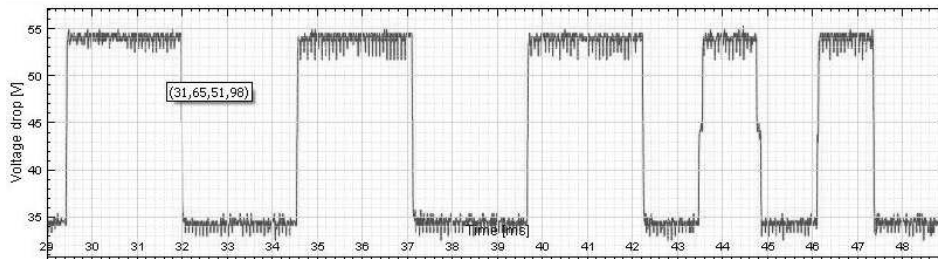


Figure 10.3: Data waveform

height of the current pulses varies according to both the number of rows and columns connected to the source and the voltage transitions over the corresponding pixels. The HV sources deliver the current consumed in the multiplexer as well as the current needed to charge the display capacitors. The pulse width of the current pulses is about $3.75\mu s$ corresponding to the width of the widest pass pulse. After $3.5\mu s$ there is a dip in the current profile due to the end of the other pass pulse. Since the power consumption is proportional to the current flow, Figure 10.5 gives an idea about the profile of the power consumption.

At the end of the selection of the first row, the row is short-circuited with

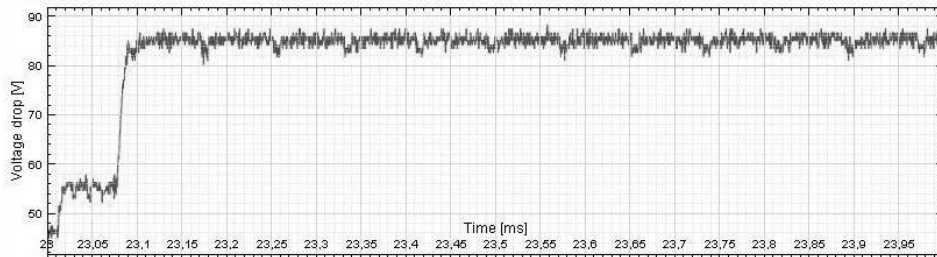


Figure 10.4: Detail of the row-select waveform

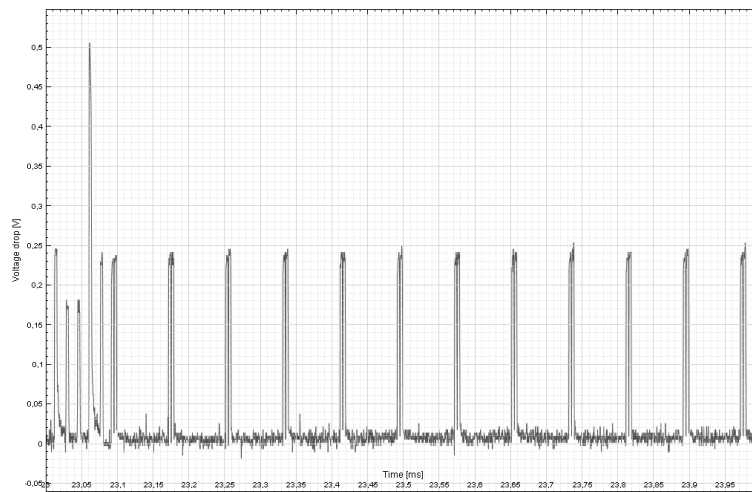


Figure 10.5: Indicator for the current delivered by one of the high-voltage sources

the succeeding second row. The profile of both voltage waveforms during that transition is shown in Figure 10.7. It is clear that the output waveforms of the driver board satisfy the conditions to drive the cholesteric texture LCD.

10.2 Measurement of the power consumption

The programme used to measure the power consumption is explained in section 8.1.1. A complete explanation of the program can be found in [1]. Table 10.1 shows the measured power consumption for the images de-

10.2 Measurement of the power consumption

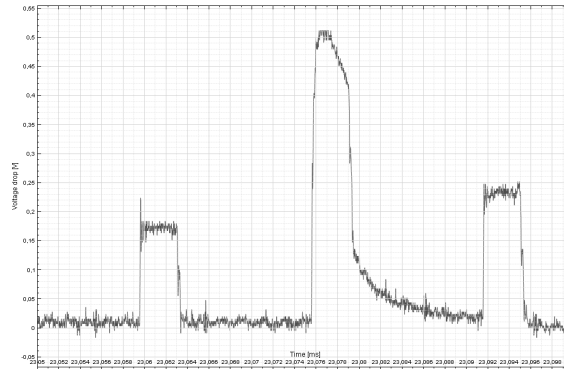


Figure 10.6: Detail of Figure 10.5

Table 10.1: Measured values of α for the images shown in Figure 10.1

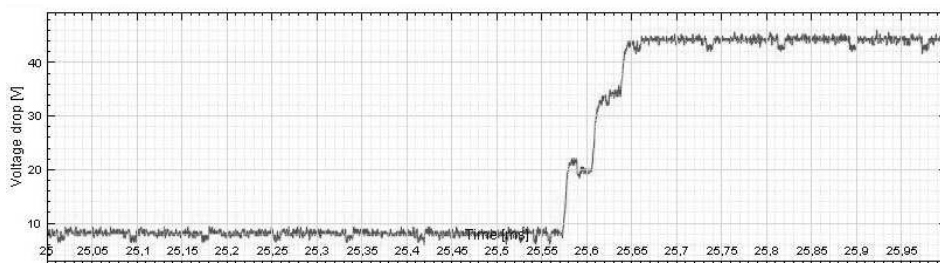
	$\alpha(V^2)$	
	no SC	SC
All grey values	322	275
Black and white columns	256	185
Mix of black and white pixels	265	245

picted in Figure 10.1. The second column gives the measured values for the images being displayed without charge-recycling by short-circuiting (SC) adjacent rows, calculated using the driving scheme presented in Figure 6.15. The third column gives the values in case adjacent rows are short-circuited, corresponding to Figure 6.18/6.19.

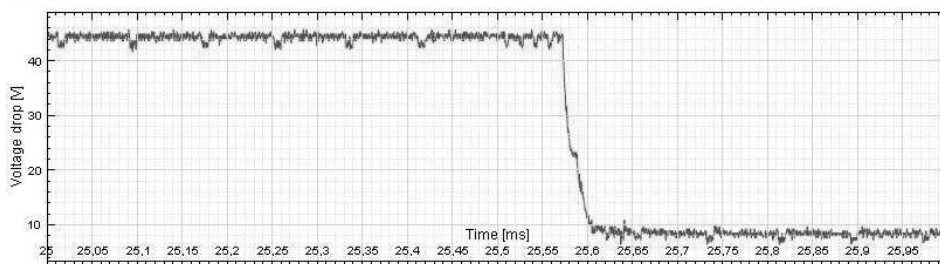
The theoretical values of α for the same images are repeated in Table 10.2. The measured values are more or less the same as the theoretical values. The correspondence is not perfect due to measurement shortcomings and

Table 10.2: Theoretical values of α for the images shown in Figure 10.1

	$\alpha(V^2)$	
	no SC	SC
All grey values	321	303
Black and white columns	272	200
Mix of black and white pixels	290	274



(a) Row1



(b) Row2

Figure 10.7: Voltage transitions in row 1 and row 2 at the end of the selection time of the first row

10.2 Measurement of the power consumption

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Table 10.3: Measured and theoretical values of α for the driving scheme A4 for the images shown in Figure 10.1

	$\alpha(V^2)$	
	measured	theory
All grey values	697	766
Black and white columns	275	350
Mix of black and white pixels	478	451

Table 10.4: Theoretical values of $\alpha(V^2)$ for a 640x480 display

	no CR	CR	A4
Only grey pixels	203	203	605
Black/white columns	202	152	205
Black/white rows	103	202	205

the fact that the power consumption is only measured during the driving of row 5 to 8.

In the end, I did the measurements again for the driving scheme A4. The results are given in Table 10.3.

These values are the results of measuring the power consumption during the driving of row 5 to row 8. It is clear once again that the behaviour corresponds to the theoretical values.

The measurements are done on a small 16x16 display. This involves that the influence of the selected rows is still relatively important. To have an idea about how scalable the results are, Table 10.4 gives the theoretical results of α for a 640x480 display.

For only grey pixels, whether or not CR is used, makes no difference in power consumption. Indeed, the waveforms over the non-selected pixels are the same in both methods. Compared to A4 the power consumption is three times less. For patterns with mostly black and white pixels, the use of CR can make a big difference. For a pronounced black/white row pattern it is a drawback to use CR. On the contrary, for a pronounced black/white column pattern, it is advantageous to implement CR.

10.3 Conclusion

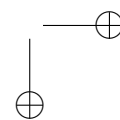
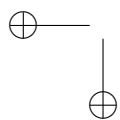
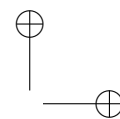
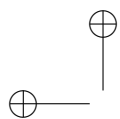
The extra logic added to the driver board is useful in decreasing the power needed to charge and discharge the display capacitances. Compared to the drive scheme A4 (Figure 5.4), a power saving of about 50% can be achieved in that part of the driver.

The measurements were done on a 16x16 display. For such a small display, the influence of the selected row is relatively high. This means that applying CR by short-circuiting adjacent rows can make a noticeable difference. With an increasing number of rows, the relative importance of the pixels on the selected row decreases and therefore the effect of this method will become smaller. For displays with a higher number of rows, the power consumption is mainly determined by the pixels on the non-selected rows and therefore by the data waveforms. However, for displays with a pronounced black/white column striped pattern, it is still a lot more efficient to reverse the waveforms on the even rows. The fact also remains that the developed drive schemes are still more than 50% power-efficient than the traditional drive schemes regardless of the number of rows.

The achieved results are also applicable to any kind of bistable display that has a capacitive nature. The developed driver board can be used to drive those displays insofar no special demands are made concerning the exact profile of the waveforms (for example the slope of the waveforms).

References

- [1] J. Verbrugghe. *Optimalisatie van de aansturing van bistabiele beeldschermen*. 2007.



Chapter 11

Conclusions and outlook

11.1 Main achievements

The main objectives of this Ph.D. work were the creation of new power-efficient driving schemes for bistable displays and the development of the required basic building blocks (hardware/software) to integrate the new driving schemes in a driver chip. These objectives are realized through the development of a driver board for a bistable cholesteric texture liquid crystal display. Its most important characteristic is the reduction of the power needed to charge and discharge the display capacitors. To reach this goal, I first did a theoretical analysis and some hand made calculations leading to a theoretical optimal drive scheme. These calculations and how they are used to compose a drive scheme are explained in chapters 4, 5 and 6. Following this, I wrote a programme that calculates the power consumption in drivers for displays with all possible dimensions. Since these results were promising, it was time to test the drive scheme on a real display. A driver board developed some years ago in our research group was used. This board is described in chapter 7. In order to test the drive scheme, the logic that calculates the drive waveforms needed to be programmed in a microcontroller. The microcontroller, programmed in assembler, generates the control signals for the levelshifters switching the correct voltage to the output. With this driver board, it was possible to measure the merits of using intermediate voltage levels. It was not possible to verify the influence of short-circuiting rows since the extra switch needed was not available. The measurement results were satisfying so a

new driver board was developed containing the digital logic and a suitable analogue part. The analogue chips containing the multiplexers were designed in Cadence. The extra logic was programmed in an FPGA using Quartus. For the design of the printed circuit board, Mentor was used. All these elements together worked out fine and the measurements could start. The measurements were done for three different image patterns. For each of them the energy consumption was measured twice. Once in case adjacent rows are short-circuited during the transition from one selected row to the other, once without short-circuiting adjacent rows. In both cases intermediate voltage levels were added. The results of these measurements confirm the theoretical results. An average power saving of about 50% is achieved using the display driver proposed in this Ph.D.

11.2 Future work

There are still other possibilities to enhance the display driver. It is still interesting to find out whether Multiple Line Addressing can be useful. Furthermore it would be interesting to reduce the power consumption in the analogue part of the driver even more. Especially for applications like e-books, it is not needed to have a fast switching time of the liquid crystal. Due to this easier boundary condition, it is possible to lower the current in the levelshifters.

Once the basic building blocks are optimized in accordance with the application, the final step should be the integration of the FPGA logic into an ASIC together with the analogue HV part in a smart power technology like I2T100 or in a pure CMOS technology.